

A single ended dynamic feedback control 8T sub threshold SRAM cell

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ABSTRACT: In this paper an 8T RAM cell with high information security that works on ULV is proposed. The proposed cell's zone is twice as that of 6T. The proposed 8T cell has high solidness and can be worked at ULV of 200–300 mV power supplies. The upside force utilization of the proposed 8T cell empowers that it should be utilized for battery worked SoC plan. Future and utilizations of the proposed 8T cell can possibly be in low/ULV and medium recurrence operation like neural sign processor, subthreshold processor, wide-working extent IA-32 processor, quick Fourier change centre, and low voltage reserve operation. At last it can be observed that proposed system gives better results compare to existed one.

KEY WORDS: 8T RAM Cell, ULV, RBL, RWL.

I.INTRODUCTION

The growing demand of portable battery operated systems has made energy efficient processors a necessity. For applications like wearable computing energy efficiency takes top most priority. These embedded systems need repeated charging of their batteries. The problem is more severe in the wireless sensor networks which are deployed for monitoring the environmental parameters. These systems may not have access for recharging of batteries. We know that on chip memories determine the power dissipation of SoC chips. Hence it is very important to have low power and energy efficient and stable SRAM which is mainly used for on chip memories.

There are various approaches that are adopted to reduce power dissipation, like design of circuits with power supply voltage scaling, power gating and drowsy method. Lower power supply voltage Reduces the dynamic power in quadratic fashion and leakage power in exponential

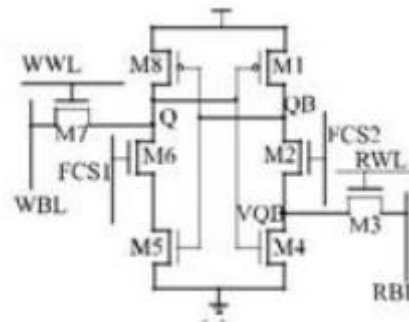
Way. But power supply voltage scaling results in reduced noise margin. Many SRAM arrays are based on minimizing the active capacitance and reducing the swing voltage. In sub-100nm region leakage currents are mainly due to gate leakage and sub threshold leakage current. High dielectric constant gate technology decreases the gate leakage current. Forward body biasing methods and dual V_t techniques are used to reduce sub threshold leakage current. The sub threshold of SRAMs is lower than the transistor threshold voltage (V_t). Now the sub threshold leakage current is the operating current.

The energy loss during writing is more than the energy loss during reading in conventional SRAM since there is full swing of voltage in bit lines whereas the bit line voltage swing is very less during reading. It is known that the energy stored in the bit lines of the conventional

presented in read way. This spillage current increments with the scaling consequently, expanding the likelihood of fizzled read/compose operations. Comparative the cells will keep the cell current without aggravating the capacity hub as additionally.

III. PROPOSED SYSTEM

Single-finished with element criticism control cell is displayed to make a cell stable in all operations, as shown in Figure (2). The single-finished configuration is utilized to decrease the differential exchanging power and read–write operation. The force expended and exchanging/flipping of information on single piece line is lesser than that on differential bit-line pair. The RAMempowers composing through single nMOS in 8T. It likewise isolates the read and composes way and displays read decoupling. The basic change of cell is considered to upgrade the safety against the process–voltage– temperature (PVT) varieties.



It is a 1) of 8T cell in sub threshold/close edge area. The proposed 8T has one cross-coupled inverter pair, in which every inverter is comprised of three fell transistors. These two stacked cross-coupled inverters: M1–M2–M4 and M8–M6–M5 hold the information amid hold mode. The compose word line (WWL) controls one and only nMOS transistor M7, used to exchange the information from single compose bit line (WBL). A different read bit line (RBL) is used to exchange the information from cell to the yield when perused word line (RWL) is initiated. Two segments one-sided criticism control signals: FCS1 and FCS2 lines are utilized to control the input cutting transistors: M6 and M2, individually.

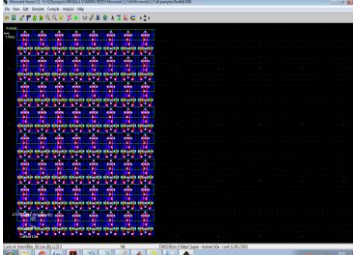
- 1) **Cell Layout:** For examination of region, format of 5T, 6T, RD-8T, and proposed 8T are attracted UMC 90-nm CMOS innovation. The sizes of MOSFETs utilized as a part of proposed 8T cell are delineated. The RD-8T involves 1.3× range as contrasted and that of 6T. Because of the configuration limitations and contact region between M2, M3, M4, and M8 the 2 × zones will be contrasted on 6T cell.
- 2) **WriteOperation:** The criticism slicing plan is utilized to compose into 8T. In this plan, amid compose 1 operation FCS1 is made low which switches OFF M6. At the point when the RWL is made low and FCS2 high, M2 conducts associating Complementary Q (QB) to the ground. Presently, if the information connected to word bit line (WBL) is 1 and WWL is actuated, then current streams from WBL to Q and makes a voltage trek on Q by means of M7-composing 1 into the cell.
- 3) **Read Operation:** The read operation is performed by precharging the RBL and enacting RWL. On the off chance that 1 is put away at hub Q then, M4 turns ON and makes a low resistive way for the stream of cell current through RBL to ground. This releases RBL

rapidly to ground, which can be detected by the full swing inverter sense intensifier. Since WWL, FCS1, and FCS2 were made low amid the read operation

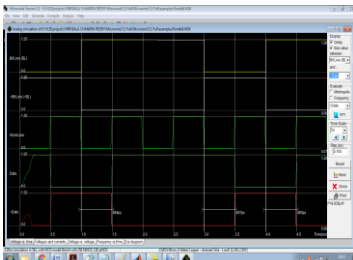
- 4) **Half-Selected Issue:** At whatever point a cell is chosen for compose operation, the voltage of genuine stockpiling hub (Q) of line half-chose cells will ascend because of charge exchange from WBL. The reciprocal stockpiling hub QB does not have solid association with the bit line (RWL is OFF) and in this way, less opportunities to flip the cell as com-pared with traditional 6T/RD-8T cell. This can be checked by 1000 Monte Carlo (MC) re-enactments, as appeared.

IV. RESULTS

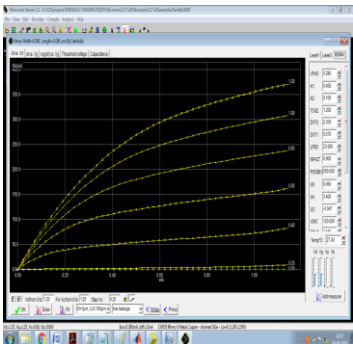
LAYOUT IN MICROWIND



LAYOUT OUTPUT



DRAIN VOLTAGE VS CURRENT



V. CONCLUSION

An 8T SRAM cell with high information security (high μ and low σ) that works in ULV supplies is exhibited. We achieved improved SNM in sub threshold administration utilizing SE-DFC and read decoupling plans. The proposed cell's zone is twice as that of 6T. Still, it's better implicit procedure resistance and element voltage relevance empowers it to be utilized like cells (8T, 9T, and 10T). The proposed 8T cell has high solidness and can be worked at ULV of 200–300 mV power supplies. The upside of lessened force utilization of the

proposed 8T cell empowers it to be utilized for battery worked SoC plan. So at last it can conclude that the proposed system gives better efficiency compared to exist one.

VI. REFERENCES

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