International Journal of Research
Available at https://edupediapublications.org/journals
e-ISSN: 2348-6848
p-ISSN: 2348-795X
Volume 05 Issue 19
August 2018

TEN-SWITCH UNIFIED POWER QUALITY CONDITIONING SYSTEM

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Abstract:

This paper proposes a new topological configuration for a unified power quality conditioner (UPQC). Generally, the power structure of the three-phase three-wire UPQC consists of two voltage source inverters (VSI) by using 12 switches, connected in six for shunt and six for series arrangement with the grid. For this configuration, six of the series inverter switches will be underutilized most of the time. To improve the semiconductor utilization and consequently to reduce switching losses, this paper proposes a new reduced switch topology for the UPQC. The proposed topology is realized using only ten switches and retains all the performance merits of the 12-switch UPQC while minimizing its underutilization without increasing the switch VA rating. The paper provides a detailed analytical study and evaluation by comparing the proposed topology with the twelve- and nine-switch-based UPQC system configurations.

I INTRODUCTION

A unified power quality conditioner (UPQC), it is probable to ensure a controlled voltage for the loads, balanced and with low harmonic distortion and at the same time draining undistorted currents from the utility grid, even if the grid voltage and the load current have harmonic substances. The UPQC contains of two active filters, the Series Active Filter (SAF) and the Shunt or Parallel Active Filter (PAF)THE ever increasing use of solid state technology in industrial and domestic applications is extensively contributing towards line current harmonics, leading to nonlinear voltage drops, cables overheating, poor power factor and additional power losses at distribution levels [1]-[2].

This paper proposes a new reduced switch UPQC system topology that comprises of ten switches in total. The main objective is to reduce the overall switch count of the back-to back UPQC system while retaining its operational features without any performance tradeoff. To

International Journal of Research
Available at https://edupediapublications.org/journals
e-ISSN: 2348-6848
p-ISSN: 2348-795X
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maintain the linear modulation range and uniform switching frequency for all the switches within the proposed topology, a carrier based double zero sequence injection scheme is also developed. An appropriate control algorithm is developed to achieve the seamless operation of the proposed UPQC topology under different operating conditions.

A UPQC generally consists of two voltage source inverters (VSI), connected in shunt and series configuration with the grid, at the point of common coupling (PCC) and share a common dc link capacitor [4]. The series VSI protects the downstream loads from sags/swells in the PCC voltage whereas the shunt VSI reduces the upstream line losses by compensating the harmonic distortion and reactive component of the load current. When the voltage at PCC is distorted, the series VSI can be additionally controlled to mitigate and prevent the voltage harmonics from reaching the load [10]. The proposed topology is realized using only ten switches and retains all the performance merits of the twelve- switch UPQC while minimizing its underutilization without increasing the switch VA rating.

II THREE PHASE THREE WIRE UPQC SYSTEM CONFIGURATIONS

For three-phase-three-wire system, generally, the back-to back inverter based UPQC system is widely used and is shown in Fig. 1.

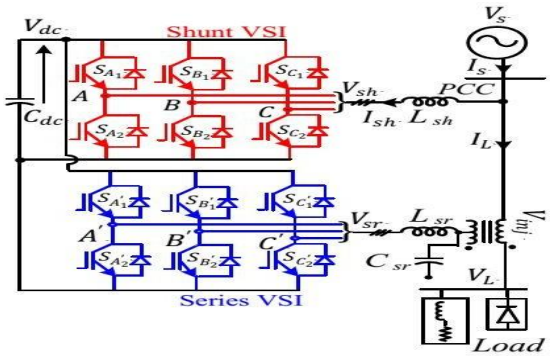

Fig. 1. Twelve-switch UPQC topology.

It comprises of twelve power semiconductor switches in total. Switches constitute the shunt VSI which is connected at the PCC, whereas, the switches constitute the series VSI and is connected between the PCC and load. Both inverters share the common dc link capacitor. As shown in Fig. 1, the twelve- switch UPQC deploys two dedicated inverters for performing the UPQC functionalities. This feature allows UPQC to have shunt VSI connected at either the PCC or load with no effect on the compensation ability.

Recently, there has been an effort to reduce the total switch count of in Fig. 1, the reduced nine-switch UPQC topology is achieved. This configuration has a set of three shared switches as illustrated in Fig. 2.

the UPQC as reported. By merging the lower three switches of the shunt VSI

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p-ISSN: 2348-795X
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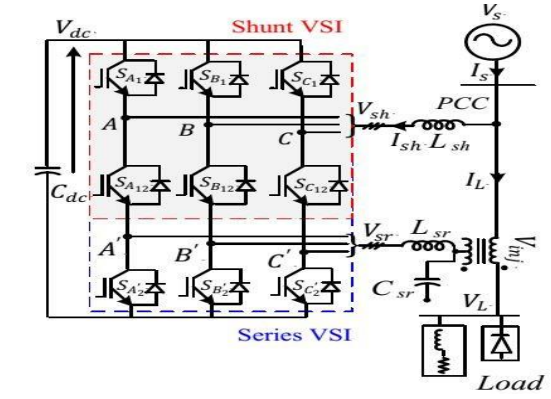

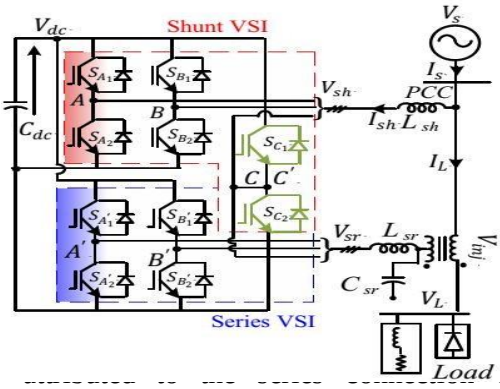

of three
under
crease in
causes
atings of
mainly
of three

switches in each leg. Therefore, six out of nine switches must be oversized for adequate operation of the nine-switch UPQC. In addition, all the nine switches must remain operational irrespective of the UPQC compensation mode. Thus, the reliability of the nine-switch UPQC reduces for a single switch malfunction.

III PROPOSED TEN-SWITCH UPQC TOPOLOGY

In this paper, a new topology of UPQC, based on ten switches, is proposed for power quality enhancement applications. As depicted in Fig. 3, the proposed topology is realized by combining the phase C switches of shunt and series VSI {S_{C1}, S_{C2}} and {S_{C1F} , S_{C2F} }in Fig. 1, respectively, into a common leg with a shared set of two switches S_{C1} and S_{C2}. Until now the ten-switch structure has been utilized in following subsection provides an overview of the ten- switch related work in the literature UPQC topology

Fig. 3. Proposed ten-switch.

A. Existing constraints and background work related to ten switch structure

Like most reduced semiconductor topologies, ten-switch structure faces restriction on its allowable switching states for the shared leg (phase C in Fig. 3).

TABLE I

SWITCHING STATES FOR PHASE "C" OF SHUNT AND SERIES VSI IN TWELVE-SWITCH CONFIGURATION

International Journal of Research
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e-ISSN: 2348-6848
p-ISSN: 2348-795X
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Voltage	Switching State
$V_{sh} = V_{sr} = V_{dc}$	$S_{C1}, S_{C'1}$= ON and $S_{C2}, S_{C'2}$= OFF
$V_{sh} = V_{sr} = 0$	$S_{C2}, S_{C'2}$= ON and $S_{C1}, S_{C'1}$= OFF
$V_{sh} = V_{dc}$ and $V_{sr} = 0$	$S_{C1}, S_{C'2}$= ON and $S_{C2}, S_{C'1}$= OFF
$V_{sh} = 0$ and $V_{sr} = V_{dc}$	$S_{C2}, S_{C'1}$= ON and $S_{C2}, S_{C'1}$= OFF

The switching state where the upper terminal is connected to and lower terminal is connected to ground or vice-versa is not realizable as it will result in a direct short circuit of the dc bus. The blocking of two (out of four) states limits the dc link voltage available for the shared leg ("phase C") to half of its value for back-to back configuration.

TABLE II

SWITCHING STATES FOR PHASE "C" OF SHUNT AND SERIES VSI IN TEN-SWITCH CONFIGURATION

Voltage	Switching State
$V_{sh} = V_{sr} = V_{dc}$	S_{C1} = ON and S_{C2} = OFF
$V_{sh} = V_{sr} = 0$	S_{C1} = OFF and S_{C2} = ON
$V_{sh} = V_{dc}$ and $V_{sr} = 0$	Not Realizable
$V_{sh} = 0$ and $V_{sr} = V_{dc}$	Not Realizable

Ten-switch configuration was earlier reported in [14]-[16] to replace twelve-switch back- to-back converter for dual induction machine drive system. Although the configuration allows independent control of both machines with a wide range of variation in load torque and rotational speeds, it imposes a limitation on the dc link voltage.

If U_{m1} and U_{m2} are the maximum values of phase- to- phase voltages at the terminals of the induction machine M_1 and M_2, respectively, it is shown that,

$V_{DC} \geq \max (U_{m\,1} + U_{m\,2})$, for the ten − switch system

$V_{DC} \geq \max (U_{m\,1} + U_{m\,2})$, for the twelve − switch system (1)

Where V_{DC} is the voltage across the dc link capacitor. In the special case of $U_{m1} = U_{m2} = U$ the following constraints can be established.

$V_{DC} \geq 2U$, for the ten − switch system

$V_{DC} \geq 2U$, for the twelve − switch system (2)

Equation (2) implies that the dc-link voltage must be doubled to achieve the maximum rotational speed for both machines simultaneously. Doubling of dc-link voltage increases all the component stress by two folds, thus offsetting the saving of two switches. For the same dc-link voltage, the ten-switch structure leads to reduction in the terminal voltage and consequent speed range of both machines.

Attempts to enhance the dc-bus utilization for the ten-switch architecture have been reported in [18]–[21]. The improvement reported in [18] is obtained at the expense of identical operating (speeding and loading) conditions for both machines. In [19], the

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e-ISSN: 2348-6848
p-ISSN: 2348-795X
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controller divides the dc-link voltage by allocating prede- fined switching vectors to each machine. The restriction that the controller must have prior knowledge of the voltage profile for each machine makes the scheme impractical for variable in- dustrial loads. In [20], the ten-switch configuration is employed to drive the two induction motors in the center-driven winders. It overcomes the limitation of dc-link oversizing given by (1) and (2) due to "inverse loading profile" of the two machines. When one motor operates at maximum speed, the other motor operates at minimum speed and *vice versa*. Since both mo- tors increase/decrease speed in an alternate fashion, their volt- age requirement is completely different (opposite). This allows the ten-switch system to remain operational for center-driven winders utilizing the same dc-link voltage required for back-to- back converter. However, the center-driven winder is a special case, and, in general, the ten-switch configuration has not shown much economic value for dual-motor drive systems.

B Proposal

This paper proposes the use of ten-switch configuration as the most suitable candidate for shunt-series configuration, such as, UPQC. The rationale behind this recommendation is given below. shared leg during normal (upper) and sag (lower) mode of operation in the proposed configuration.

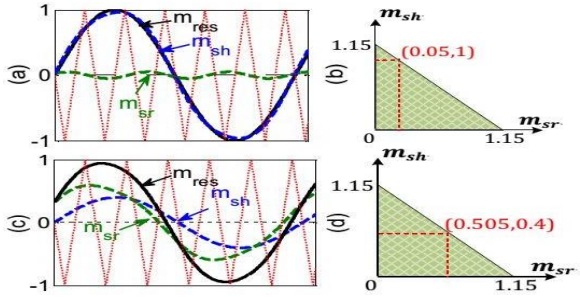

Fig. 4. Modulation references transition for

As shown in Fig. 3, the outputs of the upper VSI are connected to the PCC constituting the shunt configuration whereas, the outputs of lower VSI are connected in series with the same PCC constituting the series configuration. The shared set of switches

S_{C1} and S_{C2} are driven by the modulation signal which is calculated as follows.

$$m_{res} = m_{sh} + m_{sr} \quad (3) \qquad (3)$$

where m_{sh} and m_{sr} are the amplitude of the modulating sig- nal for shunt and series VSIs, respectively. m_{res} is the resultant modulating signal for the shared set of switches. Fig. 4(a) shows these details within the bandwidth of the dc-link voltage in per unit (p.u.), where 1, 0, 1 corresponds to V_{dc}, 0, V_{dc} . To maintain the linear range of modulation for S_{C1} and S_{C2}, the maximum allowable limit for m_{res} is 1 to +1. This limit can be further stretched by 15% using third-harmonic injection [11],

[12] extending the linear range from 1, 1 to [1.05, 1.15] as shown in Fig. 4(b) and (d). Thus, up to 15% total

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harmonic distortion (THD) in the PCC voltage can be compensated with- out increasing the dc-link voltage. For higher values of voltage THD, (i.e., >15%), like all existing configurations, the proposed topology will also require a higher dc-link voltage.

During normal condition, the shunt VSI supplies harmonic and fundamental reactive component of the load current, while the series VSI injects the inverse of PCC voltage harmonics usually <5% [11]. Since the shunt VSI operates at the same voltage level as PCC (1 p.u.), its reference signal amplitude is also unity. From (3), the amplitude of the reference signal for shared leg can go as high as 1.05 as shown in Fig. 4(a). If an ideal grid is considered (with no distortion in PCC voltage), the series VSI will simply operate with a modulation index of zero and

$m_{res} = m_{sh} = 1$.

Now consider that there is sag of magnitude ΔV_{sag}(p.u.) in the PCC voltage. On the occurrence of sag, the PCC voltage undergoes a reduction of ΔV_{sag}. The shunt VSI modulation index also decreases proportionally to the new value of $(1-\Delta V_{sag})$. The series VSI compensates the sag by injecting a fundamental voltage given by

$$V_{sr} = V^{*}L - V_{pcc} \quad (4)$$

where $V^{*}L$ is the nominal load voltage. The new modulation index of the series VSI increases from 0.05 to ΔV_{sag} + 0.05. Fig. 4(c) reflects the transition in all three modulation indexes m_{sr}, m_{sh}, m_{res} from normal to sag mode of operation.

It can be observed from Fig. 4(a) and (c) that the resultant modulation signal for the shared leg (phase *"C"*) does not ex- tend out of the dc-link bandwidth during both (normal and sag) modes of operation. This is attributed to the fact that amplifica- tion in m_{sr} by any amount is always accompanied by a reduction in m_{sh} by the same factor. The self-tuning feature of both the modulation references causes the shared leg switches to always operate in the linear range of modulation. Thus, the proposed configuration can be considered as the most suitable application of a ten-switch topology. Fig. 4(b) and (d) reflects the opera- tional area of the ten-switch UPQC for normal and sag mode of operations, respectively. The operating points {0.05, 1} in Fig. 4(b) and {0.505, 0.4} in Fig. 4(d) correspond to the normal mode in Fig. 4(a) and sag mode in Fig. 4(c), respectively.

IV SWITCH RATING ANALYSIS

In Section III, a subjective explanation is presented to use ten- switch configuration as UPQC. Despite its two switch saving feature, the effectiveness of the proposed ten-switch UPQC can only be evaluated after comprehensive analysis of its switch rating. Therefore, an analytical study is presented in this section to

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e-ISSN: 2348-6848
p-ISSN: 2348-795X
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determine and compare the switch rating of the ten-switch UPQC with the twelve- and nine-switch topologies.

From Fig. 1, the p.u. current flowing in the series and shunt VSI can be expressed as

$$\left.\begin{aligned} i_{\mathrm{sr}} &= \frac{i_L \angle\theta_{La}}{n_t} = \sum_{h=1}^{\infty} I_L \cos\left(hw_L t + \varphi_{Lh}\right) = I_L \angle\theta_L = 1\angle\theta_L \\ i_{\mathrm{sh}} &= \sum_{h=1}^{\infty} I_{\mathrm{sh}} \cos\left(hw_{\mathrm{sh}} t + \varphi_{\mathrm{sh}-h}\right) = \left(1\angle\theta_L - 1\cos\theta_L\right) + I_{1K} \end{aligned}\right\} \quad (5)$$

where h = 1, 2, 3 is the harmonic order, and i_{sr} and i_{sh} are the terminal currents of series and shunt VSIs, respectively. Con sidering the load current magnitude as the base and angle of the fundamental PCC voltage as the reference angle, transformer turns ratio n_t as unity, the series VSI current i_{sr} is 1 p.u. as shown in the first part of (5). The shunt VSI current i_{sh} consists of fundamental reactive and harmonic portion of load current. In the second part of (5), cosθL denotes the fundamental active component of load current, whereas *I*1*K* accounts for the additional fundamental active component required to maintain the dc-link voltage. During steady state, *I*1*K* represents the loss component of the UPQC system, and during sag condition, it also contains the active power component to achieve the overall power balance [7]. For simplicity, neglecting the inverter losses and defining the sag depth as $k = 1 - VL$. The current *I*1K can be expressed as be expressed as

$$I_{1K} = \left\{ \begin{array}{ll} 0, & \text{if} \quad k = 0 \\ \left(\frac{1}{1-k}\right)\cos\theta_L, & \text{if} \quad 0 \le k \le 1 \end{array} \right\}. \quad (6)$$

From (6), it is clear that *I*1*K* is a function of the load power factor and sag depth during off nominal conditions. Furthermore, it can be observed from (5*)* that *i*sr and *i*sh have different magnitudes and phase angles.

A. Switch Rating of the Back-to-Back UPQC

Using the derivations given in [22], the switch current for the back-to-back UPQC of Fig. 1 can be expressed as

$$\left.\begin{aligned} i_{SA_1} &= \textstyle\sum_{\sigma=1\to fsw} \left\{2\left(k_1\right)\left(T - T_1\right) i_{\mathrm{sh}}\right\}_\sigma \\ i_{SA_1'} &= \textstyle\sum_{\sigma=1\to fsw} \left\{2\left(k_2\right)\left(T_2\right) i_{\mathrm{sr}}\right\}_\sigma \\ k_1 &= \begin{cases} 1, & i_{\mathrm{sh}} \le 0 \\ 0, & i_{\mathrm{sh}} > 0 \end{cases} \quad k_2 = \begin{cases} 1, & i_{\mathrm{sr}} \le 0 \\ 0, & i_{\mathrm{sr}} > 0 \end{cases} \end{aligned}\right\} \quad (7)$$

where *iSA*1 and *iSA*_1 are phase *A* switch currents of shunt and series VSIs, respectively. *T* is the half switching period of the carrier waveform. *T*1 is the time interval during which the amplitude of carrier is higher than the modulating signal *SA*1 amplitude. *T*2 is the time interval during which the amplitude of modulating signal *SA*1 is higher than the carrier. *k*1 and *k*2 are symbolic variables governing the unidirectional current through *SA*1 and *SA*1 . Based on (7), the maximum current rating of each switch in series VSI is $1\angle\theta L$ (p.u) and shunt VSI is $(1\angle\theta L - 1\cos\theta L) + I1K$ (p.u). The

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e-ISSN: 2348-6848
p-ISSN: 2348-795X
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voltage rating of each switch in the 12-switch converter is the same as the dc-link voltage. Considering the nominal *rms* load voltage (1 p.u.) as base, the dc-link voltage would be 2√2 (p.u).

B. Switch Rating of the Nine-Switch UPQC

In the nine-switch UPQC topology of Fig. 2, the switch current can be expressed as follows [22], [23]: Based on (8) and the derivation in [23], the maximum current handled by three upper switches of the shunt VSI *{SA*1, *SB*1, *SC*1*}* and three lower switches of the series VSI *{SA*2, *SB*2, *SC*2*}* is (2∠*θL* − cos*θL*) + *I*1*K* (p.u.).

The current rating of the shared set of switches will bemax of (ish, isr). The voltage rating of all the switches is 2√2 (p.u.) similar to the 12-switch UPQC. Further explanation on nine-switch converter rating and loss analysis can be found in [22] and [23].

$$\left.\begin{aligned} i_{SA_1} &= \sum_{\sigma=1\to fsw}\left\{\begin{matrix} 2(k_1)(T-T_1-T_2)\,i_{\rm sh} \\ +(k_3)\,T_2\,(i_{\rm sh}+i_{\rm sr}) \end{matrix}\right\}_\sigma \\ i_{SA_{12}} &= \sum_{\sigma=1\to fsw}\left\{\begin{matrix} 2(1-k_1)(T_1)\,i_{\rm sh} \\ +(k_2)\,T_2 i_{\rm sr} \end{matrix}\right\}_\sigma \\ i_{SA_2} &= \sum_{\sigma=1\to fsw}\left\{\begin{matrix} 2(1-k_2)(T-T_1-T_2)\,i_{\rm sr} \\ +(1-k_3)\,T_1\,(i_{\rm sh}+i_{\rm sr}) \end{matrix}\right\}_\sigma \\ k_1 &= \begin{cases} 1, i_{\rm sh}\le 0 \\ 0, i_{\rm sh}>0 \end{cases}, \quad k_2 = \begin{cases} 1, & i_{\rm sr}\le 0 \\ 0, & i_{\rm sr}>0 \end{cases}, \\ k_3 &= \begin{cases} 1, & i_{\rm sh}+i_{\rm sr}\le 0 \\ 0, & i_{\rm sh}+i_{\rm sr}>0 \end{cases} \end{aligned}\right\}. \tag{8}$$

C. Switch Rating of the Proposed Ten-Switch UPQC

The instantaneous current for the shared set of witches SC1and SC2 in the proposed ten-switch UPQC of Fig. 3 can be expressed as follows:

$$\left.\begin{aligned} i_{SC_1} &= \sum_{\sigma=1\to fsw}\{2(k_1)(T_1)\,i_{\rm sh}\}_\sigma \\ i_{SC_2} &= \sum_{\sigma=1\to fsw}\{2(k_2)(T_2)\,i_{\rm sr}\}_\sigma \\ k_1 &= \begin{cases} 1, & i_{\rm sh}\ge 0 \\ 0, & i_{\rm sh}<0 \end{cases} \quad k_2 = \begin{cases} 1, & i_{\rm sr}\le 0 \\ 0, & i_{\rm sr}>0 \end{cases} \end{aligned}\right\}. \tag{9}$$

The current rating of the above two shared set of switches will be max of (ish, isr). The remaining four shunt VSI switch currents and four series

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e-ISSN: 2348-6848
p-ISSN: 2348-795X
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VSI currents are identical to that of the 12-switch shunt and series VSIs, respectively. Similar to nine switch topology, the voltage rating of all the switches is $2\sqrt{2}$ *p.u.*

TABLE III
PER UNIT COMPONENT RATING OF SEMICONDUCTORS AND OVERALL VA RATING FOR VARIOUS UPQC TOPOLOGIES

UPQC TOPOLOGY	No of switches	Maximum Switch Voltage Rating	Maximum Switch Current Rating: Dedicated Shunt VSI switches	Maximum Switch Current Rating: Dedicated Series VSI switches	Maximum Switch Current Rating: Shared switches	Overall UPQC VA Rating
Twelve-switch	12	$2\sqrt{2}$	$(1\angle\theta_L - \cos\theta_L) + I_{1K}$	$1\angle\theta_L$	–	$\boldsymbol{VA} = 6\boldsymbol{X}$ $X = 2\sqrt{2}\,((2\angle\theta_L - \cos\theta_L) + I_{1K})$
Nine-switch	9	$2\sqrt{2}$	$(2\angle\theta_L - \cos\theta_L) + I_{1K}$	$(2\angle\theta_L - \cos\theta_L) + I_{1K}$	$\max(i_{sh}, i_{sr})$	$\boldsymbol{VA} = 6\boldsymbol{X} + 3\boldsymbol{Y}$ $X = 2\sqrt{2}\,((2\angle\theta_L - \cos\theta_L) + I_{1K})$ $Y = 2\sqrt{2}\,(\max(i_{sh}, i_{sr}))$
Proposed Ten-switch	10	$2\sqrt{2}$	$(1\angle\theta_L - \cos\theta_L) + I_{1K}$	$1\angle\theta_L$	$\max(i_{sh}, i_{sr})$	$\boldsymbol{VA} = 4\boldsymbol{X} + 2\boldsymbol{Y}$ $X = 2\sqrt{2}\,((2\angle\theta_L - \cos\theta_L) + I_{1K})$ $Y = 2\sqrt{2}\,(\max(i_{sh}, i_{sr}))$

TABLE IV
PER UNIT VA LOADING OF UPQC FOR VARIOUS SAG DEPTHS

SAG DEPTH / UPQC TOPOLOGY	Normal conditions			0.2			0.4			0.6		
	X	Y	total	X	Y	total	X	Y	total	X	Y	total
Twelve-switch ($VA = 6X$)	3.74	-	22.45	6.19	-	37.16	7.12	-	42.75	9.03	-	54.17
Nine-switch UPQC ($VA = 6X + 3Y$)	3.74	2.8	30.9	6.19	5.68	54.1	7.12	6.68	62.76	9.03	8.69	80.23
Proposed Ten-switch ($VA = 4X + 2Y$)	**3.74**	**2.8**	**20.62**	**6.19**	**5.68**	**36.2**	**7.12**	**6.68**	**41.84**	**9.03**	**8.69**	**53.48**

D. Comparative Analysis

Using the aforementioned expressions for the currents and dclink voltage requirements, a comparative switch rating analysis is conducted for the three UPQC topologies. Table III provides a summary of the comparison. It can be clearly seen that the total VA rating of the nine-switch UPQC is higher than 12-switch topology by a factor of *3Y*. Since the maximum value of *Y* is always less than *X* [i.e., max (*i*sh, *i*sr)< (*i*sh + *i*sr)], the total VA rating of the proposed UPQC topology will always be lower than the 12-switch topology. For a better illustration, an analytical comparison of VA

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e-ISSN: 2348-6848
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loading for the three UPQC topologies is conducted and given in Table IV. The sag depths of 0.2, 0.4, and 0.6 are considered with a linear inductive load of $1\angle -30^\circ$. It can be seen from Table IV that among all three topologies, the nine-switch topology requires highest VA loading, whereas the proposed topology performs the same tasks with the least VA loading of the UPQC system.

For example, for a sag depth of 0.6 p.u., it can be observed that compared with the 12-switch topology, the proposed topology, in addition to saving of two semiconductor switches, requires 2% less VA, whereas the nine-switch topology needs at least 60% higher VA loading.

V. MODULATION SCHEME FOR THE TEN-SWITCH UPQC

Fig. 5 shows the developed modulation scheme to generate gate pulses for the proposed ten-switch UPQC topology. It involves dual-stage zero-sequence injection in the modulating references. The inputs to the modulator block are three reference signals each from the shunt and series VSI control blocks (further explained in Section VI). The developed modulation technique has two stages that are explained below. In the first stage, to enhance the dc bus utilization, the third-harmonic injection is carried out. Let $V^*_{\mathrm{sh}a,b,c}$ and $V^*_{\mathrm{sr}a,b,c}$ be the reference signals determined by the shunt and series VSI control blocks, respectively. These signals can be represented as

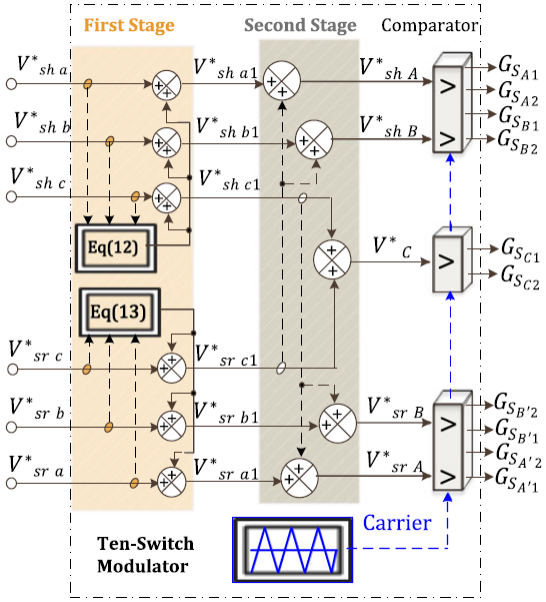

Fig. 5. Modulation scheme for the proposed ten-switch UPQC system.

$$\left.\begin{aligned} V^*_{\mathrm{sh}-a} &= M_{\mathrm{sh}}\cos\left(w_{\mathrm{sh}}t+\emptyset_{\mathrm{sh}}\right)\\ V^*_{\mathrm{sh}-b} &= M_{\mathrm{sh}}\cos\left(w_{\mathrm{sh}}t-120^\circ+\emptyset_{\mathrm{sh}}\right)\\ V^*_{\mathrm{sh}-c} &= M_{\mathrm{sh}}\cos\left(w_{\mathrm{sh}}t-240^\circ+\emptyset_{\mathrm{sh}}\right)\end{aligned}\right\} \quad (10)$$

$$\left.\begin{aligned} V^*_{\mathrm{sr}-a} &= M_{\mathrm{sr}}\cos\left(w_{\mathrm{sr}}t+\emptyset_{\mathrm{sr}}\right)\\ V^*_{\mathrm{sr}-b} &= M_{\mathrm{sr}}\cos\left(w_{\mathrm{sr}}t-120^\circ+\emptyset_{\mathrm{sr}}\right)\\ V^*_{\mathrm{sr}-c} &= M_{\mathrm{sr}}\cos\left(w_{\mathrm{sr}}t-240^\circ+\emptyset_{\mathrm{sr}}\right)\end{aligned}\right\} \quad (11)$$

where Msh, $w$sh , and $\varnothing$sh are the modulation ratio, angular frequency, and phase angle of the

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e-ISSN: 2348-6848
p-ISSN: 2348-795X
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shunt VSI.*M*sr , *w*sr , and ∅sr are the corresponding values for the series VSI, respectively. Using the third-harmonic injection method [11], the zero-sequence signal can be obtained as

$$V_{\text{no-sh}} = -0.5 \cdot \left[\text{Max}\left(V^*_{\text{sh}a,b,c}\right) + \text{Min}\left(V^*_{\text{sh}a,b,c}\right)\right] \quad (12)$$

$$V_{\text{no-sr}} = -0.5 \cdot \left[\text{Max}\left(V^*_{\text{sr}a,b,c}\right) + \text{Min}\left(V^*_{\text{sr}a,b,c}\right)\right] \quad (13)$$

and

$$V^*_{\text{sh}-i1} = V^*_{\text{sh}-i} + V_{\text{no-sh}} \quad (14)$$

$$V^*_{\text{sr}-i1} = V^*_{\text{sr}-i} + V_{\text{no-sr}} \quad (15)$$

where $V^*\text{sh}-i$ and $V^*\text{sr}-i$ (i = a, b, c) represent the three modified sinusoidal reference signals for shunt and series VSIs, respectively. In the second stage, five modulating signals for each leg, from the six aforementioned references, are generated. The series VSI reference for the shared phase *"C"* is added to the three modified shunt VSI references of (14). Similarly, the shunt VSI reference for the shared phase *"C"* is added to the three modified series

VSI references of (15). The resulting signals are expressed as

$$\left.\begin{aligned} V^*_{\text{sr}-A} &= V^*_{\text{sr}-a1} + V^*_{\text{sh}-c1} \\ V^*_{\text{sr}-B} &= V^*_{\text{sr}-b1} + V^*_{\text{sh}-c1} \\ V^*_{C} &= V^*_{\text{sr}-c1} + V^*_{\text{sh}-c1} \\ V^*_{\text{sh}-A} &= V^*_{\text{sh}-a1} + V^*_{\text{sr}-c1} \\ V^*_{\text{sh}-B} &= V^*_{\text{sh}-b1} + V^*_{\text{sr}-c1} \end{aligned}\right\}. \quad (16)$$

In (16), $V^*\text{sr}-c1$ is added to $V^*\text{sh}-a1$, $V^*\text{sh}-b1$, $V^*\text{sh}-c1$, and $V^*\text{sh}-c1$is added to $V^*\text{sr}-a1$, $V^*\text{sr}-b1$, and $V^*\text{sr}-c1$. This addition does not affect the reference modulation signals of shunt and series VSIs as the added signals $V^*\text{sr}-c1$ and $V^*\text{sh}-c1$ only appear as zero-sequence components and cancel out in line-to-line voltages at the ac terminals of shunt and series VSIs, respectively. Therefore, five modulating signals are generated out of six reference signals at the output of the second stage as shown in Fig. 5. The comparators then generate the required gate signals for the ten switches.

To illustrate the performance of the proposed ten-switch topology, a scenario is considered where linear *RL* Load is connected to a distorted supply voltage having THD ⩽ 5% and the fundamental voltage magnitude of 1 p. u. In this case, the shunt VSI requires the maximum dc-link voltage for load reactive power compensation. This infers that the peak magnitudes of the shunt reference modulation indices ($V^*\text{sh}-ABC$) in (16)

would be very close to unity which is given in Fig. 6(a). The corresponding output voltages at the shunt VSI terminal are shown in Fig. 6(c).

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e-ISSN: 2348-6848
p-ISSN: 2348-795X
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However, as shown in Fig. 6(b), the reference modulation indices for series VSI (V^*_{sr-ABC}) have peak magnitudes of approximately unity due to the addition of common phase "*C*" modulation index in stage 2. Nevertheless, the effective contribution of these reference signals toward the injected voltage will correspond to only a small voltage as shown in Fig. 6(d) consisting of the voltage required to compensate the harmonics in the PCC voltage. This is due to the fact thatthe added zero-sequence signals effectively cancel out in the injected line–line voltages.

When there is a drop in the PCC voltage, the peak amplitude of the voltage at shunt VSI terminals decreases as shown in Fig. 6(g). To compensate the sag, the output voltage amplitude of the series VSI increases. Fig. 6(f) and (h) reflects the transition in series VSI reference and output voltage during sag condition.

VI. CONTROL SCHEME FOR THE PROPOSED TEN-SWITCH UPQC

A. Control for Shunt VSI

The task of the shunt VSI is to compensate the reactive and harmonic components of load current and regulate the dc-link voltage during normal and sag conditions. To realize these objectives, the control scheme is shown in Fig. 7. The measured load current $iLabc$ is converted to the synchronous reference frame quantitates iLd and iLq , which are given as

$iLd = .iLd + \tilde{}iLd$

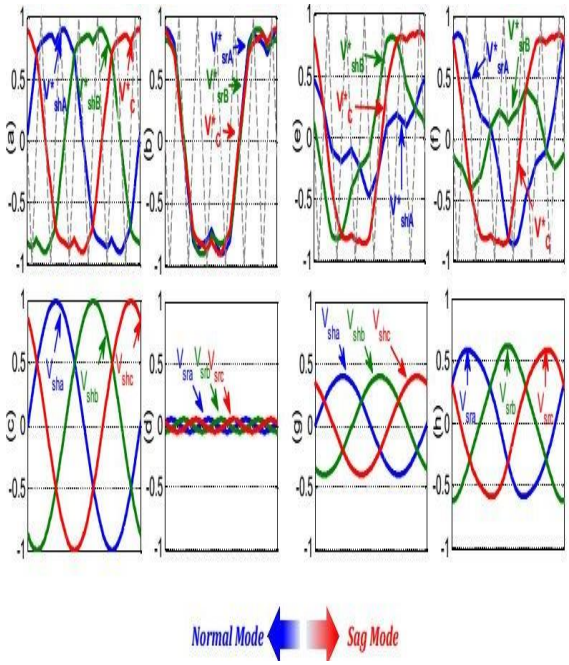

Fig. 6 Representation of modulation indexes and output voltages after second stage for (a),(c) shunt VSI during normal mode (b),(d) series VSI during normal mode (e),(g) shunt VSI during sag mode and (f),(h) series VSI during sag mode.

International Journal of Research
Available at https://edupediapublications.org/journals
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p-ISSN: 2348-795X
Volume 05 Issue 19
August 2018

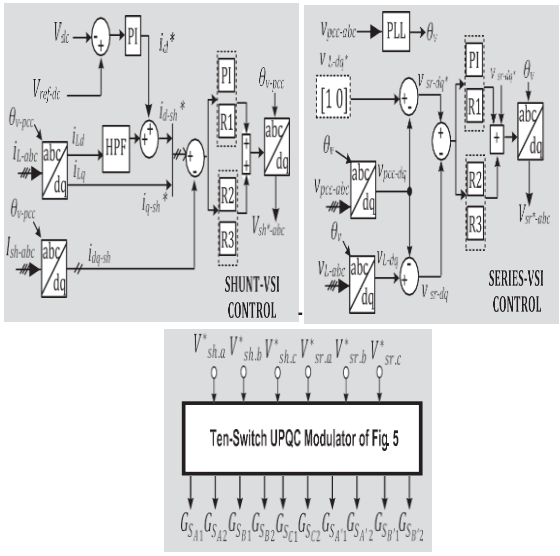

Fig. 7. Detailed control block diagram for the proposed ten-switch UPQC control for series VSI

$$i_{Lq} = \bar{i}_{Lq} + \tilde{i}_{Lq} \quad (17)$$

where. iLd and. iLq correspond to the fundamental active and reactive components of load current, respectively. iLd and iLq reflect the harmonic components of iL . The reference current of the shunt VSI can be expressed as

$$i_{ref-sh} = \tilde{i}_{Ld} + i_{Lq} + i_{Loss}$$

where $\tilde{i}_{Ld}$ is obtained by passing i_{Ld} through a high-pass filter. i_{Loss} corresponds to the active component of the source current required to maintain the dc-link voltage at rated value .i_{ref-sh} is compared with actual shunt current i_{sh} in the synchronous transformed back to the stationary reference frame giving V^*_{sh} a, b, c constituting the reference modulating signals for the shunt VSI.

The objective of the series VSI is to maintain the rated sinusoidal voltage at load terminals regardless of the voltage variation at the PCC. The overall series VSI control block is shown in Fig. 7.

TABLE V
UPQC SYSTEM DATA FOR EXPERIMENTAL STUDY

Programmable voltage source	Supply voltage: 175 $V_{L-L\,peak}$, 50 Hz Source Impedance: $R_g = 0.047\Omega$ and $L_g = 160\ \mu$H
UPQC	DC-link capacitors, $C_{dc} = 1100\ \mu$F Reference dc-link voltage = 230 V Series filter, $L_{sr} = 2.5$ mH $C_{sr} = 15\ \mu$F Shunt filter, $L_{sh} = 5$ mH Series transformer = 240/240 V (1:1 ratio)
Load	Linear: $R = 27\Omega$ and $L = 50$ mH Nonlinear $R = 57\ \Omega$ and $L = 5$ mH Nominal Load voltage $V_{L-L\,peak} = 50$ V

The difference between the series VSI reference voltage($V^*_{sr-vsi-dq} = V^*_{L-dq}$ $- V_{pcc-dq}$) and actual voltage ($V_{sr-vsi-dq} = V_{L-dq} - V_{pcc-dq}$) is processed by a combination of PI and resonant controllers in the synchronous reference frame. For sag detection, the absolute error between PCC reference voltage

(18)

(1 p.u.) and the actual PCC voltage magnitude (p.u.) in the synchronous reference frame is calculated as follows:

$$V_{\text{error}} = \left|1 - \sqrt{V_{\text{pcc}-d}^2 + V_{\text{pcc}-q}^2}\right|. \qquad (19)$$

The controller continuously monitors V_{error}, and as soon as it exceeds the threshold of zero p.u., sag is detected. Although $V^*_{\text{sr}-\text{vsi}-dq}$ can be directly used to control the series VSI in open loop by converting it into the stationary reference frame, however it will not be able to compensate the drop across VSI switches, interfacing filter and series transformer. It is therefore added as a feed forward signal to the output of PI to compensate for system losses. The resulting signal is converted into the stationary frame giving $V^*_{\text{sr}-a,\,b,\,c}$, which is the reference modulating signal for series VSI.

VII RESULT

To validate the performance of the proposed ten-switch UPQC, an experimental prototype is developed. A digital signal processor, *dSPACE DS1103,* is used to control the shunt and series inverters of the ten-switch UPQC. The developed algo- rithm requires a sampling time of 50 μs to execute the code on *dSPACE DS1103*. Both inverters operate at a switching fre- quency of 10 kHz. To emulate the sag and harmonic distortion in the grid voltage, a three-phase programmable source is used. The experimental system parameters are listed in Table V. Note that in all the experimental results, the PCC and load voltages are shown as line-to-line voltages, whereas the series-injected voltages are shown as phase voltages across series transformer. Fig. 8 depicts the steady-state performance of the pro- posed ten-switch UPQC system considering a linear *RL* load (V_{pcc} = 1p.u). Initially, the shunt VSI is maintaining the dc- link voltage by drawing a small current [see Fig. 8(c)], whereas the load reactive power is supplied by the grid. As seen from Fig. 8(e), the grid current lags the grid voltage by 37°. The reac- tive compensation starts at time t = T. The shunt VSI injects the necessary current causing the grid to supply only the load active power [i.e., grid current being in-phase with the grid voltage as shown in Fig. 8(e)]. On the same system, a sudden sag condition is imposed. An unbalance voltage sag is introduced in the grid voltage as shown in Fig. 9(a). It can be seen from Fig. 9 that the proposed ten switch UPQC effectively maintains the dc link as well as the load voltage at nominal values [see Fig. 9(b) and (c)]. The series controller injects the missing component in-phase with the positive-sequence voltage and cancels the negative-sequence component of PCC voltage.

International Journal of Research
Available at https://edupediapublications.org/journals
e-ISSN: 2348-6848
p-ISSN: 2348-795X
Volume 05 Issue 19
August 2018

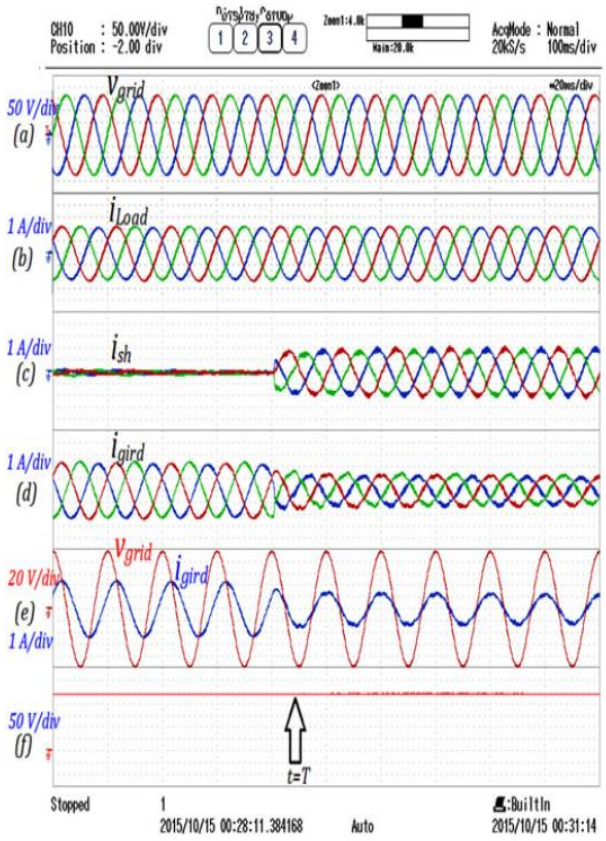

Fig. 8. Experimental result: power factor correction during steady-state condition.

Further, the performance of the proposed UPQC configuration is validated under the worst case scenario of maximum three-phase balanced voltage sag depth of 40% with only nonlinear load (diode bridge rectifier with current THD of 28%) connected to the system. As shown in Fig. 10(c), the load voltage are maintained at rated value in this case as well. Additionally, the shunt VSI compensates the harmonics in the load current and maintains the dc-link voltage at reference value. The source current THD is improved from 28% to 1.8%.Fig. 11 depicts the performance of the proposed ten-switch

UPQC when the PCC voltage and load current are distorted. A combination of linear (*RL*) and nonlinear load is considered with the combined load current THD of 18%. The fifth- and seventh harmonic voltages are added in the grid voltage to achieve a THD of 10%. The series part effectively mitigates the harmonics in the grid voltage. The improved load voltage profile can be noticed from Fig. 11(d), wherein the THD is reduced to 3%. Simultaneously,

the shunt controller effectively compensates the load current harmonics achieving sinusoidal grid currents with the THD of 2.1%. Thus, the above experimental study verifies the feasibility of the proposed ten-switch UPQC topology for practical applications to improve the power quality.

VII CONCLUSION

To overcome the limitations of nine-switch-based reduced switch power conditioner, this paper proposes a new structure of UPQC using ten semiconductor switches to reduce the switching losses. The important feature of the proposed topology is its capability of maintaining the same power quality enhancement with less number of switches and without increasing the switch VA rating. A

comparative study is conducted and the results instruct that the proposed ten switch topology can achieve the same power quality mitigation performance with the least VA loading of the UPQC system. The performance of the proposed topology has been validated experimentally under various operating conditions.

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