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Control and Management of Pc & Pq By Ssufcl In Der's

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ABSTRACT: *This paper proposes a framework to simultaneously optimize the Power Quality (PQ) and Protection Coordination (PC) levels in a DER-enabled microgrid with multiple connection modes. Introduction of DERs in a grid increases the fault currents. Different connection modes for these DERs lead to varying fault levels. Both phenomena jeopardize the PC. A Solid-State Unidirectional Fault Current Limiter (SSUFCL) is used as an interface between the microgrid as downstream and the utility as upstream networks, which limits the downstream contribution to the upstream fault currents for increasing the PC and PQ margins, while it is disabled in the case of downstream faults to improve the PQ. In this way the complete coordination between upstream and downstream networks will be achieved. To simultaneously optimize the PC and PQ, the time and current settings of the Over Current Relays (OCRs) and the characteristics of the SSUFCL are set. The optimization formulation of the protection coordination problem is extracted.Fuzzy optimization technique is used to make a compromise between PQ and PC after objectives' fuzzification. Genetic Algorithm (GA) is used to find the proper characteristics of the SSUFCL as well as the best settings of OCRs.*

Keywords: DERs, fault current limiter, microgrids, power quality, protection coordination.

I. INTRODUCTION

Based on the standards, DERs should be disconnected in the case of the main distribution system (upstream network) This paragraph of the first footnote will contain the date on which you submitted your work for review. It will also contain support information, including sponsor and financial support acknowledgment. Faults to reduce the microgrid (downstream network) share from the fault current. Though the PC is held, this will decrease the microgrid reliability due to unnecessary interruptions. In this situation limiting the fault current in the tie section may solve the problem. However,during a fault or starting a large motor load in the downstream network, limiting the upstream fault current leads to PC issues between upstream and downstream Over Current Relays (OCRs) and also PQ degradation due to the voltage reduction for the microgrid sensitive loads. Both problems can be alleviated using a Solid State.

Unidirectional Fault Current Limiter (SSUFCL) as proposed in the literature. In the present work a framework is proposed to simultaneously maximize the PC level and power quality(voltage sag mitigation is considered) and therefore, to maximize the benefit gained by installing a SSUFCL in the tie section. SSUFCLs was used to preserve the PC and/or to improve the PQ of a microgrid. In contrast, co-optimization of PC and PQ levels is proposed in this work. Here, different connection modes are considered for the microgrid DERs. The options available to optimize the PC and PQ levels are OCRs' time and current settings as well as the SSUFCL characteristics. The objectives are fuzzy field and a fuzzy multi objective optimization technique is used to solve the problem. Genetic Algorithm (GA) is used to determine the characteristics of the SSUFCL and the OCRs' settings Installation of some devices such as Fault Current Limiters (FCLs) with proper characteristics may solve the problem. The main idea is to avoid unnecessary power. interruptions to maximize the benefits of the DERs in both grid-connected and standalone modes. Other than restricting the magnitude of the fault currents, FCLs can limit the variation of the current level in different fault situations. As the number of DERs increases, one approach is optimal locating and parameter setting of additional FCLs in the connecting section of new DERs.

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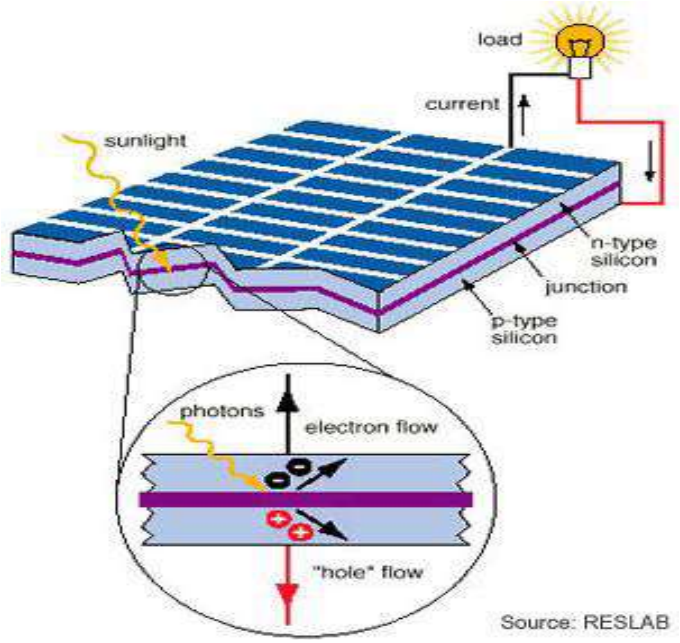

Fig. **Schematic diagram of a photovoltaic system**.

Distributed Generation (DG) is one of the new trends in power systems used to support the increased energy-demand. There is not a common accepted definition of DG as the concept involves many technologies and applications. Different countries use different notations like “embedded generation”, “dispersed generation” .

Type	Size
Micro distributed generation	1Watt < 5kW
Small distributed generation	5kW < 5 MW
Medium distributed generation	5 MW < 50MW
Large distributed generation	50MW < 300MW

Table : Size of the DG

The different DG technologies and impacts of distributed generation are introduced in this chapter; besides, islanded operation and the impact of DG on distribution feeder protection are presented.

TYPES OF DISTRIBUTED GENERATION

DG can be classified into two major groups, inverter based DG and rotating machine DG. Normally, inverters are used in DG systems after the generation process, as the generated voltage may be in DC or AC form, but it is required to be changed to the nominal voltage and frequency. Therefore, it has to be converted first to DC and then back to AC with the nominal parameters through the rectifier.

Some of the DG technologies, which are available at the present: photovoltaic systems, wind turbines, fuel cells, micro turbines, synchronous and induction generators are introduced.

PHOTOVOLTAIC SYSTEMS

A photovoltaic system, converts the light received from the sun into electric energy. In this system, semi conductive materials are used in the construction of solar cells, which transform the self contained energy of photons into electricity, when they are exposed to sun light. The cells are placed in an array that is either fixed or moving to keep tracking the sun in order to generate the maximum power. These systems are environmental friendly without any kind of emission, easy to use, with simple designs and it does not require any other fuel

than solar light. On the other hand, they need large spaces and the initial cost is high.

PV systems generate DC voltage then transferred to AC with the aid of inverters. There are two general designs that are typically used: with and without battery storages.

PROPOSED SYSTEM

Electric power systems are designed such that the impedances between generation sources and loads are relatively low. This configuration assists in maintenance of a stable, fixed system voltage in which the current fluctuates to accommodate system loads. The primary advantage of this arrangement is that loads are practically independent of each other, which allows the system to operate stably when loads change. However, a significant drawback of the low interconnection impedance is that large fault currents (5 to 20 times nominal) can develop during power system disturbances. In addition, the maximum fault current in a system tends to increase over time for a variety of reasons, including:

- Electric power demand increases (load growth) and subsequent increase in generation.
- Parallel conducting paths are added to accommodate load growth.
- Interconnections within the grid increase.
- Sources of distributed generation are added to an already complex system.

These devices have a fixed impedance so they introduce a continuous load, which reduces system efficiency and in some cases can impair system stability. Fault current limiters (FCLs) and fault current controllers (FCCs) with the capability of rapidly increasing their impedance, and thus limiting high fault currents are being developed. These devices have the promise of controlling fault currents to levels where conventional protection equipment can operate safely.

The power quality improvement depends widely on the current limiting capability of the SSUFCL and the quality of its one way operation as well as its operation speed. According to in order to determine the fault direction in a short time, 3rd and 5th orders of instantaneous harmonic power passing through the SSUFCL are calculated. The fault direction is then determined based upon their signs. The current limiting capability of a SSUFCL depends on the impedance inserted during the upstream faults. A resonant type solid state FCL is shown in Fig. 2(a) gives the full specifications of the device. During normal conditions, L, downstream equivalent inductance (Ls) and C form a series resonant circuit.

As a fault occurs the voltage across the capacitor increases suddenly. As the result, the MOV operates and the gate cathode voltage of the short circuiting thyristor reaches a sufficient level to fire the thyristor. In this condition, T2 which is a saturate transformer will be saturated and the inductance viewed from the primary of this transformer falls to a value of a few nano henries, which does not affect the parallel resonant circuit.

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To achieve a fast turn on of the thyristor, T1 has a small magnetic core with a very low turn ratio.

The variable resistance R models the resistance of the parallel resonant circuit in series with a variable resistance designed for the better adjustmentIn such situation the impedance of the SSUFCL is found using . After segregation of the real and reactive components the maximum impedance condition can be found.

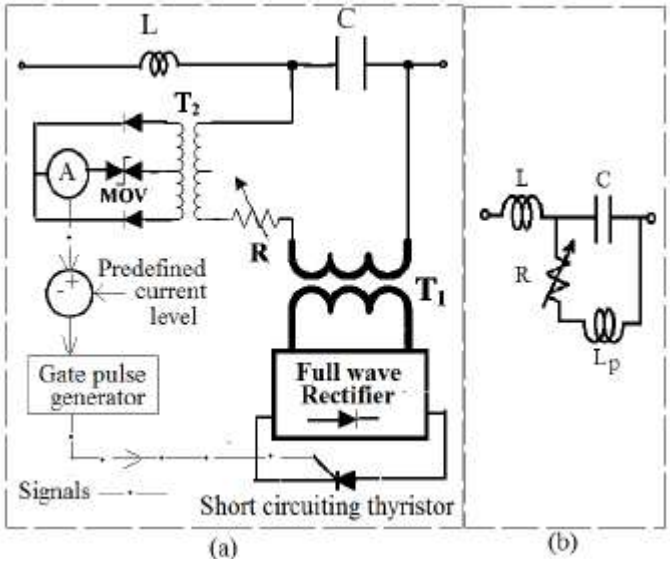

Fig : Resonant SSUFCL

A variety of FCL technologies that utilize unique and novel approaches for limiting the magnitude of fault currents are now in the prototype stage of development and, if successful, will soon be ready for grid deployment. The focus is on superconducting technologies, but several FCLs based on other technologies are described for completeness.

ADVANTAGES

- Limited fault current.
- Limited inrush current , even for capacitive loads.
- Repeated operations with reliability and with wear out.
- Reduced switching surges.
- Add the FCL when system is stable even though load changes.

SIMULATION RESULTS

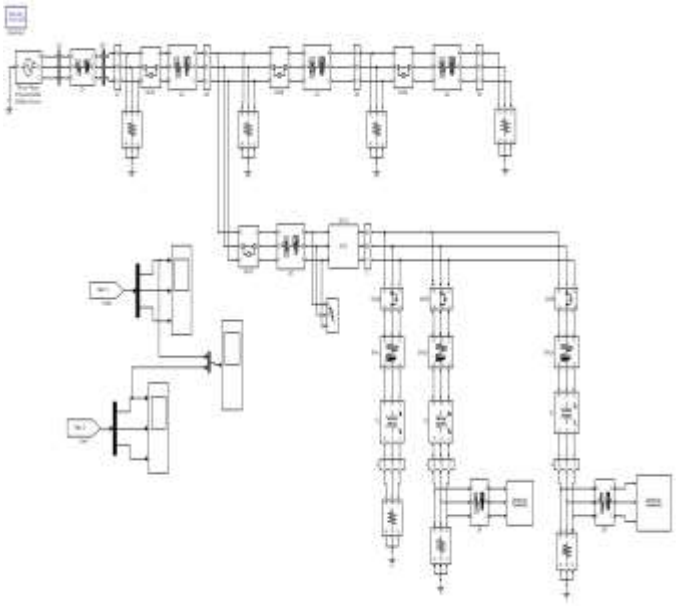

Fig: simulation diagram

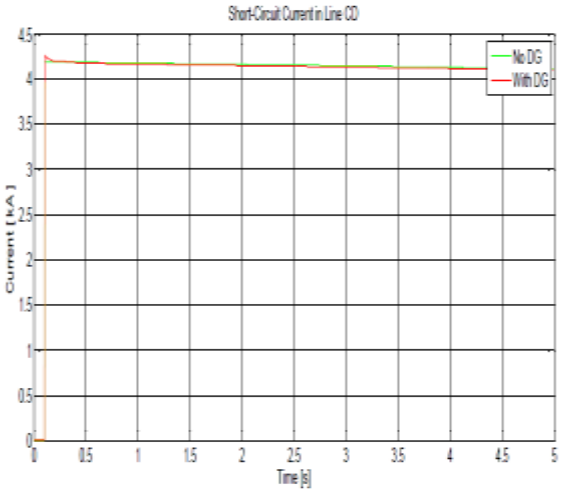

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Fig: Short circuit current in line CD with and without DG1

In Fig. the short circuit currents for a three phase fault in line CD, with and without DG1 connected to bus A, are shown. It can be seen from the Fig. that the short circuit current contribution from the DG1 is negligible and the short circuit levels remain within the allowable margin defined for the case with no DG connected in the system.

The IP of all relays is set 1.5 times maximum normal current. The current values are chosen from design study shown in Fig.

Instantaneous pick up times (T inst) are set as 50ms. The TD for each relay is calculated using equation and taking into account that clearing of fault takes around 70ms after the picking up of the relay and upstream relay reset time is well within 30ms. This gives enough time for R1 to pickup and to send the tripping signal to the correspondent circuit breaker to open and clear the fault before R2 picks up. Relays 2 and 3 are designed similarly. The pickup currents, time dial setting and the instantaneous pick up current for each relays R1, R2 and R3 are shown in.

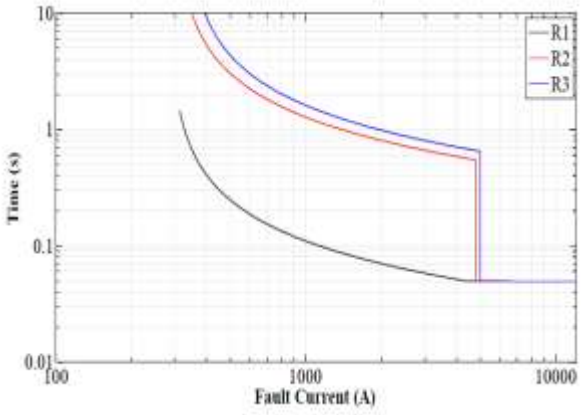

Fig: Time over-current plot of relays R1, R2 and R3.

Fig. shows the clearing time for a three phase fault in line CD after relay picks up and the corresponding opening trip signal is sent to the circuit breaker. The relay is clearing the fault within the setting time (50ms).

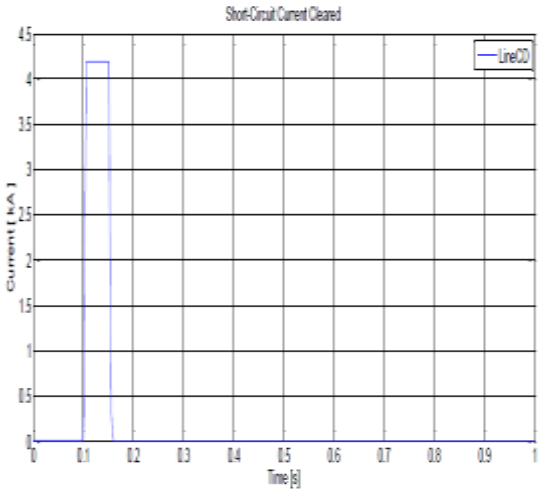

Fig: Fault cleared after the relay picks up time

In Fig. a single DG with the same characteristics as DG1 is connected to bus B. In this case, for a fault in section AB with relays characteristics same as in the previous case, relays 2 and 1 will not see the upstream fault current. Meanwhile relay 3 will sense the downstream fault

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current and if this current is higher than the set value, relay 3 operates and hence, DG2 and the downstream loads will form an island.

In Fig. the short circuit currents for a three phase fault in line CD when DG2 is connected to bus B and without DG, are shown. It can be seen that the short circuit current level in this line is roughly the same as in the previous case since DG2 is providing very little short circuit current to the fault.

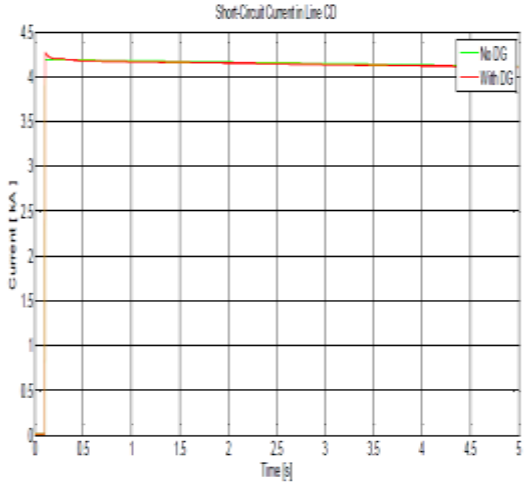

Fig: Short circuit current in line CD with DG2 connected

Relay settings are the same as in the previous case. If an island is formed, the protection scenario changes and therefore setting relays must adapt to the new limits. When the system is islanded the short circuit current seen by the relays is less compared to the case when the distribution system is connected to the transmission grid. As a proposed solution adaptive protection relays can be used. These relays are able to update the trip characteristics by detecting the operating states and the faulted section.

- Multiple DGs interconnected to radial systems .

DG2 and DG3 (same characteristics as DG2) connected at bus B and bus C, respectively. For a downstream fault from DG3 the coordination of relays is the same as in the previous case and selectivity between them will hold if the fault is lower than the permissible current limit. For a fault in line BC, relay 2 operates before relay 3 and for a fault in line AB relay 3 should trip while the loads, DG2 and DG3 will form an island. The proper coordination of the relays depends on the amount of fault current, which is increased when DG is connected to the system and should not exceed the predetermined current set range of the relays, if not, coordination may be lost. It can be said that with a downstream fault of DG, selectivity and coordination holds and sensitivity is improved as long as the fault current does not exceed the permissible limits.

In Fig. the short circuit current for a three phase fault in line CD when DG2 and DG3 are connected to bus B and bus C and when they are not is shown. As in the two previous cases not appreciable difference between the short circuit current with and without DG is noticed. However, a slight decrease in the short circuit current when DG it is connected is noticeable in Fig.

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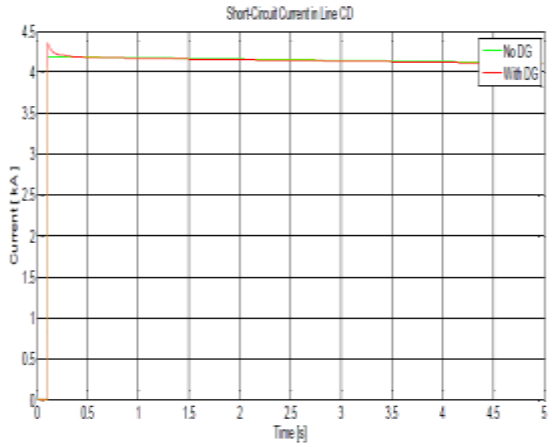
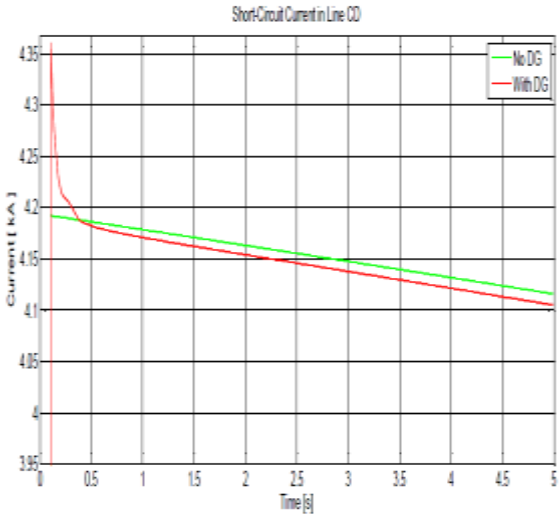


Fig: Short circuit current in line CD with DG2, DG3 connected and without DG

The decrease in the short circuit current level when DG is connected to the system is caused by an increase on the impedance seen by the fault. Before the DG is connected, the radial system has less impedance and therefore the current seen by the fault is higher. On the other hand, the connection of DG increases the impedance of the whole system in a proportion defined by the impedance provided by the DG technology, which in this case is wind turbines.



Relay settings are the same as the previous cases and it was observed that coordination between relays hold and the fault was cleared in the expected time as it is shown in Fig.

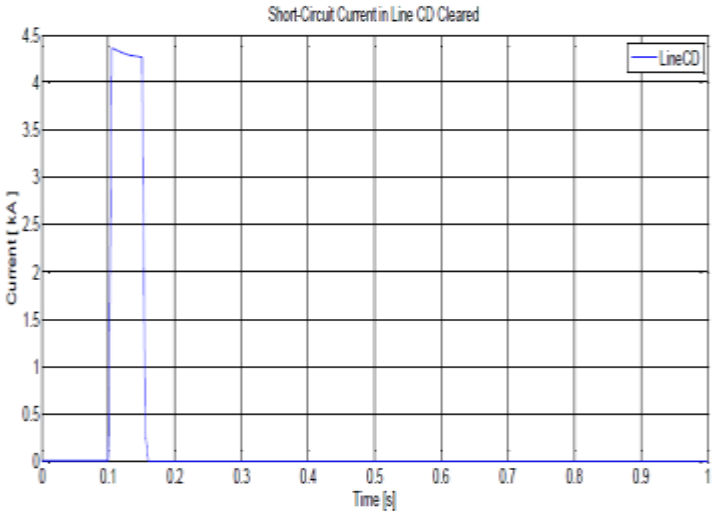


Fig: Clearing fault when DG2 and DG3 are connected to the system

As a conclusion it can be said that as long as the fault current does not exceed the permissible current limits, the presence of DG in a system may enhance the coordination between relays by increasing the fault current, but, on the other hand, the DG may also cause a decrease in fault current from the transmission system. Both situations are possible when DG is connected into a radial system and they need to be investigated for minimum tripping or coordination problems. Furthermore, relays operation may lead to islanding (if the DG technology can support the island, for example: synchronous generators), which also needs to be investigated in order to set the proper protection coordination.

VII. CONCLUSION

A framework was presented to solve the PC and PQ issues in a microgrid connected to the main distribution system.

A SSUFCL was used as the interface between the microgrid and the main system. In order to maximize the benefit gained by installing the SSUFCL the framework optimizes the OCRs settings as well as the SSUFCL parameters to co-optimize the PC and PQ in the microgrid. The results show that the proposed framework can effectively co-optimize the PC and PQ levels. The physical restrictions of the SSUFCL are taken into account. A complete formulation is proposed for PC optimization and is modified carefully to be solved using a heuristic optimization algorithm. The PC is restored in every connection mode in the microgrid after installing the DERs and the unnecessary interruptions are avoided to maximize the system reliability.

The voltage sag issue in the sensitive buses of the microgrid in the case of the upstream disturbances is mitigated without engaging into the resynchronization issues.

FUTURE SCOPE

This work can be further elongated by considering rescheduling of reactive power generation and its compensation utilizing UPQC. Secondly the work can additionally be elongated in bilateral transaction environment of deregulated power system. Further the performance of the perspicacious optimization technique like Particle Swarm optimization used predicated on evolutionary methods can be enhanced by optimizing its control parameter.

VIII. REFERENCES

[1] M. Ezzeddine, Kaczmarek, and R. Iftikhar, “Coordination of directional over current relays using a novel method to select their settings,” Proc.Inst. Elect. Eng., Gen., Transm., Distrib., vol. 5, no. 7, pp. 743–750,2011.

[2] H. J. Lee, G. T. Son, and J.W. Park, “Study on wind-turbine generator system sizing considering voltage regulation and over current relay coordination,” IEEE Trans. Power Syst., vol. 26, no. 3, pp. 1283–1293,Aug. 2011.

[3] E. M. Lightner and S. E. Widergren, “An orderly transition to a transformed electricity system,” IEEE Trans. on Smart Grid, vol. 1, no.1, pp. 3–10, Jun. 2010.

[4] D. S. Popovic and E. E. Boskov, “Advanced fault management as a part of smart grid solution,” in Proc. IET CIRED Seminar 2008: Smart Grids Distrib., Jun. 23–24, 2008, pp. 1–4.

[5] A. Molderink, V. Bakker, M. G. C. Bosman, J. L. Hurink, and G. J. M.Smit, “Management and

e-ISSN: 2348-6848
p-ISSN: 2348-795X
Volume 05 Issue 20
September 2018

control of domestic smart grid technology," IEEE Trans. Smart Grid, vol. 1, no. 2, pp. 109–119, Sep. 2010.

[6] IEEE Standard for Interconnecting Distributed Resources with Electric Power Systems, IEEE Std. 1547, 2003.

[7] T. Ghanbari, and E. Farjah, "Unidirectional fault current limiter: an efficient interface between the microgrid and main network," IEEEtrans. Power Syst., vol. 1, no. 1, pp. 1591-1598, May 2013.

[8]A. Pregelj, M. Begovic, A. Rohatgi, "Recloser allocation for improved reliability of DG-enhanced distribution networks," IEEE Trans. Power

Syst., vol. 21, no. 3, pp. 1442–1449, Aug. 2006.

[9] H. Laaksonen, D. Ishchenko and A. Oudalov, "Adaptive Protection andMicrogrid Control Design for Hailuoto Island," IEEE Trans. on Smart Grid, vol. 5, no. 3, pp. 1486-1493, May 2014.