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Light-Load Efficiency Power Conversion Scheme Using Bidirectional Buck Converter

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Abstract: High efficiency under a light-load condition is becoming important ,because power systems operate mostly under this condition. In the current social atmosphere promoting energy savings, high efficiency is valued for server power supplies in data centers to reduce power consumption. For this reason, many programs and regulations require high light-load efficiency. In this project, a new power conversion scheme considering paralleled modules is to be proposed. Under a very light-load condition, only a non-isolated buck converter in the secondary side of the remaining power supply provides the output power, which is different from the cold-redundant (CR) concept.Furthermore,in the proposed concept, the voltage source in the buck converter is maximized by using an additional voltage bus connecting between the snubber capacitors of each module. To achieve high power density, the buck converter is integrated with the rectifier circuits in the secondary side of the Phase shift full-bridge(PSFB) converter. The validity of the basic operational principles is confirmed with two 12V/750W by using MATLAB/ simulink software .The results will be demonstrated for the proposed converter.

Key words—Bidirectional, buck converter, integrated, light-load efficiency, paralleled, power conversion, server power supply.

I.INTODUCTION

IN the current social atmosphere promoting energy savings, high efficiency is valued for server power supplies in data centers to reduce power consumption. Especially, high efficiency under a light-load condition is becoming important, because power systems operate mostly under that condition. For this reason, many programs and regulations require high light-load efficiency. For example, the 80 PLUS performance specification requires power supplies in computers and servers to be high efficient To achieve Titanium certification, the efficiency must be satisfied mostly to be greater than 90% at 10 % load, as well as under a full-load condition. Furthermore, many manufacturers of computer, telecommunication, and network equipment require high light-load

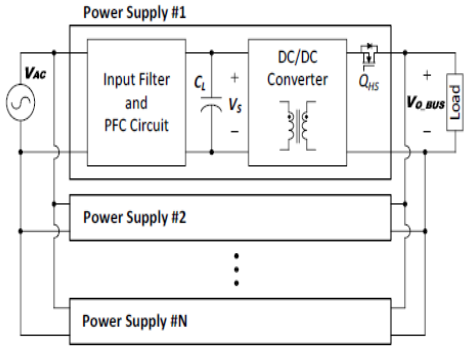

Fig. 1. General structure of a server power supply.

efficiency even below a 5% load condition, which exceeds the latest Energy Star specifications .This means that very light-load efficiency will become more important in the future.

Fig. 1 shows the general structure of a server power supply. The *N* power supplies are connected in parallel and provide the output power with an equally shared load current. This increases the power handling capability and the overall efficiency. Additionally, redundant power supplies are normally adopted in this structure. These enable the power to be supplied continuously even when an arbitrary power supply is turned off due to faults, which improves overall reliability . Each power supply has two power conversion stages. The first one is the input filter and the power-factor-correction (PFC) circuit, which creates low EMI, surge protection, and a high power factor. The PFC circuit, normally using a boost converter, converts the AC voltage to DC link voltage *VS* of about 400V. The second power conversion stage is the DC/DC power conversion circuits, which use an isolation transformer and regulate the output voltage at about 12V. A phase-shift full-bridge (PSFB) converter is generally used to meet the high step-down voltage, low output voltage and high output current. In DC/DC power conversion, many components, including many switches and magnetic components, are used, so it is very difficult to improve the overall efficiency, especially under a light-load condition, due to the switching and core losses. Meanwhile, hot-swap circuits using a switch *QHS* and load-share control circuits are additionally required to connect and drive the paralleled power supplies.

To improve the light-load efficiency in a PSFB converter, various research has been presented. Discontinuous conduction mode (DCM) operation reduces the operating duty ratio, which results in low core and switching losses. Also the conduction loss in the body diode of the synchronous rectifiers (SRs) is reduced by using AND-gated signals for SRs [5]. In [6], the gate driving voltage of power MOSFETs and the operating voltage of controller ICs are controlled according to the load condition. Below a certain load condition, the gate driving voltage is decreased so the gate driving loss and controller driving loss are decreased. In [7], a maximum duty point tracking method is applied. The link voltage is adjusted to keep the maximum duty ratio based on the link and output voltage, which reduce the circulating and switching losses. In [8], three-level converter was studied. The switches in that converter must conduct about twice the current as those in a two-level converter, but it has low switch voltage stress that is half the input voltage. Thus, a three-level converter has low switching loss which means higher light-load efficiency, but higher conduction loss which means lower heavy-load efficiency. In [9], the power converter operates according to the load power with maximum efficiency by changing the dc-link voltage and the switching method. According to the load condition, the switching mode of the PSFB converter is changed into the PWM and burst modes. Thus, the light-load efficiency is increased by minimizing the switching and circulating conduction losses. Another approach is to consider paralleled modules, not limited to a single module. The cold-redundant (CR) concept is proposed in [10]-[13]. Under a certain light-load condition, the DC/DC converter in the redundant power supply is turned off and enters standby mode, so the remaining modules provide the total output power, which eliminates the switching, core, and control losses in the

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DC/DC converter of the redundant power supply.

In this paper, a new power conversion scheme considering paralleled modules is proposed. Under a light-load condition, the redundant power supply enters standby mode as in the CR concept. However, under a very light-load condition, only a non-isolated buck converter in the secondary side of the remaining power supply provides the output power, which is different from the CR concept. Thus, the operating components and the related power losses are more minimized. Also, to achieve high power density, the buck converter is integrated with the rectifier circuits in the secondary side of the PSFB converter. Furthermore, in the proposed concept, the voltage source in the buck converter is maximized by using an additional voltage bus connecting between the snubber capacitors of each module.

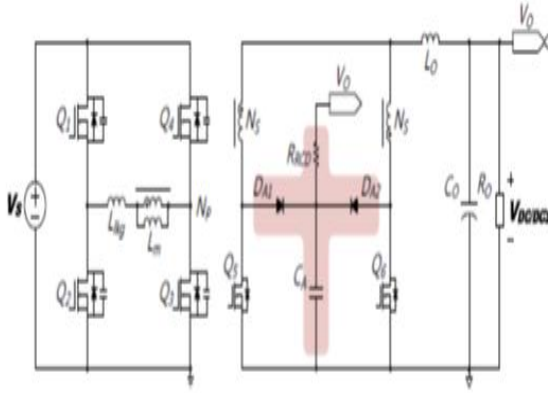

Fig. 2. Circuit diagram of a phase-shift full-bridge DC/DC converter.

II. PROPOSED CIRCUIT AND OPERATION

Fig. 2 shows the circuit diagram of a PSFB converter. PSFB converters are widely used in low-voltage, high-current and high-power applications due to its low output current stress achieved by using an output inductor (*LO*), which results in low overall conduction loss. Also, because the full-bridge inverter is controlled via phase-shifts, ZVS can easily be achieved by using transformer leakage inductance (*Llkg*). Another feature is the RCD snubber. To reduce the voltage stresses on the SRs and to be able to use low-voltage-rated switches, the snubber capacitor (*CA*) in the RCD snubber, indicated in red box in Fig. 2, clamps the voltages of the SRs and its energy is dissipated to the output voltage (*VO*) through *RRCD*. By adjusting *RRCD*, the voltage stresses on the SRs are controlled [14].

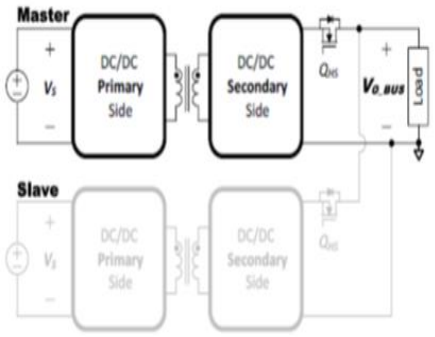

Fig. 3. CR concept under a light-load condition.

Fig. 3 shows the CR concept in two power supplies. For example, above a 20% load condition, the two power supplies have equal load currents, which is called the load share mode. On the other hand, below a 20% load condition, one power supply is turned off, and another power supply has the entire load current which provides high light-load efficiency. The turned-off power supply is called the slave, and the other is called the master. However, the overall efficiency is still low under a very light-load condition. For example, the efficiency at 1% load condition is about 50% in 12V / 750W output. Therefore, in this paper, to improve the overall efficiency under very light-load efficiency, a new power conversion scheme is

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proposed. In order to explain the proposed circuit and operation easily, this chapter is divided into three parts: 1) concept of proposed circuit, 2) implementation of proposed circuit, 3) operational principles of proposed circuit.

A.Concept of proposed circuit

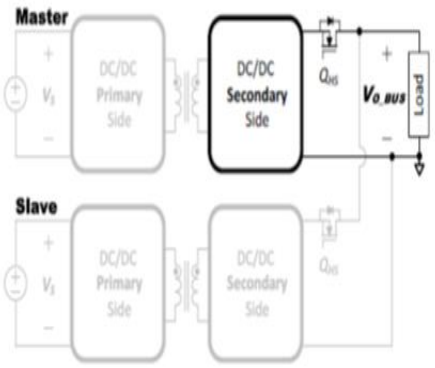

Fig. 4. Proposed circuit concept under a very light-load condition.

This part explains the concept of the proposed circuit. Under a light-load condition, the proposed circuit operates like the conventional CR concept, as shown in Fig. 3. On the other hand, under a very light-load condition, the primary-side circuits in the master are turned off, as shown in Fig. 4. Thus, only the secondary-side circuits in the master transfers power to the load,

III.IMPLEMENTATION OF PROPOSED CIRCUIT

In this part, the implementation of the proposed circuit is explained to realize the concept of the proposed circuit. Fig. 7 shows the proposed circuit employing the PSFB converter where *RRCD* in the RCD snubber is omitted to simplify the circuit diagram. Firstly, the voltage source (*VAUX*) is implemented by the snubber capacitor (*CA*). Generally, multi-layer ceramic capacitors (MLCCs) are used for *CA* because low capacitance and high power density are required. However, in the proposed circuit, aluminum electrolytic capacitors are employed to provide the power for the load with sufficiently large capacitance and stored energy. Moreover, by connecting the snubber capacitor and adding another voltage bus (*VAUX_BUS*), the energy of *VAUX* can be maximized in the

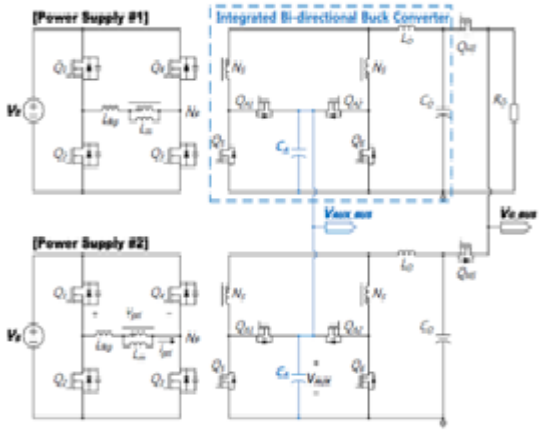

Fig 5. Circuit diagram of the proposed circuit

paralleled modules. Therefore, *VAUX* can be used as a new voltage source under a very light-load condition.

Secondly, the bidirectional converter is required to not only transfer power to the load but also charge *VAUX* effectively. Meanwhile, the bidirectional buck converter is widely used for non-isolation and bidirectional power flow due to its simple structure and high efficiency [15]-[18]. Thus, the bidirectional buck converter is applied to the proposed circuit for transferring power from *VAUX-BUS* to the load and charging *VAUX-BUS* from the slave. Fortunately, with small changes, the bidirectional buck converter can be easily integrated into the secondary-side circuit of the PSFB converter. By using the switches (*QA1* and *QA2*) instead of the diodes of the RCD snubber (*DA1* and *DA2*), two bidirectional buck converters with one inductor *LO* are integrated. The output inductor current *iLO*is equally divided into two bidirectional buck converters with the help of the transformer

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secondary windings (*NS*) which are coupled to each other with same turns. Therefore, the proposed concept can be implemented very effectively in converters which have a center-tap rectifier with SRs and an output inductor.

IV.OPERATIONAL PRINCIPLES OF PROPOSED CIRCUIT

In this part, the operational principles of the proposed circuit are explained by dividing operation mode into the charging mode and discharging mode. Fig. 8 shows the operating modes of the proposed circuit under a very light-load condition and Fig. 9 shows the key waveforms of the bidirectional buck converter. In these figures, the reference direction of *iLO*is expressed as the charging direction of *CA*. In addition, to simplify the analysis, it is assumed that the dead times between the gate signals are neglected.

1) Discharging mode

In the discharging mode, the slave is turned off, and only the bidirectional buck converter operates and transfers power from *VAUX-BUS* to the load by using the energy stored in *CA*, as shown in Fig. 8(a). Firstly, when *QA1* and *QA2* are turned on and *Q5* and *Q6* are turned off,

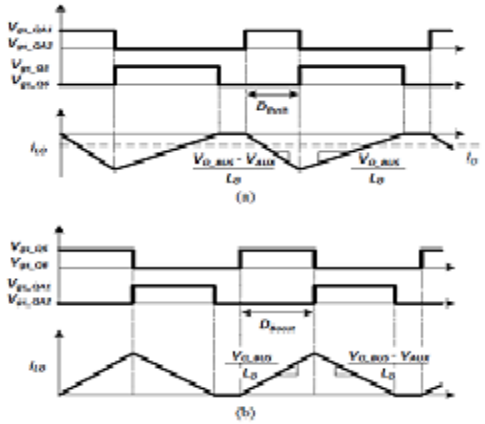

Fig. 6 Key waveforms of the bidirectional buck converter. (a) Discharging mode. (b) Charging mode.

*iLO*builds up with a slope of (*VO_BUS-VAUX*)/*LO*. After *QA1* and *QA2* are turned off and *Q5* and *Q6* are turned on, *iLO*decreases to zero with a slope of *VO_BUS*/*LO* as shown in Fig. (a).

2) Charging mode

In the charging mode, the primary-side of the master is still turned off but the slave is turned on. Thus, the slave transferspower to the load and charges *CA* by using the bidirectional buck converter with the boost.

V.DESIGN CONSIDERATIONS

To use the proposed circuit effectively, the design consideration of the bidirectional buck converter is required. Therefore, in this chapter, VAUX, CA, DBuck, and DBoostof the bidirectional buck converter are explained except for LO because LO is already designed by the PSFB converter.

VAUX

To obtain sufficient energy from CA under a very light-load condition, the voltage swing range of VAUX should be maximized. However, since VAUX is also used as the snubber voltage over a light-load condition, the range of VAUX should not affect the operation of the PSFB. Thus, in designing VAUX, the snubber voltage range of the PSFB operation should be considered. Firstly, VAUX_MIN is determined by the minimum snubber voltage, which is expressed as follows:

$$V_{AUX\_MIN} > 2V_{S\_MAX}\frac{N_S}{N_P}, \quad (1)$$

whereVS_MAX is the maximum link voltage, and NP and NS are the transformer primary and secondary turns, respectively. Thus, VAUX_MIN can be designed as 30V according

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to the design parameters of the PSFB converter, where VS_MAX=400V, NP=27, and NS=1. Secondly, VAUX_MAX is determined by considering the voltage stresses on SRs. In general, the PSFB converter providing 12V output uses 60V voltage-rated switches for SRs because SRs of the PSFB converter suffer from the additional voltage spike caused by the resonance between the leakage inductor of the transformer and junction capacitor of SRs, Therefore, with the 50% voltage margin, VAUX_MAX is designed as 40V to use 60V voltage-rated designed as 40V to use 60V voltage-rated switches.

TABLE I
COMPARISON OF CAPACITOR VOLUME

	Conventional	Proposed	
	Link capacitor	Link capacitor	C_A
Working voltage	450V	450V	50V
Capacitance	560μF	450μF	1mF
#	1	1	4
Size (Φ*mm)	35*45	30*45	12.5
Volume (liter)	43295	41621	

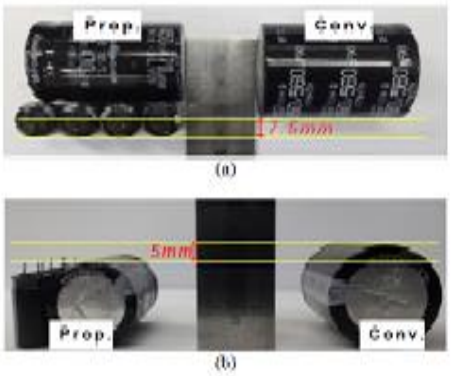

Fig 7 Overall capacitor size. (a) Side view. (b) Top view.

As a result, the range of VAUX is designed as 30-40V.

CA

As mentioned in Chapter II, aluminum electrolytic capacitors are used for CA to transfer power to the load with sufficient large capacitance. However, large size of aluminum electrolytic capacitor decreases the power density. Moreover, since the size of aluminum electrolytic capacitor can be more increased as the capacitance is increased, CA should be designed by considering the power density.

Meanwhile, the sever power supply has a special requirement called the hold-up time (TH), where VO_BUS stays within a regulated range by using the energy stored in the DC link capacitor (CL) after AC is lost. That means CL is inevitably large to provide power for the load without AC source. However, since VAUX can be used another voltage source during the hold-up time, CA can help the hold-up time to be extended. Conversely, CL can be designed to be smaller while maintaining the same TH. The relation between CL and CA is written as follows:

In practical circuits, the switching stress is much higher because of the parasitic inductance (L_p) and capacitance (C_p). C_p includes the output capacitance of the switch and stray capacitance due to PCB layout and mounting. L_p includes the parasitic inductance of the PCB route and MOSFET lead inductance. These parasitic inductances and capacitances from the power devices form a filter that resonates right after the turn-off transient, and therefore superimposes excessive voltage ringing to the devices as shown in Figure 3. To suppress the peak voltage, a typical RC snubber is applied across the switch as shown in Figure 4. The value of the resistor must be close to the impedance of the parasitic resonance which it is intended to damp. The snubber capacitance must be larger than the resonant circuit capacitance, but must be small enough in order to keep the power dissipation of the resistor to a minimum.

whereVS_MIN is the minimum link voltage, PO_REQ is the required output power for the hold-up time, η is the efficiency of the DC/DC

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converter, and CL_C and CL_P are the link capacitance in the conventional and proposed

TABLE II
COMPONENTS LIST

	Conventional	Proposed
Q_1, Q_2, Q_3, Q_4	IPP60R299	
Q_5, Q_6	BSC014N06NS	
D_{A1}, D_{A2} or Q_7, Q_8	ES1D	BSC014N06
C_L	560μF	470μF
C_A	100nF	1mF * 4
L_O	2μH	
N_P : N_S : N_A	27 : 1 : 1	
Controller	TMS320F28069	

$$T_H = \frac{C_{L\_C}\left(V_{S\_MAX}{}^2 - V_{S\_MIN}{}^2\right)}{2P_{O\_REQ}/\eta} = \frac{C_{L\_P}\left(V_{S\_MAX}{}^2 - V_{S\_MIN}{}^2\right) + C_A\left(V_{AUX\_MAX}{}^2 - V_{AUX\_MIN}{}^2\right)}{2P_{O\_REQ}/\eta} \quad (2)$$

converters, respectively. When VS_MAX=400V, VS_MIN=340V, and CL_C =560μF, from (2), CL_P and CA can be designed as 470μF and 1mF*4 by considering the size of CL_C and CL_P+CA. Table I shows the capacitor volume and Fig. 10 shows the overall capacitors size in the proposed and conventional converters. In summary, although the proposed circuit has a large CA, it has a smaller total capacitor volume because CA can help the size of DC link capacitor to be reduced.

DBuck and DBoost

The buck duty ratio (DBuck) is naturally determined by IO to regulate VO_BUS, which is expressed as follows:

$$D_{Buck} = \sqrt{\frac{8L_O I_O f_S}{V_{O\_BUS}\left[(V_{AUX}/V_{O\_BUS}-1)^2 - 1\right]}}, \quad (3)$$

Where fS is the switching frequency of the bidirectional buck converter.

Meanwhile, since the boost duty ratio (DBoost) decides the charging current (ICH), it relates to the charging time, which affects the overall all efficiency. The expected efficiency in the proposed circuit can be expressed as follows:

$$\eta_{Expect} = \frac{P_O}{\left(P_{Loss\_CH} + P_O\right)\frac{T_{CH}}{T_{Period}} + P_O\frac{T_{DISCH}}{T_{Period}}}, \quad (4)$$

wherePO is the output power, PLoss_CHis the power loss in the charging mode, TCH and TDISCH are the charging and discharging times, respectively, and TPeriodis the sum of TCH and TDISCH, as shown in Fig. 6. TDISCH is determined by the PO and power loss during the discharging time. From (4), to achieve high efficiency under a very light-load condition, TCH should be minimized because PLoss_CHis additionally caused during TCH.

However, the shorter TCH requires larger ICH and Dboost, which creates higher current stress on CA as well as conduction loss.

Thus, the maximum current stress of CA should be considered to decide DBoost.

VI. SIMULATION RESULTS

A.SIMULINK DIAGRAM OF PROPOSED CIRCUIT

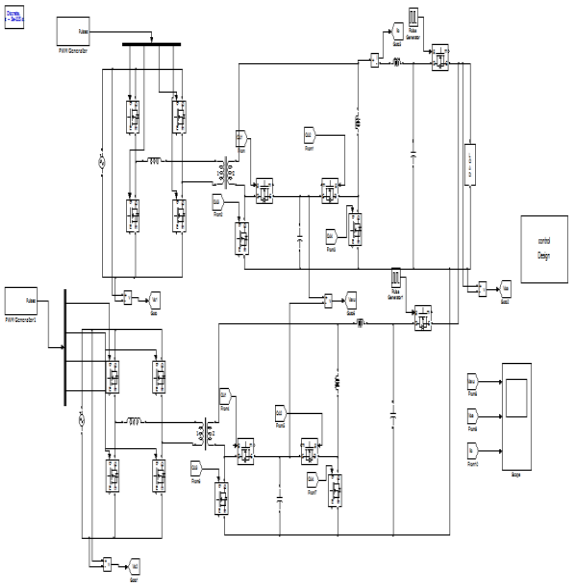

Fig 8(a) SIMULINK DIAGRAM OF PROPOSED CIRCUIT

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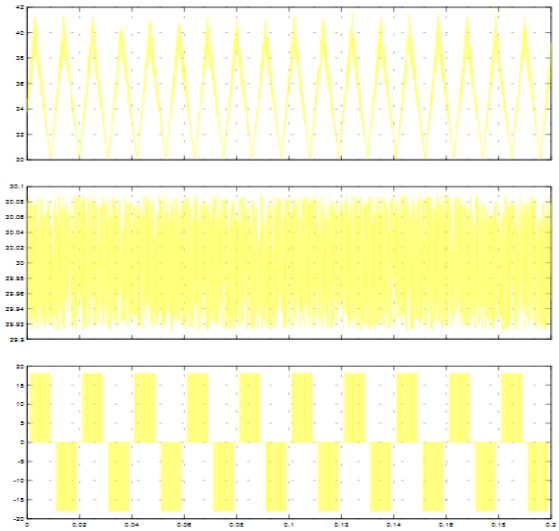

Fig 8(b) Out put

B.SIMULINK DIAGRAM OF DISCHARGING MODE

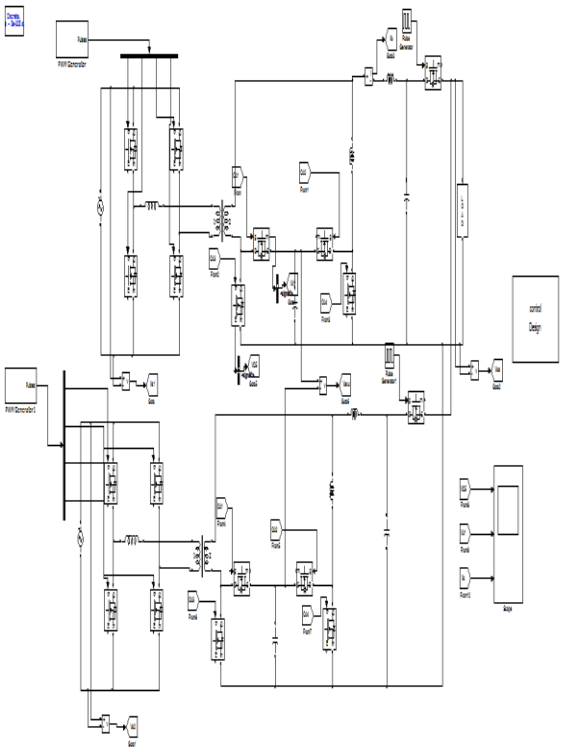

Fig 9(a)SIMULINK DIAGRAM OF DISCHARGING MODE

In the discharging mode, the slave is turned off, and only the bidirectional buck converter operates and transfers power from VAUX-BUS to the load by using the energy stored in CA, as shown in Fig. (a). Firstly, when QA1 and QA2 are turned on and Q5 and Q6 are turned off, iLObuilds up with a slope of (VO_BUS-VAUX)/LO.

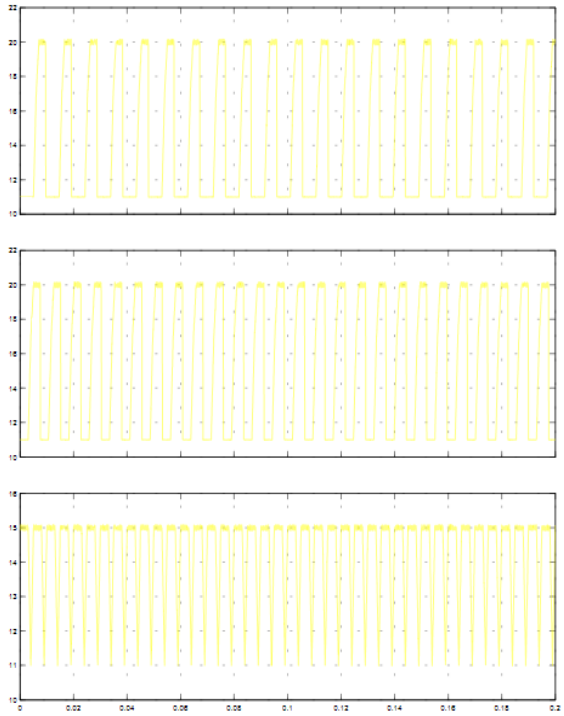

Fig 9(b) Out Put

After QA1 and QA2 are turned off and Q5 and Q6 are turned on, iLOdecreases to zero with a slope of VO_BUS/LO as shown in above Figure.

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C.SIMULINK DIAGRAM OF CHARGING MODE

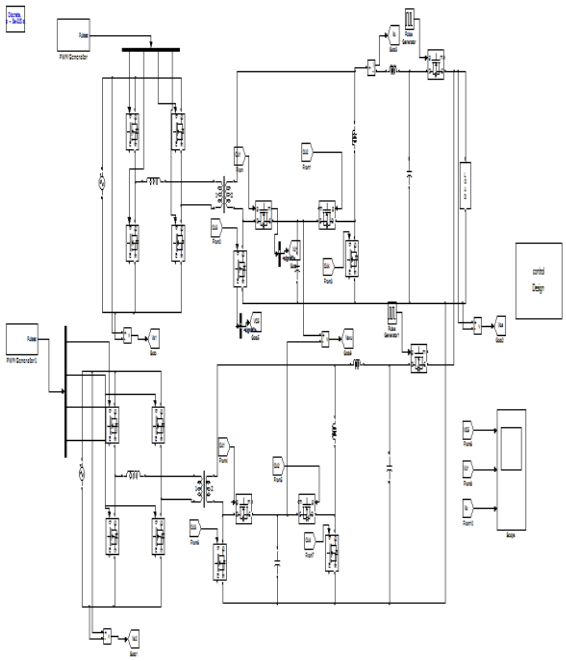

Fig10(a) SIMULINK DIAGRAM OF CHARGING MODE

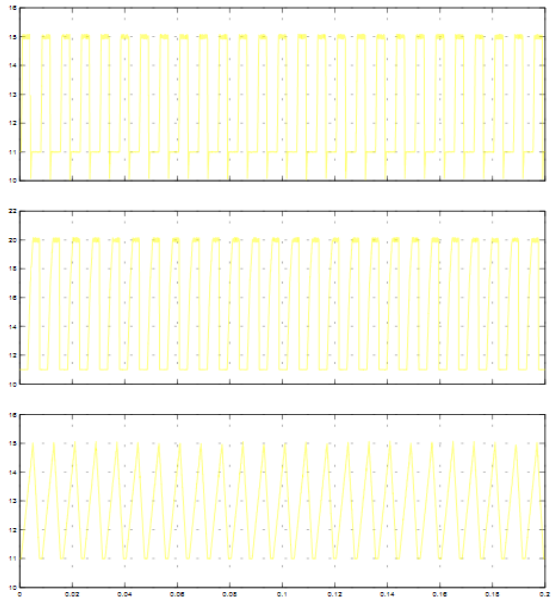

Fig10(b) Out Put

In the charging mode, the primary-side of the master is still turned off but the slave is turned on. Thus, the slave transfers power to the load and charges CA by using the bidirectional buck converter with the boost operation, as shown in above Figure.

Snubbers are frequently used in electrical systems with an inductive load where the sudden interruption of current flow leads to a sharp rise in voltage across the current switching device ("inductive kick"), in accordance with Faraday's law. This transient can be a source of electromagnetic interference (EMI) in other circuits. Additionally, if the voltage generated across the device is beyond what the device is intended to tolerate, it may damage or destroy it. The snubber provides a short-term alternative current path around the current switching device so that the inductive element may be discharged moresafely and quietly. Inductive elements are often unintentional, but arise from the current loops implied by physical circuitry. While current switching is everywhere, snubbers will generally only be required where a major current path is switched, such as in power supplies. Snubbers are also often used to prevent arcing across the contacts of relays and switches and the electricalinterference and welding or sticking of the contacts that can occur (see also arc suppression).

VII.CONCLUSION

A new power conversion scheme is presented using paralleled modules is to be proposed. Under a very light-load condition, converter

achieved high efficiency by using an integrated bidirectional buck converter. The buck converter is integrated easily by using switches instead of snubber diodes. By connecting the snubber voltage from each module and by using it as additional voltage bus, an auxiliary voltage source is effectively obtained for the buck converter. In this project the circuit operation and design considerations are illustrated. The validity of the basic operational principles is confirmed with two 12V/750W by using MATLAB/Simulink software. The results will be demonstrated for the proposed converter.

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