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Design of low power high -performance of 2-4 and 4-16 mixed logic line decoders

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ABSTRACT:

This paper presents a Mixed logic design strategy for line decoders, consolidating transmission entryway logic, pass transistor double esteem logic and static CMOS. Two epic topologies are exhibited for the 2-4 decoder: a 14-transistor topology pointing on limiting transistor tally and power dispersal and a 15-transistor topology pointing on high power-defer execution. Both a typical and a modifying decoder are actualized for each situation, yielding an aggregate of four new designs. Besides, four new 4-16 decoders are designed, by utilizing blended logic 2-4 pre decoders joined with standard CMOS post-decoder. All proposed decoders have full swinging ability and decreased transistor check contrasted with their traditional CMOS partners. At long last, an assortment of relative recreations at the 65 nm demonstrates that the proposed circuits present a noteworthy enhancement in power and postponement, outflanking CMOS in all cases.

Index Terms—line decoder, mixed-logic, power-delay optimization.

INTRODUCTION

1.0 SCOPE OF THE PROJECT

Power management has turned into a noteworthy issue in the advancement of a computerized system particularly, in the versatile gadgets in which upgrade of the battery life time and diminishing the charging time are turning into a testing issues step by step. The significant issue is power dispersal. Innovation scaling prompts Increase spillage current, which prompts increment in sub edge spillage current. It is fundamental that these high computational capacities are put in a low-power, compact condition. Thus, an all around coordinated low vitality design methodology must be set up. As the thickness of the incorporated circuits and size of the chips and systems propagate to develop, it turns out to be increasingly laborious to give sufficient cooling to the systems.

In joining to warm deliberation, there are monetary and natural issues for low power advancement. In the Amalgamated States, PC hardware represents around 2-3% of aggregate power utilization. This figure is required to increase as there is gigantic increment in family PC applications, Web telephones, handheld PCs, and inside terminals. These financial and natural reasons have constrained the essential for vitality effective PCs.

With the end goal to meet the injunctive approval in high computational applications, the clock rate is relentlessly augmenting and clock skew being an undeniably central piece of the clock cycle. The vitality devoured by low-skew clock appropriation systems is unendingly developing.

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Clock-related power utilization can achieve more than 30-40% of the aggregate power of microchip and is turning into an all the more cosmically massive portion of the chip strength. In coordination, the quantity of logic door delays in a clock period is decreased by 25% per age. Subsequently, dormancy of flip tumbles or hooks is turning into an all the more cosmically monstrous bit of the process duration.

Static CMOS circuits are used for most by a long shot of logic portals in composed circuit . They involve comparing nMOSpulldown and pMOSpullup systems and present extraordinary execution and what's more security from disturbance and device assortment. Thusly, CMOS logic is depicted by power against voltage scaling and transistor assessing and in like manner reliable undertaking at low voltages and little transistor sizes. Data signals are related with transistor entryways simply, offering diminished design multifaceted nature and help of cellbased logic amalgamation and design. Pass-transistor logic was predominantly made amid the 1990s, when distinctive design styles were displayed, hoping to give a viable choice as opposed to CMOS logic and upgrade speed, power and locale. Its central design refinement is that inputs are associated with both the gateways and the source/drain spread terminals of transistors. Pass transistor circuits are realized with either individual nMOS/pMOS pass transistors or parallel arrangements of nMOS and pMOS called transmission gateways. This work develops a mixed logic design system for line decoders, joining gateways of different logic to a comparable circuit, with a true objective to get improved execution stood out from single-style design.

Line decoders are real circuits, by and large used in the periphery equipment of memory groups (e.g. SRAM), multiplexing structures, execution of boolean logic limits and diverse applications. Notwithstanding their criticalness, a for the most part little proportion of composing is committed to their optimization, with some progressing work including.

I. OVERVIEW OF LINE DECODERCIRCUITS

In cutting edge systems, discrete measures of data are addressed by twofold codes. A n-bit twofold code can address up to 2n obvious parts of coded data. A decoder is a combinational circuit that changes over twofold data from n input lines to a most extraordinary of 2n exceptional output lines or less, if the n-bit coded data has unused mixes. The circuits investigated in this work are called n-to-m line decoders, and their purpose is to make the m = 2n minterms of n input factors.

A. 2-4 LineDecoder

A 2-4 line decoder delivers the 4 minterms D0-3 of 2 input factors An and B. Its logic errand is dense in Table. Dependent upon the data blend, one of the 4 outputs is picked and set to 1 while the others are set to 0. An improving 2-4 decoder makes the indispensable minterms

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I0-3, along these lines the picked output is set to 0 and the rest are set to 1, as showed up in TableII.

TABLEI:TRUTH TABLE OF 2-4 DECODER

A	B	D 0	D 1	D 2	D 3
0	0	1	0	0	0
0	1	0	1	0	0
1	0	0	0	1	0
1	1	0	0	0	1

TABLEII:TRUTH TABLE OF INV 2-4 DECODER

A	B	I 0	I 1	I 2	I 3
0	0	0	1	1	1
0	1	1	0	1	1
1	0	1	1	0	1
1	1	1	1	1	0

In regular CMOS design, NAND andNOR doors are liked to AND or potentially, since they can be executed with 4 transistors, rather than 6, in this way actualizing logic capacities with higher effectiveness. A 2-4 decoder can be executed with 20 transistors utilizing 2 inverters and 4 NOR doors, as appeared in

Fig.1(a).The relating invertingimplemented with 2-4 decoders and 16 2-input NAND entryways (Fig. 2(b)). In CMOS logic, these designs require 8 inverters and 24 4-input entryways, yielding a sum of 104 transistors each.

(a) (b)

Fig. 1. 20-transistor 2-4 line decoders executed with CMOS logic: (a) Non-annoying NOR-based decoder, (b) Inverting NAND-based decoder. Decoder can in like manner be realized with 20 transistors using 2 inverters and 4 NAND entryways, as showed up in Fig. 1(b).

A. 4-16 Line Decoder with 2-4Predecoders

A 4-16 line decoder delivers the 16 minterms D0-15 of 4 input factors A, B, C and D, and a changing 4-16 line decoder makes the relating minterms I0-15. An unmistakable execution of these circuits would require 16 4-input NOR and NAND gateways. Nevertheless, a more capable design can be gotten using a predecoding method, as shown by which squares of n address bits can be predecoded into 1-of-2n predecoded lines that fill in as commitments to the last stage decoder [1]. With this system, a 4-16 decoder can be realized with 2-4 changing decoders and 16 2-input NOR entryways (Fig. 2(a)) and a disquieting one can beFig. 2. 104-transistor 4-16 line decoders completed with CMOS logic and predecoding: (a) Non-adjusting decoder executed with two 2-4 changing predecoders and a NOR-based post-decoder, (b) Inverting decoder executed with two 2-4 non-modifying predecoders and a NAND-based post-decoder.

III. NEW MIXED-LOGICDESIGNS

In combinational logic, transmission passages have generally been used in XOR-based circuits, for instance, full adders and as the basic switch segment in multiplexers. In any case, we consider their use in the utilization of AND/OR logic, as showed in [5], which can be viably associated in line decoders. The 2-input TGL AND/OR entryways are showed up in Fig. 3(a) and 3(b), exclusively. They are full-swinging, anyway not restoring for all inputcombinations.Regarding pass-transistor logic, there are two rule circuit styles: those that use nMOS simply pass-

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transistor circuits, as CPL [3] and those that use both nMOS and pMOS pass-transistors, as DPL [4] and DVL [6]. The style we consider in this work is DVL, which offers an improvement for DPL, shielding its full swing movement with lessened transistor count[10].The2-inputDVLAND/ORgatesareshowninFig. 3(c) and 3(d), independently. Like the TGL portals, they are full-swinging anyway non-restoring.Assuming that relating wellsprings of information are available, the TGL/DVL entryways require only 3 transistors, as opposed to the 4 required in CMOS NAND/NOR entryways. Decoders are high fanout circuits, where couple of inverters can be used by various portals, in this manner using the TGL/DVL entryways can result to decreased transistor check

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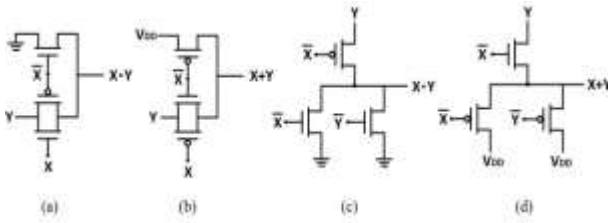

Fig. 3. The 3-transistor AND/OR entryways considered in this work (a) TGL AND passage, (b) TGL OR gateway, (c) DVL AND portal, (d) DVL OR entryway.

A fundamental essential typical for thesegates is their hilter kilter nature, ie the manner in which that they don't have balanced data loads. As showed up in Fig. 3, we named the 2 entryway inputs X and Y. In TGL gateways, input X controls the entryway terminals of all3 transistors, while input Y spreads to the output center point through the transmission door. In DVL passages, input X controls2 transistor entryway terminals, while input Y controls 1 portal terminal and causes through a pass transistor to the output. We will imply X and Y commitments as the control hail and the spread banner of the portal, separately.

This hilter kilter incorporate gives a designer the versatility to perform hail game-plan, ie picking which input is used as control and which as multiply movement in every portal. Having a relating commitment as cause hail is definitely not a nice practice, since the inverter added to the expansion way manufactures delay basically. Thusly, while executing the obstacle (A'B) or proposal (A'+B) work, it is more capable to pick the changed variable as control hail. While completing the AND (AB) OR (A+B) work, either choice is correspondingly gainful. Finally, while realizing the NAND (A'+B') or NOR (A'B') work, either choice outcomes to a relating spread signal,perforce.

A. The 14-transistor 2-4 Low-PowerTopology

Designing a 2-4 line decoder with either TGL or DVL entryways would require a whole of 16 transistors (12 for AND/OR passages and 4 for inverters). Regardless, by mixing both AND door types into a comparable topology and using authentic banner game-plan, it is possible to shed one of the two inverters, along these lines diminishing the total transistor count to 14.Let us expect that, out of the two wellsprings of information, specifically An and B, we mean to take out the B inverter from the circuit. The Do minterm (A'B') is realized with a DVL entryway, where An is used as spread banner. The D1 minterm (AB') is realized with a TGL door, where B is used as induce signal. The D2 minterm (A'B) is executed with a DVL entryway,

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where An is used as spread banner. Finally, The D3 minterm (AB) is executed with a TGL gateway, where B is used as spread banner. These particular choices thoroughly dismiss the usage of the fundamental B hail, in like manner the Binverter can be abstained from the circuit achieving a 14-transistor topology (9 nMOS, 5 pMOS).

Following a similar system with OR passages, a 2-4 turning around line decoder can be completed with 14 transistors (5 nMOS, 9 pMOS), as well: I0, I2 are executed with TGL (using B as incite banner) and I1, I3 are realized with DVL (using An as spread banner). The B inverter can undoubtedly beelided.The inverter transfer diminishes transistor count, logical effort and as a rule trading activity of the circuits, in this way constraining power spread. To the degree the makers are concerned, 14 is the base number of transistors required to comprehend a full-swinging 2-4 line decoder with static (non-planned) logic. The two new topologies are named '2-4LP' and '2-4LPI', where 'LP' stays for 'low power' and 'I' for 'disquieting'. Their schematics are showed up in Fig. 4(a) and Fig. 4(b),respectively.

Fig. 5. New 15-transistor 2-4 line decoders: (a) 2-4HP (b) 2-4HPI.

Grasping this design method, and concerning the hypothesis showed on territory II, we executed four 4-16 decoders by using the four new 2-4 as predecoders identified with CMOS NOR/NAND ways to convey the decoded outputs. The new topologies got from this mix are: 4-16LP (Fig. 6(a)), which solidifies two 2-4LPI predecoders with a NOR-based post-decoder, 4-16HP (Fig. 6(b)), which joins two 2-4HPI predecoders with a NOR-based post-decoder, 4-16LPI (Fig. 6(c)), which unites two 2-4LP predecoders with a NAND-based post-decoder and, finally, 4-16HPI (Fig. 6(d)), which joins two 2-4HP predecoders with a NAND-based post-decoder.

DESIGN TOOLS

Microwindis an instrument for designing and reproducing circuits at format level. The device includes full altering offices (duplicate, cut, past, copy, move), different perspectives (MOS attributes, 2D cross segment, 3D process watcher), and a simple test system. DSCH is programming for logic design. In light of natives, a various leveled circuit can be assembled and reenacted. It likewise incorporates postponement and power utilization assessment. Siliconis for 3D show of the nuclear structure of silicon, with accentuation on the silicon grid, the dopants, and the silicon dioxide.

Instruments from Microwind

Microwind

MICROWIND is truly consolidated EDA programming including IC designs from thought to fulfillment, empowering chip designers to design past their inventive vitality. MICROWIND joins for the most part separated front-end and back-end chip design into an organized flow, animating the design cycle and diminished design complexities. It solidly arranges mixed banner execution with cutting edge utilization, circuit multiplication, transistor-level extraction and affirmation giving an imaginative guidance action to help individuals with building up the aptitudes required for design positions in essentially every space of IC industry.

DSCH (Schematic Editor and Digital Simulator)

The DSCH program is a logic editor and test system. DSCH is used to support the

building of the logic circuit before the microelectronics design is started. DSCH gives a straightforward condition to different leveled logic design, and brisk reenactment with concede examination, which allows the design and endorsement of complex logic structures.

DSCH in like manner incorporates the pictures, models and get together help for 8051 and 16F84 controllers. Designers can make logic circuits for interfacing with these controllers and check programming programs using DSCH.

It have someimportant centers are,

- User-obliging condition for quick design of logic circuits.
- Supports dynamic logic design.
- Handles both ordinary model built logic entertainment and common as for screen mouse-driven reenactment.
- Improved worked in extractor which delivers a SPICE netlist from the schematic chart (Compatible with PSPICETM and WinSpiceTM).
- Generates a VERILOG depiction of the schematic for configuration change.
- Immediate access to picture properties (Delay, fanout).
- Model and get together help for 8051 and PIC 16F84 microcontrollers.
- Sub-micron, significant submicron, nanoscale development support.
- Supported by huge picture library.

Prothumb (Mix-flag Simulator)

No SPICE or outside test system is required for affirmation of CMOS circuits. Microwind program has in created basic like test system which supports MOS Level 1, Level 3 or BSIM4 show. With features like snappy time-space, voltage and current estimation, amazingly common post taking care of, repeat estimation, concede estimation, sets aside a couple of minutes saver. In fact, even power estimation of circuit diversion can be watched out for screen.

It have someimportant centers are,

- Built-in SPICE-like straightforward test system.
- Features speedy time-region, voltage and current estimation, with to a great degree characteristic post taking care of: repeat estimation, concede estimation. (No outside SPICE/basic Simulator required).
- Supports level1, level3 and BSIM4 models for all headways from 1.2µm till 22 nm.
- MOS trademark watcher with access to parameters of central model.
- Time-space voltage and current waveforms available at the press of one single catch.
- DC/AC characteristics, hail repeat versus time, eye diagrams Min/Typ/Max basic diversion.
- Eye diagram see for banner output.
- On screen power estimation.
- Onscreen amassing of waveforms for result hold tight.

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- Forward and in turn around gets to move in proliferation results.

Nanolambda (Precision CMOS Layout Editor)

MICROWIND have an exactness CMOS design director, which supports headways fitting from 1.2um till 22 nm with unfathomable diagram limits. With its redesigned adjusting headings and configuration control your progression times would be shorter than you anytime imagined. Some basic centers are,

- Huge advancement support till 22 nanometers

- Design-botch free cell library (Contacts, vias, MOS contraptions, et cetera.).

- Powerful customized compiler from Verilog structure circuit into design.

- On-line design rule checker with tremendous rule base.

Protutor (MOS Characteristics TUTOR)

Beneficial screen to fathom the MOS characteristics, with a UI that designers will like. Change the model parameters and see their effects on Id/Vd, Id/Vg Id(log)/Vg, edge versus length. You can moreover fit the reenactments with estimations we made in test-chips made in 0.35, 0.25 and 0.18µm. In the manual, an instructional exercise on MOS models is given, with unpretentious components on all parameters. A couple of Points are,

- Change the model parameters and see their effects on Id/Vd, Id/Vg, Id(log)/Vg, edge versus Length.

- You can moreover fit the proliferations with estimations we made in test chips produced in 0.35, 0.25 and 0.18 µm.

- Full length instructional exercise on MOS models is given in manual, with unpretentious components on all parameters.

- Documentation joins a couple of parts of MOS showing

MEMSim (Floating Gate Memory Simulator)

The twofold entryway MOS has been displayed in MICROWIND for the amusement of non-unusual memories, for instance, EPROM, EEPROM and FLASH. The course "UV introduction" erases floating gateways and clears all electrons. The composition PC programs is performed by a high voltage supply on the entryway (7V in 0.12µm), a 1.2V voltage refinement among drain and source. A couple of electrons are sufficiently revived to experience the entryway oxide by hot tunneling sway. Highlights are,

- Simulation of non-unsteady memories, for instance, EPROM, EEPROM and FLASH using twofold entryway MOS.

- Erasure of floating passages and clearing all electrons.

- Programming can be performed by a high voltage supply on the entryway.

VirtualFab (Cross sectional and 3D Viewer)

You will never demonstrate significant sub micron advancement like already. As VirtualFab offers you an office to separate and see cross sectional point of view of silicon layers and 3D viewpoint of circuits.

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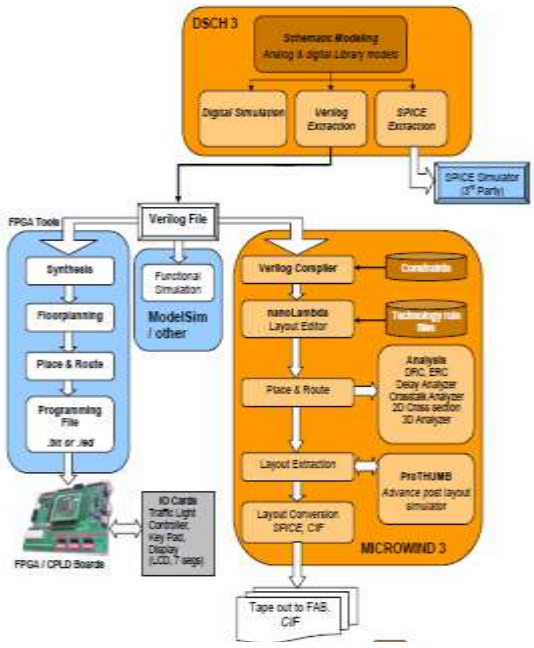
With MICROWIND v3.1 empowers to draw consistent photos of the design and investigate in full-3D at first look or inside the IC. This request relies upon OpenGL and offers outstanding picture quality. The customer can change the study position in X, Y, Z and play with light sources to make illustrative points of view of the design. A couple of focuses are,

- 3D fabricate process test system with cross sectional watcher.
- Step-by-arrange 3-D view of creation for any piece of configuration.
- See how the contacts and metallization are made.
- See oneself balanced scattering after the polysilicon entryway is made.
- Check planes of VDD, VSS, and others signals.

MICROWIND TOOL DESIGN FLOW



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DSCH in like manner incorporates the pictures, models and assembling support for 8051 and 16F84 controllers. Designers can make logic circuits for interfacing with these controllers and affirm programming programs using DSCH.

It have someimportant centers are,

- User-obliging condition for snappy design of logic circuits.

Fused circuits have changed the technique for our life. You name one gadget and will find the power of silicon which has made such complex electronic circuits possible. Facilitated circuits arrive in an extensive variety of flavors these days. Customer designed chips particularly , CPLDs and FPGAs have transformed the technique for system design. However, ASIC remains in lead, due to their speed, power and execution central focuses. Every fundamental system design is hailed with ASICs. To take in the IC design process, systems and 'fundamental' essential managing, engineers practice for an extensive period of time and hours.on EDA mechanical assemblies to expert know-how of design basics.

Present day ASIC design mechanical assemblies like DSCH and MICROWIND offers easy to encounter design flow for CMOS IC designs. It supports customary schematic circuit building procedures, organize changing, distinctive examination and affirmation systems, and fab close down. In any case, more than rights and lefts of IC design flow, it's the key design approach and circuit building techniques which prompts achievement in produce. Regardless, a noteworthy number of times, engineers stand up to hindrances in the midst of multiplication and dissatisfactions in prototyping.

EDA mechanical assemblies like MICROWIND and DSCH, which offers an aggregate IC design flow, which starts with schematic working of cutting edge circuits and a short time later changing over into verilog report for array in CMOS arrange using MICROWIND organize compiler. Every designer needs to affirm circuit before going for Fabrication. FPGAs are best available stage for ASIC prototyping.

MICROWIND supports entire front-end to back-end design flow .For front-end designing, we have DSCH (propelled schematic director) which groups in-created precedent based test system for electronic circuits. Customer can moreover create straightforward circuits and convert them into SPICE reports and use pariah test systems like WinSpice or pSPICE.

incorporated for FPGA/CPLD devices of any trader. The equal Verilog archive can

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be organized configuration change in MICROWIND.

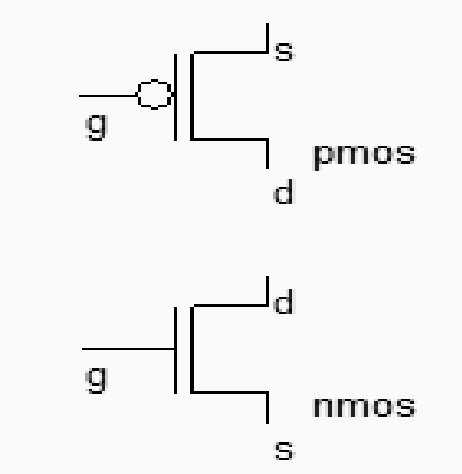
The back-end design of circuits is reinforced by MICROWIND. Customer can design propelled circuits and collect here using Verilog record. MICROWIND normally makes a bungle free CMOS design. In spite of the way that this place-course isn't adequately enhanced as we loath complex place and course algorithms.

Customer can in like manner make CMOS design of their own using total one line Verilog etymological structure or custom frame the organizations by manual delineation. The CMOS organizations can be affirmed using inbuilt mix signal test system and dismembered assist for DRC, cross talks, delays, 2D cross section, 3D see, et cetera.

• THE MOS AS A SWITCH

The MOS transistor is in a general sense a switch. Exactly when used in logic cell design, it will in general be on or among drain and source. The MOS is turned on or off dependent upon the entryway voltage. In CMOS advancement, both n-channel (ornMOS) and pchannel MOS (or pMOS) devices exist. The nMOS and pMOS pictures are represented underneath. The pictures for the ground voltage source (0 or VSS) and the supply (1 or VDD).

DSCH can change over the propelled circuits into Verilog record which can be moreover



The n-channel MOS gadget requires a logic esteem 1 (or a supply VDD) to be on. In opposite, the p-channel MOS gadget requires a logic esteem 0 to be on. At the point when the MOS gadget is on, the connection between the source and deplete is identical to an opposition. The request of scope of this 'on' opposition is 100ω-5KΩ. The 'off' opposition is viewed as limitless at first request, as its esteem is a few Mω.

6.4THREE LEVELS OF DESIGN IN MICROWIND AND DSCH

• The details we will see might be distinctive for various foundry and innovation.

• Design Example (3 Levels): NOR Gate

– Logic Design

– Circuit Design

– Layout Design

Microwind / DSCH NOR Example: NOR Gate Logic

- Open the Schematic Editor in Microwind (DSCH3). Click on the transistor symbol in the symbol Library on the right.
- Instantiate NMOS or PMOS transistors from the symbol library

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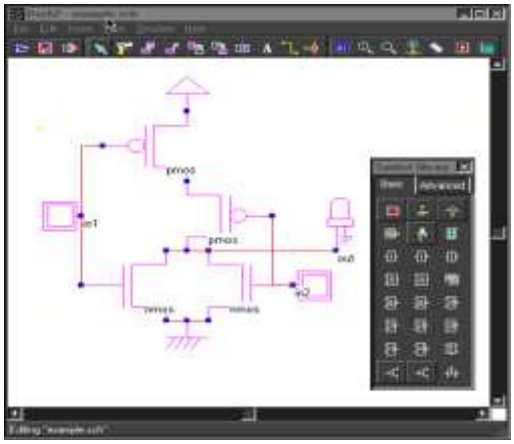
and place them in the editor window.

- Instantiate 2 NMOS and 2 PMOS transistors.
- Connect the drains and sources of transistors.
- Connect Vdd and GND to the schematic.
- Connect input button and output LED.



Presently we have NOR schematic prepared.

• Use your logic test system to check the usefulness of your schematic.

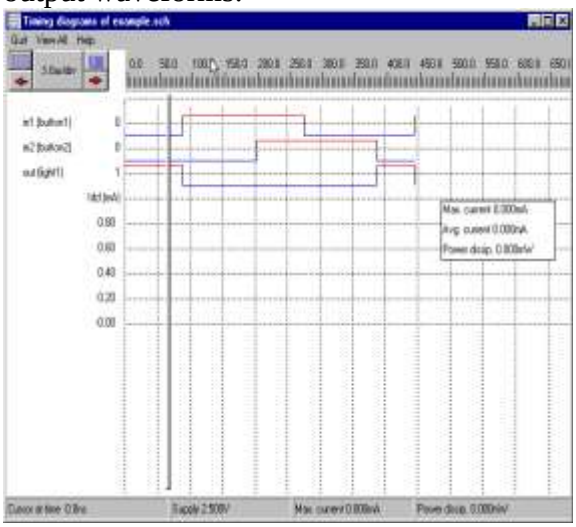
• The subsequent stage is to reenact the circuit and check for usefulness.

• Click on, Simulate - > Start reenactment.

• This raises a Simulation Control Window.

• Click on the info catches to set them to 1 or 0. Red shading in a switch shows a '1'. As appeared,

The reenactment output can be seen as a waveform after the utilization of the contributions as above. Tap on the planning outline symbol in the symbol menu to see the planning chart of the information and output waveforms.



Simulate your system with your hand calculated transistor sizes. Click File ->Make Verilog File. The Verilog, Hierarchy and Netlistwindow appears. This window shows the verilog representation of NOR gate.

- Click OK to save the Verilog as a .txt file.

Microwind / DSCH NOR Example: Circuit Design

- Open the layout editor window in Microwind. Click *File ->Select Foundry* and select *X.rul*.This sets your layout designs in X technology.
- Click on *Compile ->Compile Verilog File.* An *Open* Window appears Select the .txt verilogfile saved before and open it.

After selecting the .txt file, a new window appears called Verilog file.Click on Size on the right top menus. This shows up the NMOS and PMOS sizes. Set the sizes according to choice.

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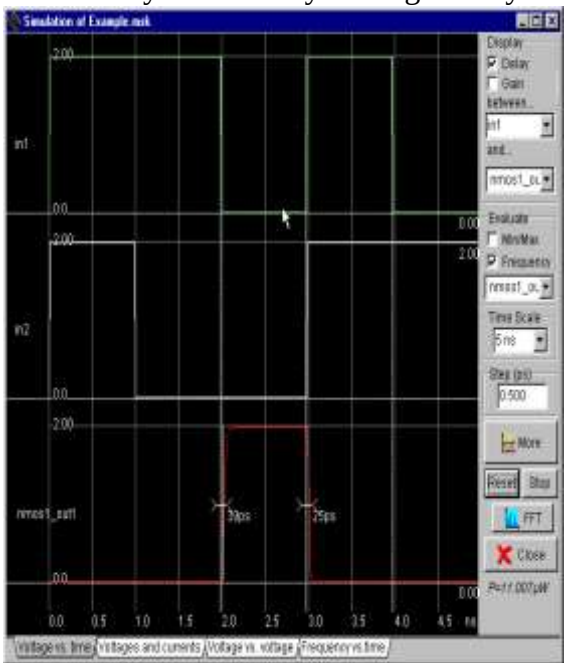
- Click Compile and then Back to editor in the Verilog File Window. This creates a layout in layout editor window using automatic layout generation procedure.
- Add a capacitance to the output of the design. The value of the capacitance depends on your choice.
- Click on OK. The capacitance is shown on the left bottom corner with a value of 0.015fF.
    - Click Simulate ->Run simulation. A simulation window appears with inputs and output, shows the tphl, tplh and tp of the circuit. The power consumption is also shown on the right bottom portion of the window.
    - If you are unable to meet the specifications of the circuit change the transistor sizes. Generate the layout again and run the simulations till you achieve your target delays.



Microwind / DSCH NOR Example: Layout Design

• Design the design physically. Open the format editorial manager window in Microwind. Snap File - >Select Foundry and select X.rul,Vdd and GND rails are of Metal1. The best rail is utilized as Vdd and the last one as GND. Tap on Metal 1 in the palette and after that makes the required square shape in the design window.

• The subsequent stage is to construct the NMOS transistors. Tap on the transistor image in the palette. Set the W, L of the transistor

• Then tap on Generate gadget. The wellspring of the transistor is associated with the GND rail. Make another NMOS and place it in parallel to the principal NMOS gadget. We share the two gadgets' deplete dispersions. A DRC check can be controlled by tapping on Analysis - >Design Rule Checker.

• The following stage is to put two PMOS transistors in arrangement. Place the PMOs transistor on format near the Vdd rail on the best. To develop two PMOS transistors in arrangement, dispersions are moved to a side and another poly line is included as second transistor. The dispersion is shared to spare region and lessen capacitance.

• The subsequent stage is to associate the sources of info and the output of the two transistors. Poly inputs is associated. Metal output is associated.

• The following stage is to associate the poly to metal1 and after that to metal2. The principal image in the main column of the palette is the poly to metal1 contact.

• Then we interface the metal1 to metal2 contact to the past contact. This is the fourth contact on the main column

• The subsequent stage is to interface the output Metal1 to Metal2. Indeed utilize the fourth contact in the principal push.

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• Now we interface metal2 to the two data sources and one output and convey them to the best to leave the cell. Watch the two data sources (left and right) and an output (center) over the Vdd rail in dim blue shading.

Presently we mark the information sources and output as In1, In2 and out. Tap on Add a Pulse Symbol in the palette (fifth from the privilege in the third line). At that point tap on the metal2 of one of the sources of info. A window shows up. Change the name of the information flag. Embed a 01 groupings and tap on Insert. The tap on Assign. Likewise appoint the second info a heartbeat.

Select the Visible Node image from the palette (seventh in the third column). Select it and tap on the output. The 'Include a Visible Property' window shows up. Change the name to out. Select Visible in Simulation. Tap on Assign. Presently the output is additionally named.

Select Vdd Supply and GND from the palette (third line). Additionally tap on the capacitor (third in second line) image and add it to the output. Likewise, expand the pwell into the Vdd Rail. The tap on Edit ->Generate - >Contacts. Select PATH and afterward in Metal pick Metal1 and N+ polarization.

To run the Simulation of your circuit, tap on Simulate - >Start Simulation. Contingent upon the info successions relegated at the information the output is seen in the reenactment. The power esteem is additionally given.

SIMULATION RESULTS

All the simulations are performed on Microwind and DSCH. The main focus of this work is to meet all challenges faces in designing of Decoder circuit using mixed logic. This work develops a mixed-logic design methodology for line decoders, combining gates of different logic to the same circuit, in an effort to obtain improved performance compared to single-style design. The simulation results are shown below figures.

Table:1 Comparisons results of mixed-logic line decoders

DESIGN	PARAMETERS	
	NO.OF TRANSISTORS	POWER
2to4 Decoder CMOS	6T	7.315uw
2to4 Decoder Mixed Logic	8T	6.647uw
4to16 Decoder CMOS	6T	7.315uw
4to16Decoder Mixed Logic	8T	6.647uw

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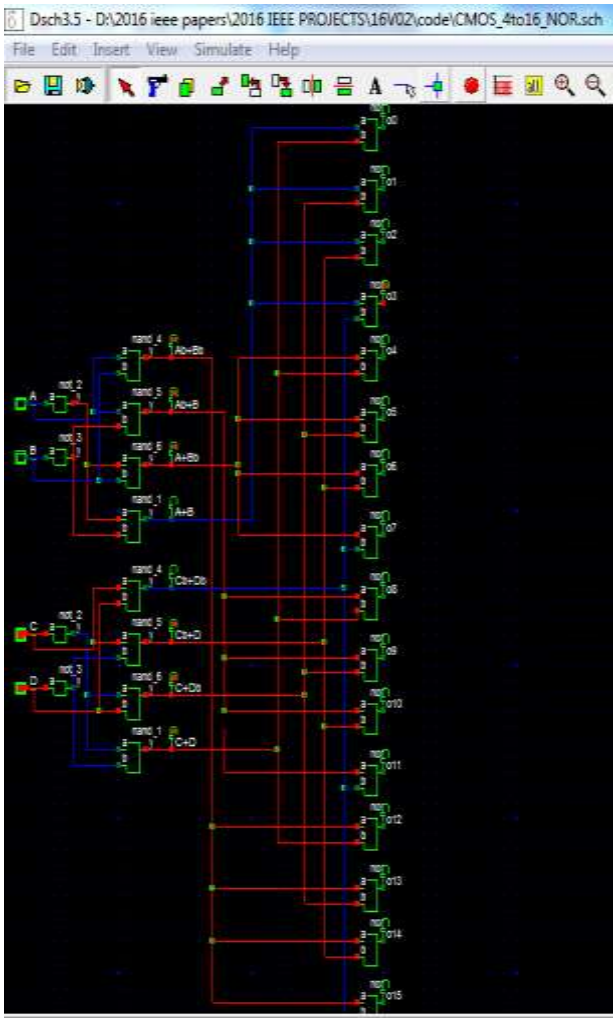

Fig 7: Schematic of 4to16 Decoder Using CMOS

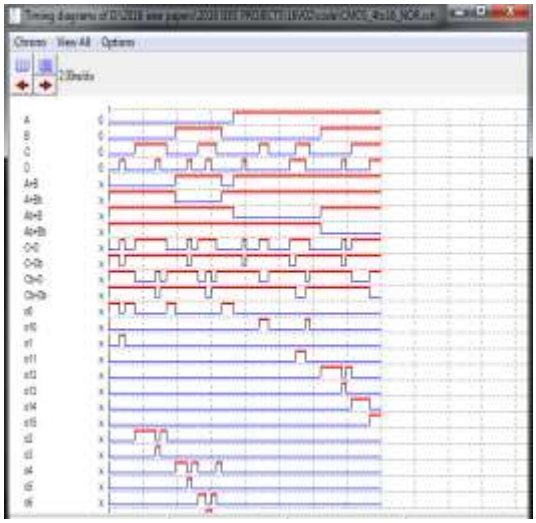

Fig 8: Timing Diagram of 4to16 Decoder Using CMOS

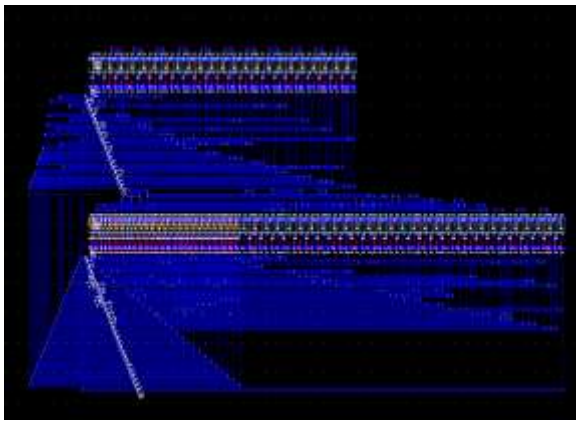

Fig 9: Layout of 4to16 Decoder Using CMOS

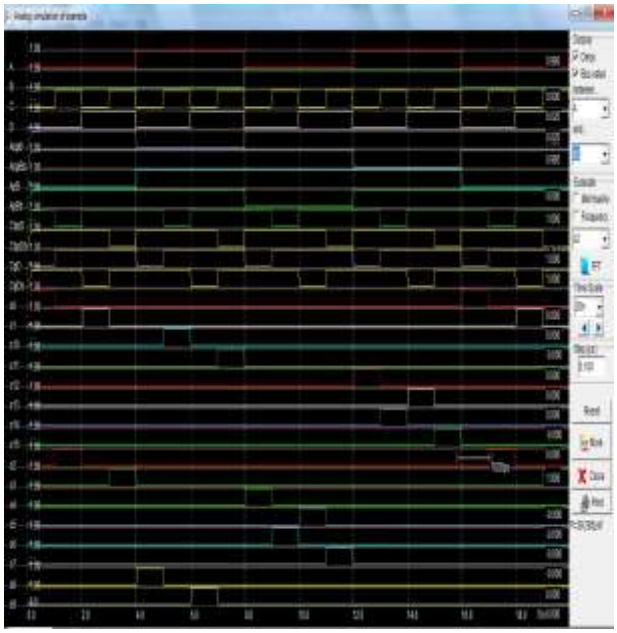

Fig 10: Simulation of Layout of 4to16 Decoder Using CMOS

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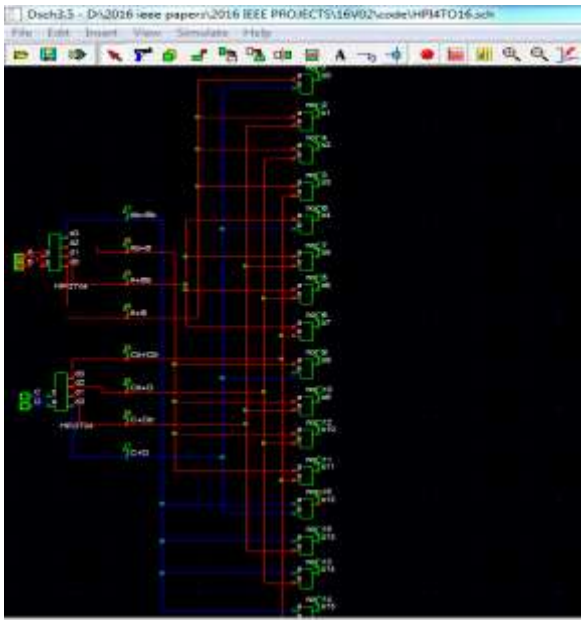

Fig 11: Schematic of 4to16 Decoder Using HPI

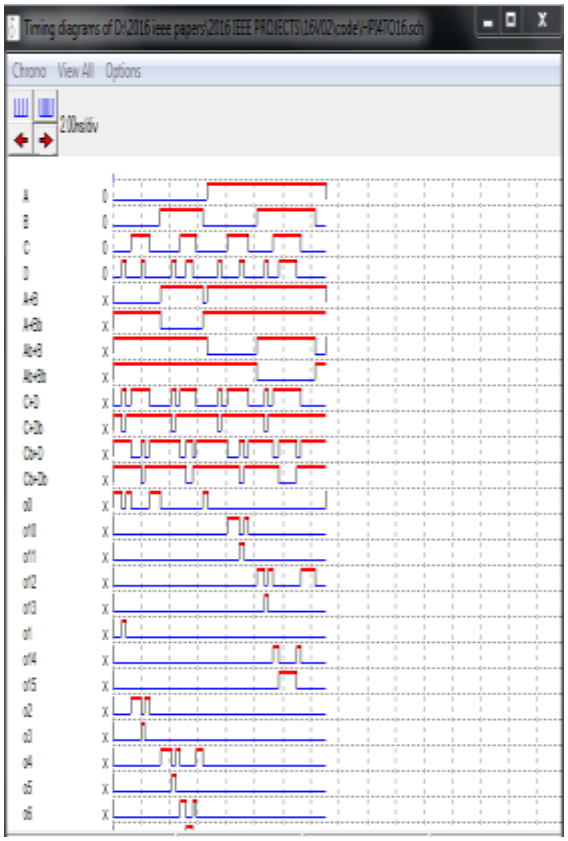

Fig 12: Timing Diagram of 4to16 Decoder Using HPI

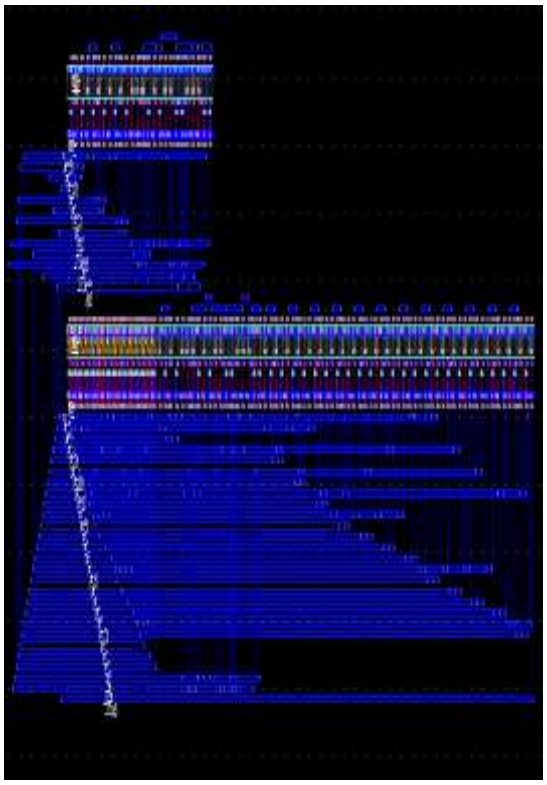

Fig 13: Layout of 4to16 Decoder Using HPI

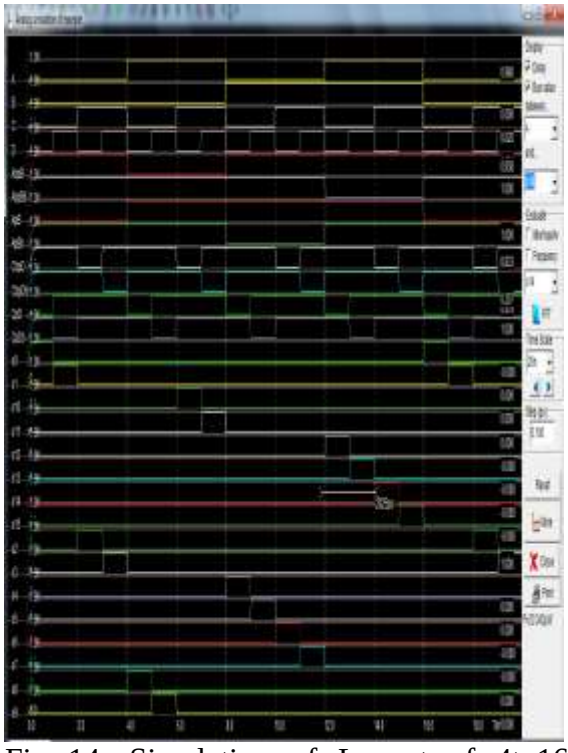

Fig 14: Simulation of Layout of 4to16 Decoder Using HPI

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Comparisons results of cmos and mixed-logic line decoders
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S.No	Design Name	No.of Trans	Area(um^2)	Power (uW)
1	2to4CMOS NAND	20	101.2	6.510
	2to4CMOS NOR	20	101.2	6.730
	2to4 LP(NOR)	14	66.9	1.700
	2to4 LPI(NAND)	14	66.9	3.319
	2to4 HP(NAND)	15	70.8	1.855
	2to4 HPI	15	70.8	3.315
2	4to16CMOS NAND	104	1301.4	28.013
	4to16CMOS NOR	104	1350	29.012
	4to16LP(NOR)	92	1141.6	17.785
	4to16LPI(NAND)	92	1145.7	14.726
	4to16HP(NAND)	94	1190.2	13.683
	4to16HPI(NOR)	94	1190.2	18.107

CONCLUSION

This paper presented a productive blended reason design for decoder circuits, joining TGL, DVL and static CMOS. By utilizing this objectivity, we made four new 2-4 line decoder topologies, especially 2-4LP, 2-4LPI, 2-4HP and 2-4HPI, which offer decreased transistor check (consequently potentially more minor design zone) and redesigned power-postpone execution in relationship with standard CMOS decoders.

Besides, four new 4-16 line decoder topologies were appeared, to be specific 4-16LP, 4-16LPI, 4-16HP and 4-16HPI, perceived by utilizing the blended strategy for thinking 2-4 decoders as predecoding circuits and obliging them with post-decoders executed in static CMOS premise. These designs harden the redesigned execution qualities of pass transistor technique for prevailing upon the reestablishing limit of static CMOS.A gathering of similar flavor reenactments was performed at the 32 nm, checking, in most cases,a clear supported position for the proposed designs. The 2-4LP and 4-16LPI topologies are by and large sensible for applications where area and power minimization is of fundamental concern. The 2-4LPI, 2-4HP and 2-4HPI, and what's progressively the relating 4-16 topologies (4-16LP, 4-16HPI, 4-16HP), wound up being sensible and all-around proficient designs, in like way they can adequately be utilized as building ruins in the design of more prominent decoders, multiplexers and other combinational circuits of changing execution requirements.Moreover, the indicated diminished transistor check and low power characteristics can profit both mass CMOS and SOI design too. The picked up circuits are to be executed on plan level, making them sensible for standard cell libraries and RTL design.

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