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A Novel Coupled-Inductor Single-Phase Boost DC-AC Inverter for Photovoltaic Systems

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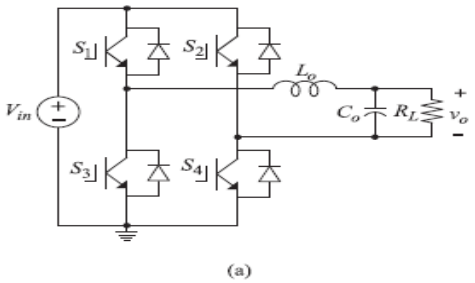
ABSTRACT: This paper presents a new single-phase switched coupled-inductor dc–ac inverter featuring higher voltage gain than the existing single-phase qZ-source and semi-Z-source inverters. Similar to the single-phase qZ-source and semi-Z-source inverters, the proposed inverter also has common grounds between the dc input and ac output voltages, which is beneficial especially for photovoltaic inverter systems. The inverter volume and maximum current flowing can be reduced significantly through the coupling of all inductors. A theoretical analysis of the proposed inverter is described and a 280-W experimental prototype is built to verify the performance of the inverter.

***Index Terms*—Common ground, dc–ac inverter, high voltage gain, qZ-source inverter, single-phase inverter, switched-coupled- inductor (SCL), Z-source inverter.**

I. INTRODUCTION

Now-a-Days, there is an increasing demand for low-cost single-phase dc–ac inverters in many applications such as photovoltaic (PV), fuel cell, and battery powered systems. The conventional methods are shown in Fig.1. 1. Fig.1. 1(a) shows the well-known full-bridge (FB) inverter referred to as buck inverter in this project. In this circuit, the inverter output voltage (*vo)* cannot be greater than input voltage (*V*in). When the input voltage is low, a boost dc–dc converter is inserted between *V*in and the inverter bridge as shown in Fig.1. 1(b). However, the two topologies in have different input and output grounds. This may result in large leakage current in applications such as transformer-less grid-tied PV inverter, which will cause safety and electromagnetic interference problem. In order to overcome the disadvantages of the conventional inverters, a large number of single-stage inverters are proposed. In addition, the Z-source inverter topologies overcome the limitations mentioned earlier. Fig.1(a) shows the current-fed (CF) single-phase qz-source inverter, and Fig.1(b) is the semi-q Z-source inverter, which is an improved version of Fig.1(a). Both the inverters have the same voltage gain as shown below and require only two active switches to obtain the same maximum voltage gain as the FB inverter shown in Fig.1(a)



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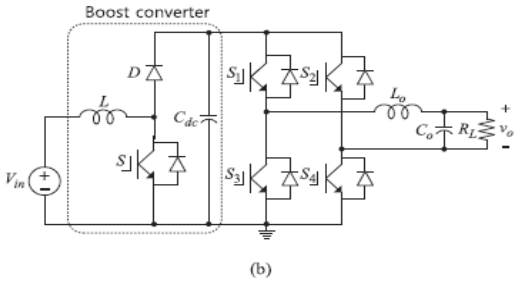

Fig. 1 Conventional single-phase inverters. (a) FB inverter. (b) FB inverter with dc–dc boost converter

$$Vo/Vin=(2D-1D)/D \qquad (1)$$

In (1), *D* is defined as the duty ratio of switch *S*2 .As shown in Fig.1, the two topologies share common grounds between *V*in and *vo*, and thus they can minimize the possible ground leakage current problem effectively when they are used for PV inverter. However, as depicted in Fig1(c), their attainable maximum voltage gain is limited to 1, which means that they are not suitable for applications where input voltage is low. In order to overcome the limitations of Fig.1 while maintaining the doubly ground features, a three-switch three-state single-phase Z-source inverter (TSTS-ZSI) was introduced in. Fig.2 shows the boost-based TSTS-ZSI and buck-boost based TSTS-ZSI, respectively. The inverters can have higher voltage gain than 1, and they comprise three switches, three capacitors, and three inductors. Although higher voltage gain is obtained, the three inductors (*L*1, L2, and *L*3) in the TSTS-ZSI make the circuit a bit bulky and heavy. In addition, the switch signals of the inverter are all different and relatively complicated.

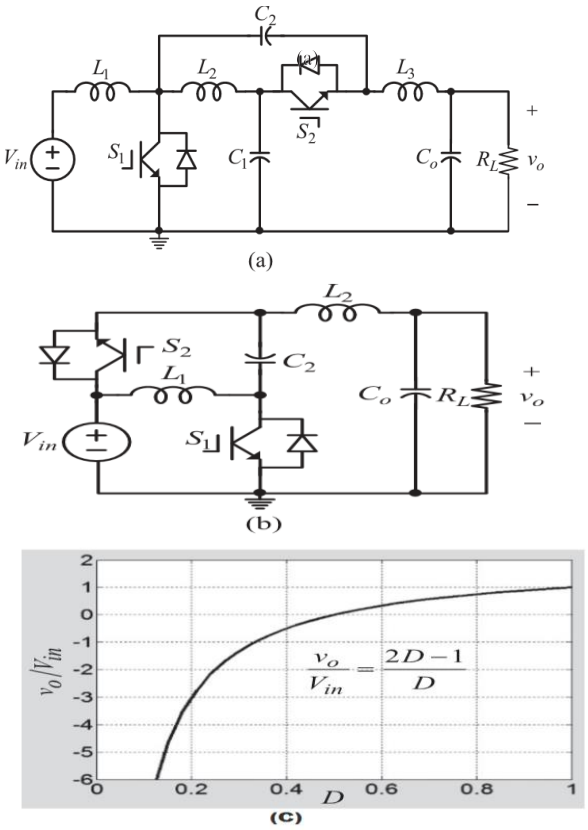

Fig.2. Single-phase qZ-source inverters. (a) Single-phase CF-qZ-source inverter. (b) Semi-qZ-source inverter. (c) Voltage gain.

Although higher voltage gain is obtained, the three inductors (L_1,L_2, and L_3) in the TSTS-ZSI make the circuit a bit bulky and heavy. In addition, the switch signals of the inverter are all different and relatively complicated.

In this paper, a single-phase switched-coupled-inductor dc– ac inverter is proposed. Similar to the TSTS-ZSIs, the proposed inverter can obtain higher voltage gain than the circuits in Fig. 2 and maintains same ground between V_{in} and v_o. The proposed inverter also requires three active switches, but all the induc- tors in the circuit can

be coupled together, which will lead to more compact and cost effective solution than the TSTS-ZSI. In addition, the switch signal generation is relatively simpler than the TSTS-ZSI. A 280-W prototype inverter is built and its performances are verified through experiment.

II. RELATED WORK

A conventional HVDC system uses an ac line frequency (50/60 Hz) transformer to boost the voltage and ac/dc converters for rectification and power flow control. This technology is robust and reliable, but it causes a considerable increase in weight and volume, which leads to higher installation cost. A high-power density can be obtained by replacing the bulky 50/60-Hz transformers with high-frequency transformers. Unfortunately, high-frequency transformers with large turn ratios are difficult to design at high voltages and mega power levels because of the enormous expense of the magnetic material, core, and dialectic losses. One of the key-enabling components for HVDC is the high power dc/dc conversion system because it has a rigid structure, is easy to control system and more compact. To overcome the increasing power losses and maintain a high power density, it is expected that large marine turbines will require a higher voltage with high-voltage gain dc/dc conversion systems to interface with the power transmission networks. Single-module dc/dc boost converters can theoretically achieve infinite voltage conversion ratios but practically, the maximum gain is limited by circuit imperfections, such as parasitic elements and switch commutation times. Multiple module boost converters have been proposed to achieve high conversion ratios for applications to offshore wind farms. Nevertheless, because the duty ratio of the main switch is large to achieve high-voltage gain, the switching frequency is relatively low to reduce the losses and also allows sufficient turn-off time for the switches.

2.1 PROBLEM FORMULATION

Therefore, increasing the size of passive elements, such as boost inductors and filter capacitors, is inevitable due to the low switching frequency. Recently, the common types of switched-capacitor (SC) converters are considered as an attractive solution for meeting the requirements, such as high-power density and control simplicity. In, a resonant SC (RSC) converter was investigated, where an extra inductor was added to form a sinusoidal manner with the capacitors to perform a soft switching. In, a multilevel RSC topology was proposed with significant benefits, including a modular structure, low-voltage stress of the switches, and reduced switching loss. On the other hand, the large number of capacitors, high passive component losses, and inevitably large physical size of the converters has limited the use of these topologies in high-voltage gain offshore wind energy systems. A 55-kW 3× (the output voltage is three times the input voltage) flying-capacitor dc/dc converter was introduced for hybrid electric vehicles. The major drawbacks are the non-modular structure, complicated switching scheme, and low-voltage gain. An RSC voltage tripler with interleaving capability and high efficiency was presented in. Nevertheless, it still has several problems including the passive component counts when a high-voltage gain is required for high-power applications due to the low-voltage conversion ratio of the circuit. To solve the problems listed previously; this paper presents a new high-gain RSC dc/dc converter for offshore wind energy

systems. The proposed converter combines the output of two modular cells to reduce the device count, output capacitance requirements, and total capacitor power rating. The principle of a soft-switching operation and output voltage analysis of the proposed converter are described in detail. The output capacitors are charged and discharged continuously by a 180◦ phase shift with respect to each other to eliminate the output voltage ripples without adding extra component.

2.2 OBJECTIVE OF THE THESIS

In this thesis, a single-phase switched-coupled-inductor dc–ac inverter is proposed. Similar to the TSTS-ZSIs, the proposed inverter can obtain higher voltage gain than the circuits in Fig. 2 and maintains same ground between *V*in and *vo*. The proposed inverter also requires three active switches, but all the inductors in the circuit can be coupled together, which will lead to more compact and cost effective solution than the TSTS-ZSI. In addition, the switch signal generation is relatively simpler than the TSTS-ZSI. A 280-W prototype inverter is built and the performance of the proposed method is evaluated through simulations in MATLAB/SIMULINK environment.

III. PROPOSED SYSTEM

The proposed inverter and it takes similar structure with the single-phase CF-qZ-inverter shown in Fig.3. Compared with Fig.2, the proposed inverter has an additional switch (Sx), capacitor (Cx), and inductor (L2) coupled with inductor L1. The inductors L1 and L2 are coupled with 1: n turn's ratio and all the inductors in the proposed topology can be coupled altogether as will be discussed in Section III. The added 1: n coupled inductor contributes to the increase of voltage gain. Although the leakage inductance of the coupled inductor may induce a voltage spike across switch S1, this is not a major problem because such a voltage spike and the voltage of S1 are low. In Section III, it will be found that the voltage stress of S1 is always half of S2 or Sx if leakage inductance is not considered. Therefore, as long as the voltage overshoot caused by the leakage inductance is not so high, the voltage stress of S1 will be less than that of S2 and there is not much problem in selecting switching device for S1. On the other hand, the leakage inductance is beneficial in limiting the current passing through Cx. Switches S1 and S2 are complementary as in the single-phase qZ-source inverter and the switch Sx is synchronized with S1. A. Mode Analysis of the Proposed Inverter Fig.4.2 shows operation of the proposed inverter and there are two operational modes during one switching cycle. In mode 1, switches S1 and Sx are turned-on, and S2 is turned-OFF. In mode 2, switches S1 and Sx are turned-OFF, and S2 is turned-on. Followings are the detailed mode analysis of the proposed inverter. In mode 1, the capacitor Cx is charged to (n + 1) Vin. Since the Cx is being charged and discharged during one switching period, its voltage has ripple and the ripple voltage depends on the output power. Therefore, when the voltage difference between (n + 1)Vin and Cx is high, relatively high surge (charging) current will flow through Vin − Dx (Sx) − L2 − Cx − S1 and the switching devices in this path (Sx and S1) can be damaged. In order to limit the high surge current, a current limiting inductor is necessary.

In this project, the leakage inductance generated by the coupling of L1 and L2 serves as the current limiting inductor.

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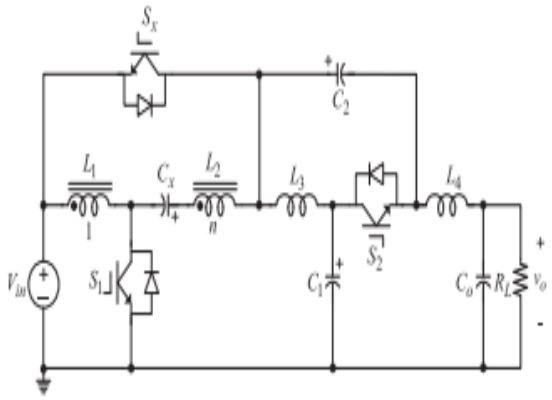

Fig 3 Proposed dc–ac inverter

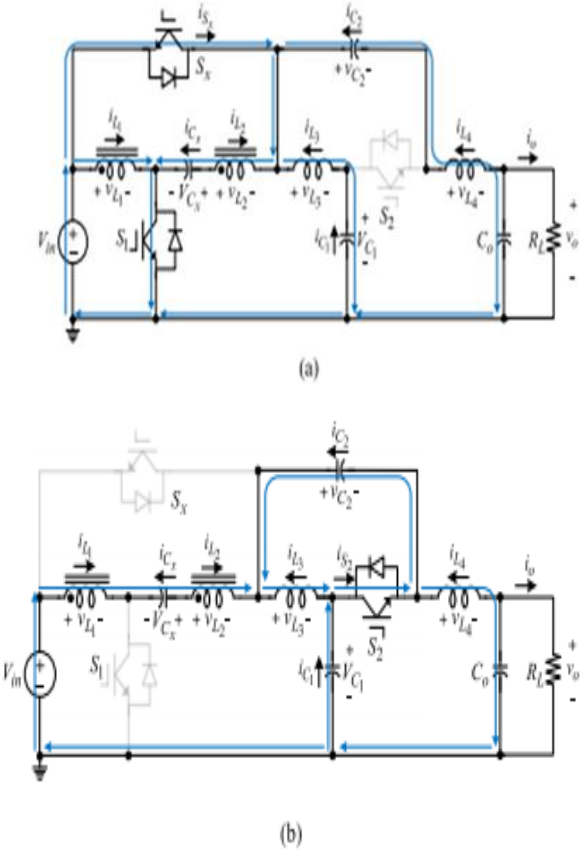

Fig. 4 Mode analysis of the proposed inverter. (a) Mode 1: S1 and Sx are ON, and S2 is OFF. (b) Mode 2: S1 and Sx are OFF, and S2 is ON.

In mode 2, capacitor Cx is discharged by the inductor current, iL1. From Fig. 4(b), the voltage and current relations in mode 2 are derived as follows:

$$V_{C_x} = V_{\text{in}} + v_{L_2} = (n+1)V_{\text{in}} \tag{2}$$

$$\begin{cases} v_{L_1} = V_{\text{in}} \\ v_{L_3} = V_{\text{in}} - V_{C_1} \\ v_{L_4} = V_{\text{in}} - v_{C_2} - v_o \end{cases} \tag{3}$$

$$\begin{cases} i_{C_1} = i_{L_3} \\ i_{C_2} = i_{L_4} \\ i_{C_x} = i_{\text{in}} - i_{L_1} + i_{L_3} + i_{L_4} \end{cases} . \tag{4}$$

In mode 2, capacitor Cx is discharged by the inductor current, iL1. From Fig. 4(b), the voltage and current relations in mode 2 are derived as follows:

$$\begin{cases} (1+n)v_{L_1} = V_{\text{in}} + V_{C_x} - v_{C_2} - V_{C_1} \\ v_{L_3} = v_{C_2} \\ v_{L_4} = V_{C_1} - v_o \end{cases} \tag{5}$$

$$\begin{cases} i_{C_1} = -i_{L_1} - i_{L_4} \\ i_{C_2} = -i_{L_1} - i_{L_3} \\ i_{C_x} = -i_{L_1} \end{cases} . \tag{6}$$

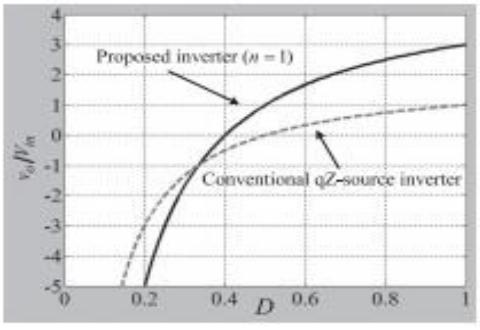

Fig. 5 Voltage gain comparison

From the aforesaid equations, voltage relations are derived as follows

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$$V_{C_1} = v_{C_2} + v_o \quad (7)$$

$$V_{C_1} = (n+2)V_{\text{in}}. \quad (8)$$

From the flux (volt–second) balance condition on L3, the capacitor C2 voltage is derived as follows:

$$v_{C_2} = \frac{(1-D)(n+1)}{D} V_{\text{in}} \quad (9)$$

Where D is the duty cycle of switch S2. By using (7)–(9), the voltage gain of the proposed inverter is derived as follows:

$$\frac{v_o}{V_{\text{in}}} = \frac{(2n+3)(2D-1)+1}{2D} \le n+2. \quad (10)$$

Fig. 5 shows the voltage gain of the proposed inverter when n = 1 and compared with the conventional inverters shown in Fig.2(c). It is found that the proposed inverter has a higher voltage gain than the conventional inverters shown in Figs. 1(a) and 2. According to the charge balance condition on Cx , C1 , and C2 , the inductor currents averaged in one switching period are derived as follows:

$$i_{L_{1\_avg}} = \frac{(2D-1)(n+1)}{D} i_o \quad (11)$$

$$i_{L_{2\_avg}} = 0 \quad (12)$$

$$i_{L_{3\_avg}} = i_{L_{4\_avg}} = -i_o \quad (13)$$

$$i_{S_{2\_avg}} = i_{S_{x\_avg}} = i_o. \quad (14)$$

Currents of inductors L1 and L2 are different in respective mode unlike inductor currents iL3 and iL4 . In mode 1, where current ripple is ignored, they are derived

$$i_{L_1} = \frac{(2D-1)(n+1-D)}{D(1-D)} i_o \quad (15)$$

$$i_{L_2} = -\frac{(2D-1)}{(1-D)} i_o. \quad (16)$$

In mode 2, they are expressed as follows:

$$i_{L_1} = i_{L_2} = \frac{2D-1}{D} i_o. \quad (17)$$

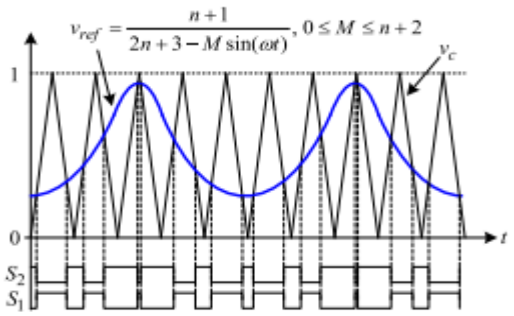

Fig. 6. Gate signal generation of the proposed inverter.

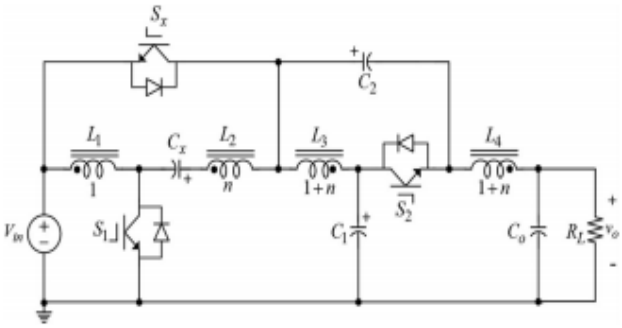

Fig. 7. Circuit topology of the proposed inverter when all inductors are coupled into one core

B. Modulation Scheme of the Proposed Inverter

Modulation scheme of the proposed inverter is the same as that of the single-phase qZ-source inverter. By defining the output voltage of the inverter as

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(18), modulation index (M) of the inverter is derived as follows:

$$v_o = V_m \sin \omega t \qquad (18)$$

$$M = \frac{V_m}{V_{\text{in}}}. \qquad (19)$$

By substituting (18) and (19) into (10), the following duty cycle equation is derived as follows:

$$D = \frac{n+1}{2n+3-M\sin(\omega t)}, \ (0 \le M \le n+2). \qquad (20)$$

When n = 1 and M = 3, the duty cycle range of the proposed inverter is 0.25–1.0. Fig.6 represents the gate signal generation of the proposed inverter. When reference signal (vref) is greater than the carrier signal (vc), switch S2 is turned on and switch S1 is turned OFF.

4.2 MAGNETIC INTEGRATION OF INDUCTORS AND COMPARISON

A. Magnetic Integration of Inductors As discussed in Section II, the L1 and L2 are coupled with 1: n ratio to obtain higher voltage gain. In this section, it is revealed that all the four inductors (L1, L2, L3, and L4) in the proposed inverter can be coupled using one magnetic core.

TABLE I
DEVICE STRESS OF THE PROPOSED INVERTER

	Voltage stress	Current stress
S_1	$\frac{2n+3+M}{2M}V_o$	$\frac{(2n+3-M)(M-1)}{n+2-M}I_o$
S_2	$\frac{2n+3+M}{M}V_o$	$\frac{2n+3+M}{n+1}I_o$
S_x	$\frac{2n+3+M}{M}V_o$	$\frac{2n+3-M}{n+2-M}I_o$

Table: 1 Device stress of the proposed inverter

The previous analysis shows that the voltages across each inductor during mode 1 are as follows:

$$\begin{cases} v_{L_1} = V_{\text{in}} \\ v_{L_2} = nV_{\text{in}} \\ v_{L_3} = V_{\text{in}} - V_{C_1} = -(n+1)V_{\text{in}} \\ v_{L_4} = V_{\text{in}} - v_{C_2} - v_o = -(n+1)V_{\text{in}} \end{cases}. \qquad (21)$$

Similarly, the voltages across each inductor during mode 2 are as follows:

$$\begin{cases} v_{L_1} = \frac{1}{n+1}(V_{\text{in}} + V_{C_x} - V_{C_1} - v_{C_2}) = -\frac{1}{n+1}v_{C_2} \\ v_{L_2} = -\frac{n}{n+1}v_{C_2} \\ v_{L_3} = v_{C_2} \\ v_{L_4} = V_{C_1} - v_o = v_{C_2} \end{cases}. \qquad (22)$$

From (21) and (22), it is found that regardless of the operating mode, the four inductors in the proposed inverter have the following voltage relationships:

$$v_{L_1} : v_{L_2} : v_{L_3} : v_{L_4} = 1 : n : -(n+1) : -(n+1). \qquad (23)$$

Therefore, all the inductors can be coupled using one core, which leads to significant reduction in magnetic volume and converter size. It should be noted that n is the turns ratio and it is not the real number of turns. Fig.7 shows the final completed circuit of the proposed inverter with the inductor polarity dots marked. The operation with magnetic integration is the same as that of the previous analysis in Section II.

B. Comparison of Switch Stress and Others from Fig.5 and (8), (9), (21), (22), voltage stresses of the three switches can be determined. Similarly, the switch current stresses can be determined from (4), (6), (13)–(17) and Fig.5. Table I shows maximum switch stress of the proposed inverter. Table II compares the

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proposed inverter when n = 1 with the boost based TSTS-ZSI shown in. k is maximum of modulation index. Although the buck–boost-based TSTS-ZSI has lower device stresses, it has drawbacks like more complicated gate signal generation, discontinuous input and output current, and requires additional LC filter that builds the circuit structure more complex and large inductor. For these reasons, the boost-based TSTS-ZSI is compared with the proposed inverter. From the result of Table II, it is evident that the overall voltage and current stresses of the proposed inverter are greater than those of the TSTS-ZSI and the proposed inverter requires one more capacitor. However, current stress of the proposed inverter is lower than that of the boost-based TSTS-ZSI when M is lower than 2.4. Moreover, the proposed inverter can reduce the magnetic volume through the coupling of all separate inductors

TABLE II
COMPARISON OF INVERTERS

		Proposed inverter ($n=1$)		Boost based TSTS-ZSI ($k=3$)	
		Voltage stress	Current stress	Voltage stress	Current stress
S_1		$\frac{5+M}{2M}V_o$	$\frac{(M-1)(5-M)}{3-M}I_o$	$\frac{5}{M}V_o$	$(M+2)I_o$
S_2		$\frac{5+M}{M}V_o$	$\frac{5+M}{2}I_o$		
S_x			$\frac{5-M}{3-M}I_o$		
No. of capacitors		4		3	
No. of inductors		1 (coupled inductor)		3 (discrete inductors)	
Current	Input	Quasi-continuous		Continuous	
	Output	Continuous		Discontinuous	
Gate signal generation		Relatively simple		Complex	
$\Delta i_{L_{\max}}$		$\Delta i_{L_1}=\Delta i_{L_2}=\frac{(3+M)(1+M)}{(5+M)^2}\times\frac{V_{in}T_s}{L_1}$, $\Delta i_{L_3}=\Delta i_{L_4}=\frac{4(3+M)}{(5+M)^2}\times\frac{V_{in}T_s}{L_3}$ ($L_1=L_2$, $L_3=L_4$)		$\Delta i_{L_f}=\frac{4}{5}\times\frac{V_{in}T_s}{L_f}$, $\Delta i_{L_1}=\Delta i_{L_2}=\frac{5}{4}\times\frac{V_{in}T_s}{L_{1,2}}$ ($L_1=L_2$)	
$i_{L_{avg}}$ (one switching period)		$i_{L_1\_avg}=I_o(M\sin(\omega t)-1)$, $i_{L_2\_avg}=0$, $i_{L_3\_avg}=i_{L_4\_avg}=-I_o\sin\omega t$		$i_{L_f\_avg}=I_oM\sin\omega t$, $i_{L_1\_avg}=i_{L_2\_avg}=I_o\sin\omega t$	
$V_{C_{\max}}$		$V_{C_x}=\frac{2}{M}V_o$, $V_{C_1}=\frac{3}{M}V_o$, $V_{C_2}=\frac{3+M}{M}V_o$		$V_{C_1}=V_{C_2}=\frac{5+M}{2M}V_o$	

Table: 2. Comparison of inverters

Comparison of maximum current ripple, average current, and maximum capacitor voltage is summarized in Table II. According to the Table II, when compared with the boost-based TSTS-ZSI, the inductor current ripples of the proposed inverter are reduced by more than 2 due to coupling effect. In Table II, L1 and L3 of the proposed inverter are self-inductances of the coupled inductor. In addition, self-inductances L1 and L2 of the proposed inverter are the same and L3 and L4 are also the same when all inductors are coupled with n = 1. The boost based TSTS-ZSI is

assumed that L1 and L2 are equal. Although, the C2 capacitor voltage of the proposed inverter is greater than that of the boost-based TSTS-ZSI, the capacitor voltages of Cx and C1 in the proposed converter are lower than those of the boost-based TSTS-ZSI. Moreover, inductor has more influence on size and weight than capacitor. The average inductor currents of the proposed inverter and boost-based TSTZ-ZSI in one switching period are almost the same. In conclusion, the proposed inverter can reduce overall magnetic volume because lower inductance is required. In addition, the boost-based TSTS-ZSI should have large output capacitor because of discontinuous output current. Moreover, the gate signal generation of the proposed inverter is much simpler than that of the TSTS-ZSI.

TABLE III
ELECTRICAL SPECIFICATIONS OF THE PROPOSED INVERTER

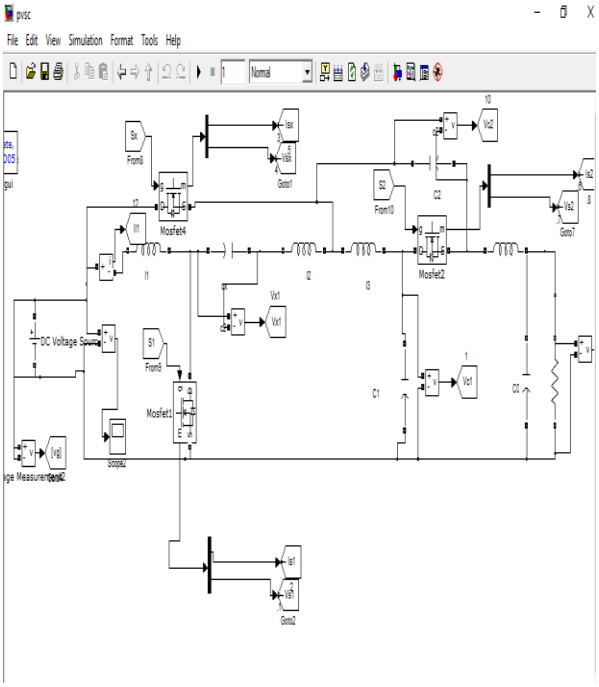
Output power	280 W
Input voltage	62 Vdc
Output voltage	110 Vrms / 60 Hz
Switching frequency	20 kHz
IGBT (S_x , S_1 , S_2)	FGH40N60
Coupled inductor	
Core	EE7066
Inductance (L_1 , L_2)	60 uH
Inductance (L_3 , L_4)	240 uH
Capacitance (C_x , C_1)	100 uF
Capacitance (C_o)	4.4 uF

Table: 3. Electrical specifications of the proposed inverter

IV. SIMULATION RESULTS

Simulation results proposed a New single- Phase Switched- coupled- Inductor DC-AC Inverter for Photovoltaic Systems. The simulated system is shown in fig.5.1. Simulation studies are carried out in the MATLAB/SIMULINK environment.

4.1 PROPOSED TOPOLOGY



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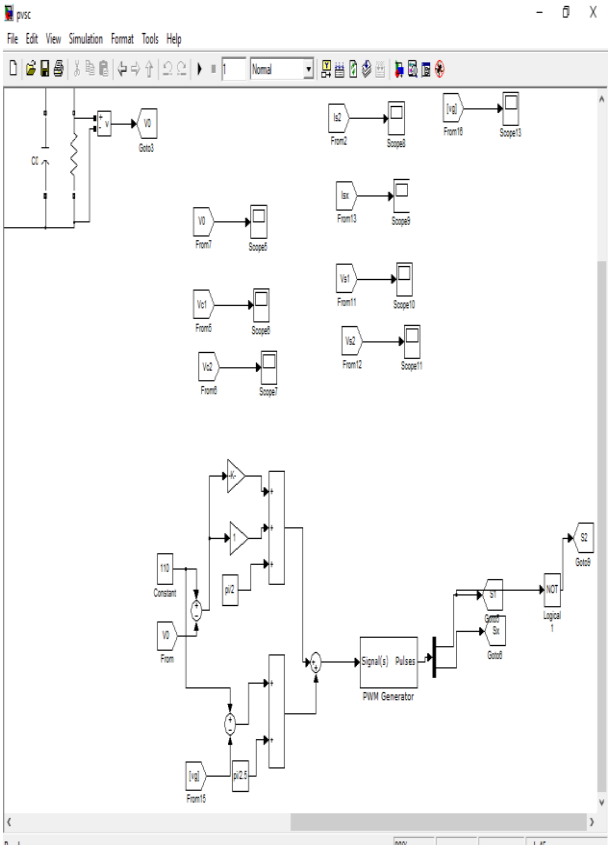
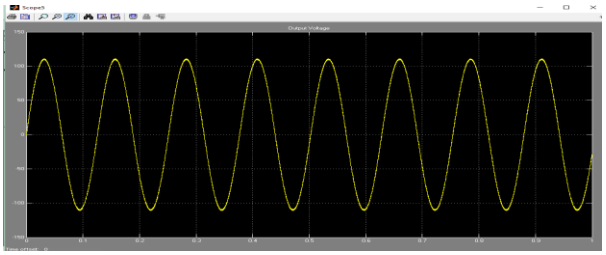


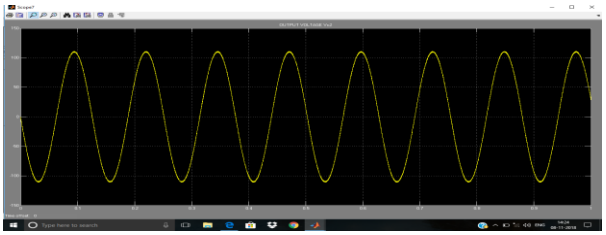
Fig 8: Block diagram for proposed methodology

SIMULATION RESULT ANALYSIS

A 280-W prototype inverter is built and tested. Detailedelectrical specifications of the proposed inverter are summarized in Table III. As already mentioned in Section II, a relatively small current limiting inductor is required in the path Vin −Dx (Sx) − L2 −Cx −S1 to limit the high surge current. In the proposed circuit, the leakage inductance (about 300 nH) generated by coupling of L1 and L2 is used for this purpose. Followings are the experimental waveforms of the proposed inverter when Vin = 62 V,M= 2.5, and Po = 280 W. Fig.9 shows the experimental wave form of the output voltage and the capacitor C2 voltage. Figs. 9 and 10 show the voltages across all switches (VSx, VS1, and VS2). As expected, there is voltage overshoot in switch S1 caused by the leakage inductance and there are no noticeable overshoots in the switches S2 voltage varying with D, the voltages across C1 and Cx are almost constant and they are fixed to 3Vin and 2Vin, respectively. Figs. 5.5 and 5.6 show current waveforms. Shows the efficiency of the proposed inverter tested with Vin = 62V with output power varies.

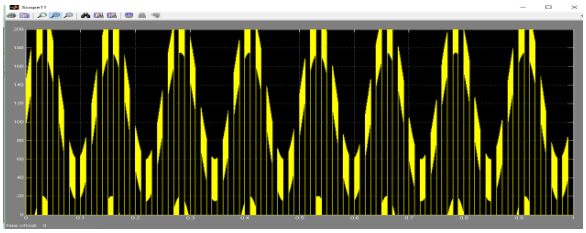


(a) Output voltage V0



(b) Output Voltage Vc2

Fig 9: Simulink waveforms of the proposed inverter (Vc2, V0)



(a) Output Voltage Vs2

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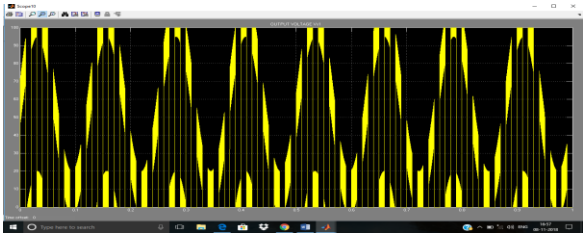
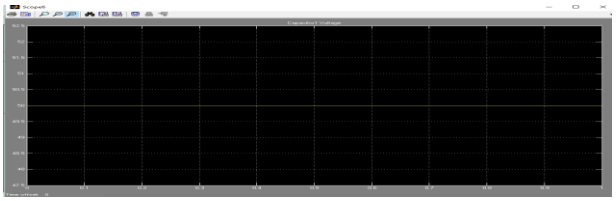
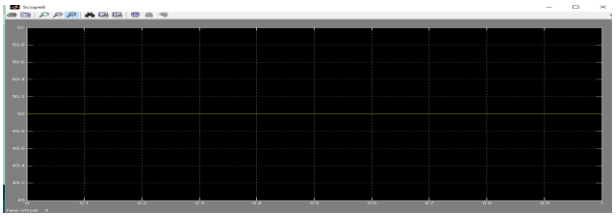


(b) Output Voltage Vs1

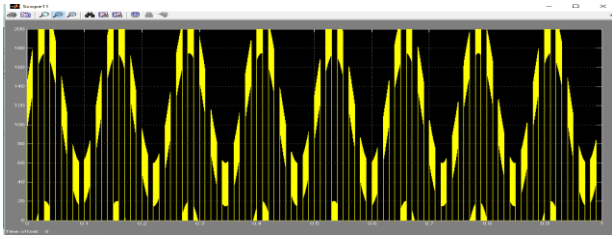
Fig 10 : Simulink waveforms of the proposed inverter (Vs2, Vs1)



(a) **Output Voltage Vc1**

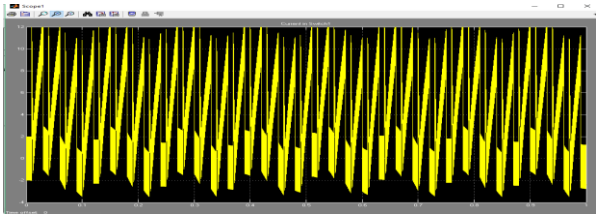


(b) Output Voltage Vc1

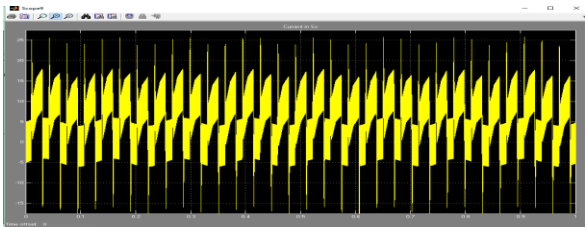


(c) Output Voltage(Vs2)

Fig 11: Simulink waveforms of the proposed inverter (Vc1, Vc1, Vs2)

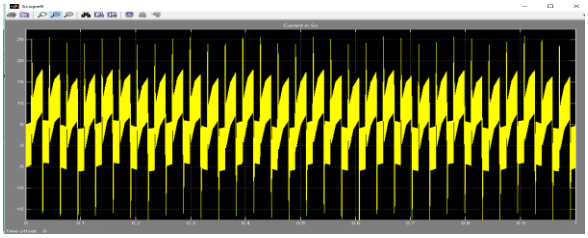


(a) Output Current Is1

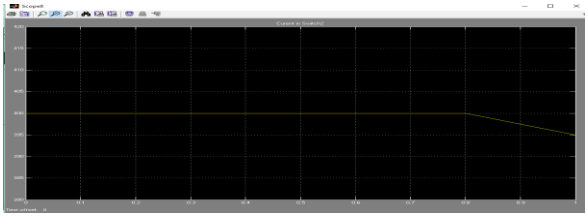


(b) Output Current Isx

Fig 12: Simulink waveforms of the proposed inverter current waveforms (Is1, Isx)

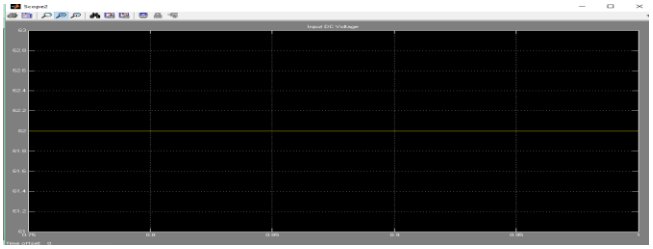


(a) Output Current Isx

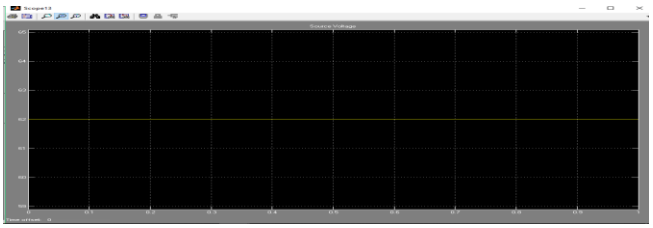


(a) Output Current Is2

Fig 13: Simulink waveforms of the proposed inverter switching current waveforms (Isx, Is2)



Input DC waveforms



Output Voltage (Vg)

Fig 14: Simulink waveforms of the proposed inverter (Input DC waveform, Output Voltage (Vg))

V. CONCLUSIONS

In this project, the single-phase switched coupled inductor dc– ac inverter was presented. It has an operation principle similar to that of a single-phase qZ-source inverter. With the addition of components Sx, Cx, and the coupled inductor, voltage gain of the proposed inverter can be extended to greater than 2. The magnetic integration of all inductors decreases the converter volume significantly and the proposed inverter has relatively simple gate signal generation. Moreover, similar to the single-phase qz- source inverter and the TSTS-ZSI, the proposed inverter shares common grounds between the dc input and the ac output voltage. A 280-W prototype inverter was built and tested to verify operation of the proposed inverter.

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