International Journal of Research
Available at https://pen2print.org/index.php/ijr/
e-ISSN: 2348-6848
p-ISSN: 2348-795X
Volume 05 Issue 23
December 2018

Design of High Speed ALU Using Adaptive Logic

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Abstract:

In this paper, we introduce high speed architecture for 32-bit ALU using Adaptive logic technique. Adaptive logic is one of the fastest and innovative logic that has been implemented in digital circuit . Adaptive logic is implemented using the CMOS technology. It works very effectively in both threshold and sub – threshold regions which uses Timing-error-detection (TED)-based systems is been shown to reduce power consumption or increase yield due to reduced margins. Reducing voltage in the circuit results in slow operation that incurs more delay. Generally delay is caused due to slow operation that results in error based upon the conditions. Canary circuit has been designed for error detection and error correction approach for reducing the power and voltage in a digital circuit. Adaptive logic, which is nothing but modified canary circuit with add-on components to canary circuit have been designed with dual latch phase in each stage. A combination of XOR gate and flip-flop around each stage is added for the verification of correct operation. The entire architecture was modeled using Verilog HDL with the help of XILINX ISE tool.

Keywords

TED,EDS, XOR.

1. Introduction

Day by day IC technology is getting more complex in terms of design and its performance analysis. A faster design with low power consumption and small area is implicit to modern electronic devices. In VLSI, Energy efficiency has emerged as a critical design requirement. In order to obtain the maximum power savings it is essential to scale the Maximum possible supply voltage that results in correct operation. Means if there is insufficient voltage to the circuit the process of operation of that circuit will be slow so if we give sufficient voltage correct operation will be observed in the circuit. Many energy efficient design techniques have been proposed in an efficient way of reducing energy consumption. Reducing voltage in the circuit results in slow operation that incurs more delay (main drawback of reducing voltage).Every day new approaches are being developed to design low-power at technological, physical, circuit and logic levels. Several techniques such as pipelining, parallel processing have been proposed to allow large reduction in voltage. But these techniques involve sequential elements into the circuit and divide a particular task into 'N' subtasks these results in large area design. To reduce the area new technique named timing margin is been implemented to overcome those drawbacks in the previous method. A major challenge in timing margin reduction methodologies is the increased probability of timing errors due to variations. In general, the variations can be categorized into two types:

1) spatial and
2) temporal variations.

Transistors on a die experience two types of spatial variations:

1. Global variation
2. Local variation

Global variation mostly affects the electrical characteristics of the devices on a die in the same way. On the other hand, local variation affects the transistor characteristics in more unpredictable way due to randomness. Temporal variation also has two types.

1. Static variation
2. Temporal variation

The amount of static variations is decided during the fabrication period and it does not change with time. On the other hand, temporal variation occurs due to environmental changes, such as temperature, supply voltage noise, and aging cause the transistors to experience variability depending on time. To accommodate the potential increase in circuit delay caused by the variations, more timing margin is given in traditional design approaches. In this, when performance of circuits is compared, it is always done in terms of circuit speed, size and power. A good estimation of the circuit's size is to count the total number of gates used. The actual chip size of a circuit also depends on how the gates are placed on the chip – the circuit's layout. Since we do not deal with layout in this report, the only thing we can say about this is that regular circuits are usually smaller than non-regular ones (for the same number

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of gates), because regularity allows more compact layout. The physical delay of circuits originates from the small delays in single gates, and from the wiring between them. The delay of a wire depends on how long it is. Therefore, it is difficult to model the wiring delay; it requires knowledge about the circuit's layout on the chip. The gate delay however, can easily be modelled by saying that the output is delayed a constant amount of time from the latest input. What we can say about the wiring delay is that larger circuits have longer wires, and hence more wiring delay. It follows that a circuit with a regular layout usually has shorter wires and hence less wiring delay than a non-regular circuit. Therefore, if circuit delay is estimated as the total gate delay, one should also have in minded the circuit's size and amount of regularity, when comparing it to other circuits. "Delay" usually refers to the "worst-case delay". That is, if the delay of the output is dependent on the inputs given, it is always the largest possible output delay that sets the speed. Furthermore, if different bits in the output have different worst case delays, it is always the slowest bit that sets the delay for the whole output. The slowest path between any input bit and any output bit is called the "critical path". If a circuit is to be speed up, it is always the critical path that should be attacked in the first place.

2. Block Diagram :

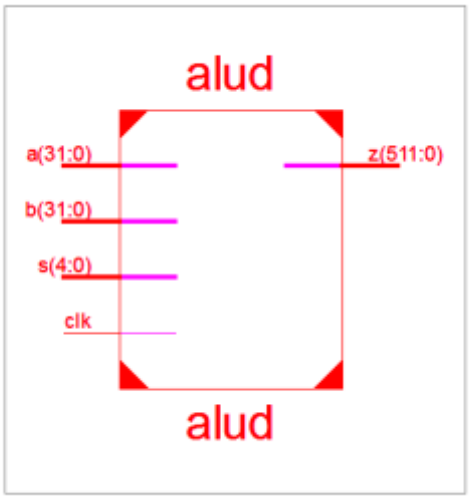

Figure1: block diagram of ALU

An ALU is a combinational logic circuit, meaning that its outputs will change asynchronously in response to input changes. In normal operation, stable signals are applied to all of the ALU inputs and, when enough time (known as the "propagation delay") has passed for the signals to propagate through the ALU circuitry, the result of the ALU operation appears at the ALU outputs. The external circuitry connected to the ALU is responsible for ensuring the stability of ALU input signals throughout the operation, and for allowing sufficient time for the signals to propagate through the ALU before sampling the ALU result.

3. Working:

The architecture of design of high speed ALU circuit using adaptive logic For every circuit, DELAY is the common problem. To avoid that canary circuit or replica circuits are used to target the delay of the real critical path with some added margins. Drawback of canary or replica circuit Replica circuit is a collection of digital gates with some tune able delays. This is suitable for only small pipeline stages, when the stages number increases local variations at threshold and sub threshold voltage cause significant delay in replica path and actual path. To overcome the above problem TED circuit is introduced.

TED based system works more effective in largely removing the variation incurred in timing margins. This technique has the benefit of tracking real path delay that is not possible in replica circuits.TED system is EDS(Error-Detection-Sequential) circuit which generate error signals when the path setup fails. In this system, TEP designed with combination of TED with Time Borrowing(TB)Combining TED with TB into TEP (Time Error Prevention) system will be produced that can tolerate late coming signals that doesn't requires any additional circuitry. TED+TB = TEP which is more effective than conventional TED. In proposed concept EDS system circuitry is composed in several pipeline stages which are embedded parallel. Dual latch phase is considered to every stage at both input and output for the purpose of time borrowing. Output from any stage may be late again and time is borrowed from n+1 stage.

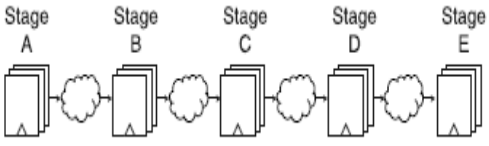

Figure2: 5Stage circuit

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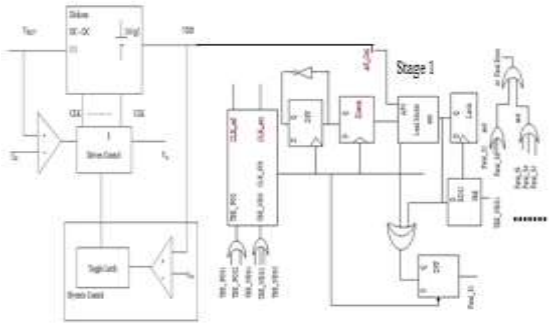

Figure3: Adaptive Logic Circuit

A combination of XOR gate with flip flop around every stage is added for verification of correction operation. Delay can be recovered by using TB technique. Time is borrowed from n+1 stage and that will be recovered at the output with out any delay. If the particular circuit is suffering from delay it automatically traces the delay and reduce the delay .Combination of XOR gate and flip flop around each stage is added for verification of correct operation .Due to above operation in every stage and the delay gets reduced by using that operation

4. **Results**:

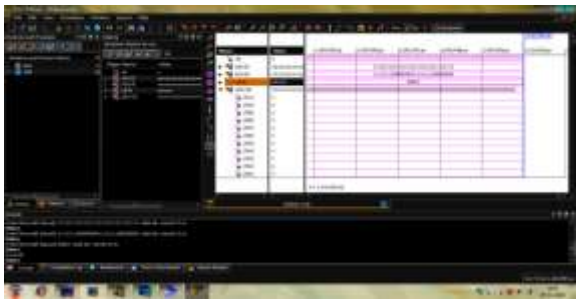

Figure4: simulation result of 32-bit ALU

Figure5: simulation result of 32-bit ALU connected to Adaptive circuit

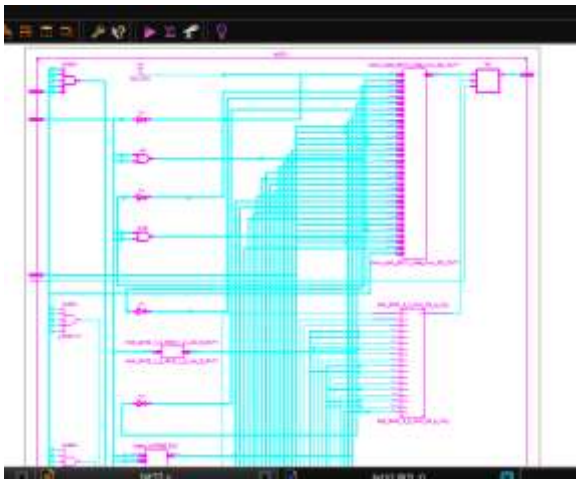

Figure6: RTL schematic of ALU

Figure7: Technology Schematic View of ALU

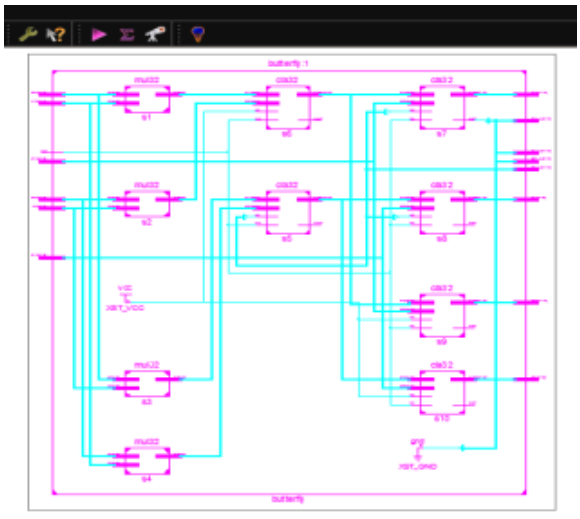

Figure8 :RTL Schematic View of32-bit ALU connected to Adaptive circuit

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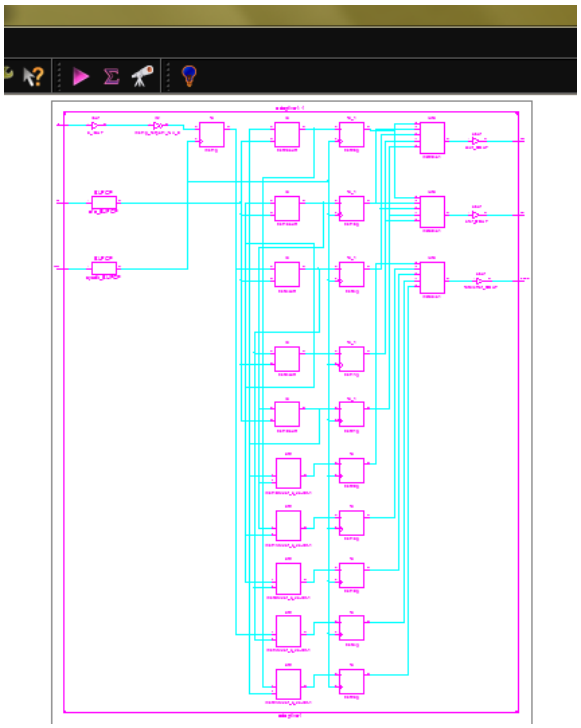

Figure9: Technology Schematic View of 32-bit ALU connected to Adaptive circuit

4.1. Timing Details Of ALU:

Timing constraint: Default OFFSET OUT AFTER for Clock 'clk'
Total number of paths / destination ports: 512 / 512

Offset: 4.395ns (Levels of Logic = 1)
Source: z_511 (LATCH)
Destination: z<511> (PAD)
Source Clock: clk falling
Data Path: z_511 to z<511>

Cell:in->out	fanout	Delay	Gate Delay	Net Logical Name (Net Name)
LD:G->Q	2	0.676	0.447	z_511 (z_511)
OBUF:I->O		3.272		z_511_OBUF (z<511>)

Total 4.395ns (3.948ns logic, 0.447ns route)
(89.8% logic, 10.2% route)

4.2Timing Details Of Adaptive Connected ALU

Timing constraint: Default OFFSET OUT AFTER for Clock 'clk'
Total number of paths / destination ports: 512 / 512

Offset: 0.811ns (Levels of Logic = 1)
Source: z_510_1 (LATCH)
Destination: z<511> (PAD)
Source Clock: clk falling
Data Path: z_510_1 to z<511>

Cell:in->out	fanout	Delay	Gate Delay	Net Logical Name (Net Name)
LDE:G->Q	1	0.472	0.339	z_510_1 (z_510_1)
OBUF:I->O		0.000		z_511_OBUF (z<511>)

Total 0.811ns (0.472ns logic, 0.339ns route)
(58.2% logic, 41.8% route

Table1: Comparison of Delay

Structure	Delay
32-bit ALU	**4.395ns**
32-bitALU connected to adaptive circuit	**0.811ns**

The delay of the proposed method is decreased with compare to others. So the proposed method attained speed in the circuit.

5. Conclusion

Insufficient supply voltage to the circuit causes delay in the circuit and results in incorrect outputs. In order to supply sufficient voltage SC DC-DC converter is used. Delay is generally caused due to errors, to reduce those errors canary circuit is designed to reduce the errors in single shot without the usage of stages. But by using dual latch phase to the circuit the performance of the circuit is improved than the previous method. By using dual latch phase, canary circuit and a combination of X-OR gate with flip flop

around every stage is added for verification of correction operation results in improved output than the previous method Delay in 32bit ALU is 4.39ns.This delay is reduced by utilizing proposed Adaptive logic here we are achieving 0.811 ns delay with same output.

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