

A New Five-Phase Coupled Inductor Inverter With SVPWM Method for Common-Mode Voltage Reduction

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ABSTRACT-In this paper, two carrier-based pulse-width-modulation techniques are proposed to reduce the common-mode (CM) voltage generated by the five-phase inverter using space vector pulse width modulation. This work presents multi-carrier interleaved PWM strategies to control common mode voltage (CMV) in three phase coupled inductor inverter (CII). In this paper Space vector modulation (SVM) algorithm is used for the control of pulse width modulation (PWM).[1] It is used for the creation of alternating current (AC) waveforms. Carrier-based pulse-width-modulation techniques are popular due to their simplicity, and have been widely researched for various three-phase inverter configurations. The five-phase inverters have more flexibility in reducing the CM voltage than their three-phase counterparts because they have more phase legs hence finer control over the star-point voltage of the load. Two methods are proposed for the conventional two-level five-phase inverter to reduce the CM voltage; one utilizing adjacent modulating waveforms and the other utilizing non-adjacent modulating waveforms. The coupled inductor inverter (CII) uses coupled inductors to generate multi-level outputs. The proposed methods are further improved to ensure the volt-second integral over each switching period is zero. Moreover, the two proposed methods are designed to reduce switching events and prevent unexpected states occurring during the switching transitions. By using the simulation results we can analyse the performance and the switching strategy of both methods are verified using five-phase coupled inductor inverter.

I. INTRODUCTION

Multiphase inverters have been widely explored in recent decades, primarily as a method to drive multiphase machines [1] [2]. Compared with their three-phase counterparts, multiphase inverters have many advantages such as improved magnetomotive force (MMF) waveform, lower torque pulsation [3], higher torque density [4], and fault tolerance. Common-mode (CM) voltage is one of the side effects in variable speed drive systems with PWM inverters. The high frequency CM voltage produces bearing currents via parasitic capacitance, which deteriorates the insulation, accelerates ageing, reduces the reliability and

ultimately leads to the failure of the machine [7][8]. In this paper Space Vector Modulation (SVM) Technique has become the important PWM technique for three phase Voltage Source Inverters for the control of AC Induction, Brushless DC, Switched Reluctance and Permanent Magnet Synchronous Motors. The study of space vector modulation technique reveals that space vector modulation technique utilizes DC bus voltage more efficiently and generates less harmonic distortion when compared with Sinusoidal PWM (SPWM) technique.

The side effects of the extra components are also apparent: more space is needed for the filters, applications of these filters are limited by the voltage and current ratings and failure probability of the system is increased due to there being more components. Reducing the CM voltage by updating the control strategies is preferred because this does not obviously increase the system cost and with the development of digital control ICs, the algorithms are not confined by limited resources of the previous digital controllers. The CM voltage was firstly researched in two-level inverters. However, as these inverters only have two output levels, the CM voltage can only be reduced with the control strategies rather than eliminated.

Several methods have been proposed to replace the zero vectors with different active vectors and these methods were reviewed in [21] from different aspects. Benefiting from the redundant vectors and extra output voltage levels, the multilevel inverters are able to eliminate the CM voltage. Many methods were proposed for different topologies aimed at eliminating or reducing the CM voltage proposed both space vector modulation (SVM) and sinusoidal pulse-width-modulation (SPWM) methods for the three-phase NPC system. A hybrid PWM method was proposed for open-end winding machine.

Space Vector Modulation (SVM) was originally developed as vector approach to Pulse Width Modulation (PWM) for three phase

inverters. It is a more sophisticated technique for generating sine wave that provides a higher voltage to the motor with lower total harmonic distortion. The main aim of any modulation technique is to obtain variable output having a maximum fundamental component with minimum harmonics. Space Vector PWM (SVPWM) method is an advanced; computation intensive PWM method and possibly the best techniques for variable frequency drive applications. The main objectives of space vector pulse width modulation generated gate pulse are the following.

- Wide linear modulation range
- Less switching loss
- Less total harmonic distortion in the spectrum of switching waveform
- Easy implementation and less computational calculations

A SVM method for a five-level inverter. [25] used predictive current control method for machine drive by only selecting switching vectors with minimum CM voltage to achieve a reduction of the CM voltage. The CM voltage in the multiphase machine drive system was also addressed. [29] The improved control methods are usually based on a star-connected load model, and then the CM voltage can be approximately expressed as the sum of the phase-to-midpoint (of the dc-link) voltages. Therefore, the essence of these methods, although they are proposed for different types of inverters, is similar, which is to choose the switching vectors so that the sum of the phase-to-midpoint voltages is minimum. The coupled inductor inverter (CII) is a competitive member in the family of multilevel inverters. In the three-phase system, the coupled inductors can utilize either three toroidal cores [30] or a more compact three-limb core [32][33].

Compared with the NPC topology [34], the advantages of CII topology are:

1. Fewer components required: to generate the same three-level output voltage, the CII only needs two switches and two diodes with the help of coupled inductor, which means the inverter semiconductor failure rate and the switching loss are reduced;

2. Dead-time is not required: Most voltage source inverters (VSI) have to use dead-time to prevent the shortcircuit of the dc-link, and the downside is obvious—distortion in the load current. However, due to the coupled inductor, the state in which both switches are ON is used to generate the middle level of the output voltage.

3. Low harmonic distortion on the load current: besides the absence of the dead-time, the CII improves the quality of the load current with

the coupled inductor which functions as a filter. Thus, extra filters between the inverter and the machine can be avoided, which reduces the system cost [35].

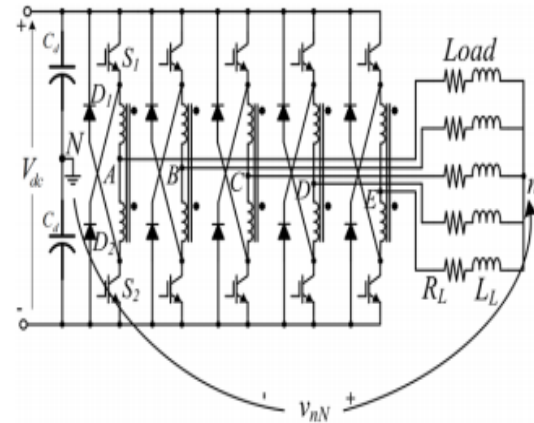


Fig. 1. Topology of the five-phase CII.

In this paper, the reduction of CM voltage is studied in the five-phase CII system with five toroidal cores. Two general carrier-based pulse-width-modulation (CBPWM) techniques are proposed to reduce the CM voltage for the multilevel inverters. Then these two methods are improved to achieve volt-second balance on the magnetic cores, hence they can be applied to the five-phase CII system. This improvement also assures fewest switching events when the balance is achieved.

This paper is organized as follows: firstly, the operating principle of the CII is explained and a CBPWM method is proposed for the normal operation of the single phase leg of the CII; Secondly, two CBPWMs with the reduction of the CM voltage for multiphase multilevel inverters are proposed and improvements of these two CBPWMs are introduced so that they are applicable to the five-phase CII system and the fewest switching events happen in the methods. Finally, the methods are verified by simulations.

FIVE-PHASE COUPLED INDUCTOR INVERTER

Coupled Inductor Inverter

Fig. 1 and Fig. 2(a) show the topology of the five-phase and single-leg coupled inductor inverter (CII). Compared with the NPC topology, the single leg CII only has two switches (e.g. IGBTs or MOSFETs) and two diodes. Effectively, the two inner switches of an NPC phase leg are replaced by a coupled inductor, which enables the CII to produce 0Vdc with reference to the mid-point of the dc-link capacitor, without intentionally making a connection to the mid-point of the dc-link capacitors. This mid-point is also used here as the reference node for the CM voltage. The CII leg is

capable of generating three levels: $-V_{dc}/2$, $0V_{dc}$, and $+V_{dc}/2$.

In three-phase inverters, the cores of the coupled inductors can be either toroidal cores or three-limb cores [30][31]. For the five-phase case, a five-limb core is not an off-the-shelf item, and a customized core will increase the cost of the system. Therefore, in this paper, the coupled inductors are made of five individual toroidal cores. From Fig. 2(a), the following holds:

$$i_0 = i_{up} - i_{dn} \quad (1)$$

where i_0 is the load current, i_{up} is the current in the upper arm of the coupled inductor and i_{dn} the current in the lower arm of the coupled inductor. The currents in the two arms share certain

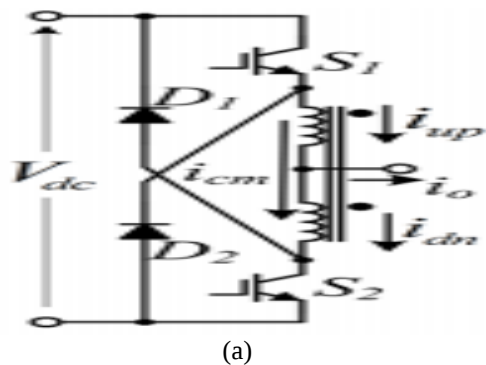


Fig. 2. Four states of one leg of the coupled-inductor inverter: (a) topology of single leg CII; components, including the dc-offset and high frequency component. These components are represented by i_{cm} . The four normal working states are shown in Fig. 2(b)-(e), and the arrows represent the current directions, showing that the CII supports bidirectional current flow.

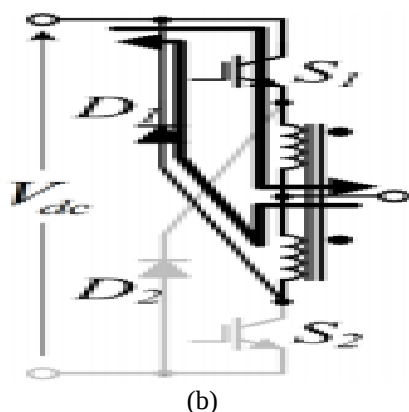


Fig. 2. Four states of one leg of the coupled-inductor inverter: (b) State1: outputs $+V_{dc}/2$ level;

When the phase leg is in State1, Fig. 2(b), the current flows into the load via S1 and out from the load via D1; when the topology is in State2, Fig. 2(c), the current flows into the load via D2 and out from the load via S2;

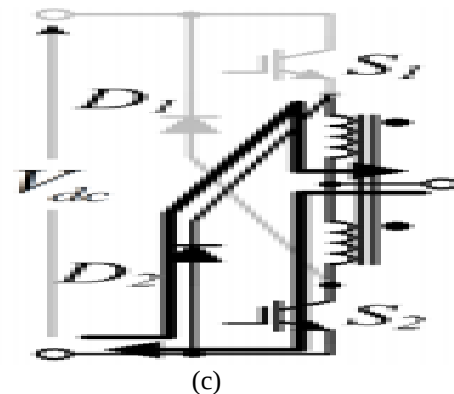


Fig. 2. Four states of one leg of the coupled-inductor inverter: (c) State2: outputs $-V_{dc}/2$ level; when the topology outputs $0V_{dc}$, S1 and S2 can be both ON, Fig. 2(d) or OFF, Fig. 2(e).

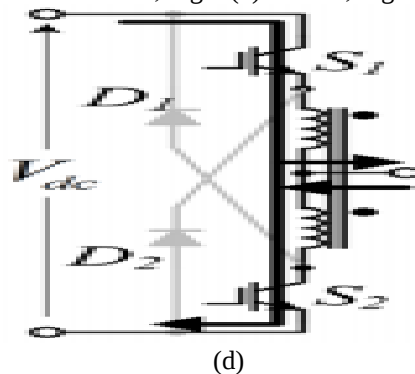


Fig.2. Four states of one leg of the coupled-inductor inverter: (d) State3: outputs $0V_{dc}$ level, the coupled inductor is energized;

In State3, Fig. 2(d), the coupled inductor is energized due to the directly imposed dc-link voltage so that the current in the coupled inductor rises. Vice versa, in Fig. 2(e), the coupled inductor is de-energized due to the reversely imposed dc-link and the current flows through two diodes (D1 and D2), and decreases.

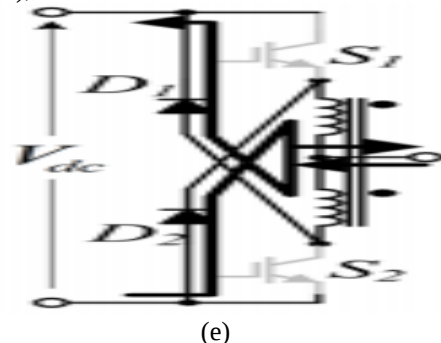


Fig.2. Four states of one leg of the coupled-inductor inverter : (e) State4: outputs $0V_{dc}$ level, the coupled inductor is de-energized.

These two states also support the bidirectional load current: according to (1), when the current i_{up} is larger than i_{dn} , the load current is

positive; when the i_{up} is smaller than i_{dn} , the load current is negative. It is also noticeable that in State3 and State4, the current in the coupled inductor rises/falls much faster than in State1 and State2. As a result, the rate of change of the currents in the coupled inductor in State1 and State2 is much smaller than that in State3 and State4, due to the low imposed voltage. As the CII is operated with PWM methods, the currents i_{up} and i_{dn} also include high-frequency components, and here they are represented as $i_{hf,up}$ for those in the upper arm, and $i_{hf,dn}$ for those in the lower arm. Finally, it is seen that, in State3, Fig. 2(d) and State4, Fig. 2(e), a zero-sequence component flows through the coupled inductor which produces a dc-offset current. It is represented by i_{dc} . Therefore, the currents in the two arms can be described as:

$$i_{up} = i_f + i_{hf,up} + i_{dc} \quad (2)$$

$$i_{dn} = -i_f + i_{hf,dn} + i_{dc} \quad (3)$$

where i_f is the fundamental-frequency component [35]. The i_f in two arms are chosen with the displacement of 180° , for the sake of convenient control. When i_{up} and i_{dn} are substituted in (2) into (1), the load current is:

$$i_o = 2i_f + i_{hf,up} - i_{hf,dn} \quad (4)$$

Hence, the load current only contains the fundamental frequency and high-frequency components.

Carrier Based PWM for the Coupled Inductor Inverter

In the conventional PWM for the NPC, the modulating waveform is compared with the triangular carriers: if the modulating waveform is equal or higher than the carrier, a switching-on signal is generated; if the former is smaller than the latter, a switching-off signal is generated. In the CBPWM method for CII proposed in [30]: two opposite carriers, which represent the upper switch (S1) and the lower switch (S2), are compared with one sinusoidal modulating waveform; the control signal for S1 is obtained according the above rule, whereas the control signal of S2 is obtained after the inversion of the signal obtained from the comparison of S2's carrier and the modulating waveform.

CBPWM METHOD FOR SINGLE LEG CII SYSTEM

In this section, a CBPWM method for the single leg CII is proposed. This technique directly follows the working principle of the coupled inductor and can naturally balance the volt-second, whereas the CM voltage is not reduced.

Proposed CBPWM for single-leg CII

In this paper, according to the aforementioned analysis, a CBPWM technique is proposed which achieves the same effect as the

previous carrier-based method for CII but is simpler to realize. The schematic of the proposed CBPWM is shown in Fig. 3, top part: two modulating waveforms (m_{S1} and m_{S2}), which have a displacement of 180° , represent two switches (S1 and S2); they are compared against a triangular carrier abiding by the conventional PWM rule and then the gate signals of S1 (sig_{S1}) and S2 (sig_{S2}) are generated, shown in the bottom part of Fig. 3.

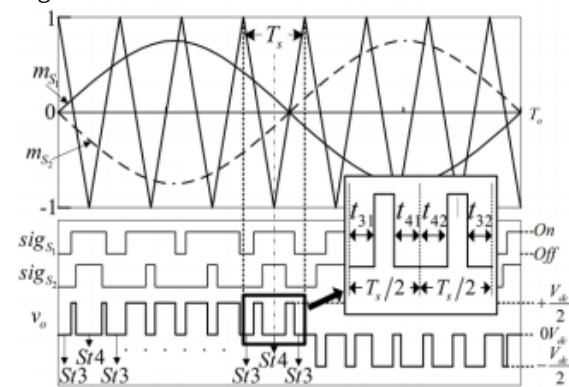


Fig.3. Schematic of the proposed CBPWM for CII: m_{S1} and m_{S2} : modulating waveforms for the upper switch S1 and the lower switch S2; sig_{S1} and sig_{S2} are the resulting gate signals generated by the comparison between m_{S1} and the carrier, and between m_{S2} and the carrier; v_o is the output voltage of one leg.

Finally, the output voltage of one leg, v_o , is obtained according to the states of two switches. The principle of this technique directly describes the operating principle of coupled inductor: by making the switches work out of phase, the two arms of the coupled inductors are imposed with the voltage pulses having opposite fundamental sinusoidal elements so that the currents in these two arms are opposite. Consequently, the load current will follow (3).

Natural Flux Balance

As mentioned in Section II, the flux generated in the energized state (State3) and the de-energized state (State4) has to be balanced within each switching period, because the core flux generated in these two states is far more than that in State1 and State2, and failure to achieve the volt-second balance will quickly saturate the coupled inductor and ultimately damage the system. The proposed method is able to automatically fulfill the volt-second balance mentioned above. In the bottom part of Fig. 3, "St3" and "St4" stand for State3 and State4. It is seen that these two states appear alternatively during a switching period change. The details of one switching period are displayed on inset of the figure: t_{31} and t_{32} are the first and the second duration of State3; t_{41} and t_{42}

are the first and the second duration of State4. Because the modulating waveforms m_{S1} and m_{S2} are opposite, t_{31} equals to t_{41} and t_{32} equals to t_{42} . Thus the durations of State3 and State4 are the same, which means the requirement of the volt-second balance is satisfied.

PROPOSED CBPWM METHOD WITH REDUCTION OF COMMON-MODE VOLTAGE IN FIVE-PHASE CII

In this section, CBPWM methods to cancel the CM voltage for five-phase inverters are proposed. Then the proposed methods are improved so that they can be applied to the five-phase CII system for the sake of volt-second balance. The improved methods also reduce switching events. Finally, the procedures of these methods are illustrated.

Common-mode Voltage

One of the side effects from the basic PWM process is an increased common-mode (CM) voltage. As shown in Fig. 1, the CM voltage, v_{nN} , is defined here as the potential of node “n” with respect to the node “N”. The frequency of the CM voltage can be equal to or higher than the switching frequency. When the inverters are connected to machines, this high-frequency voltage will produce bearing current via parasitic capacitance, leading to premature ageing of the insulation or bearing. Moreover, the CM voltage has other negative impacts such as causing vibration to the machine and producing EMI which potentially disrupts other electrical devices. In the five-phase inverter with balanced load in star-connection, the CM voltage is defined as follows:

$$v_{nN} = \frac{1}{5}(v_{AN} + v_{BN} + v_{CN} + v_{EN}) \quad (5)$$

Elimination of CM Voltage in Five-Phase Inverters

Similarly, as discussed in [35] for the three-phase case, $v_{nN} = 0$ is the requirement to eliminate the CM voltage in five-phase inverters. However, there are two ways to obtain this, shown in (5) and (6):

$$v_{nN} = \frac{1}{5}[(v_{AN} - v_{BN}) + (v_{BN} - v_{CN}) + (v_{CN} - v_{DN}) + (v_{DN} - v_{EN}) + (v_{EN} - v_{AN})] = 0 \quad (6)$$

which uses the two adjacent modulating waveforms and is called Method1;

$$v_{nN} = \frac{1}{5}[(v_{AN} - v_{CN}) + (v_{BN} - v_{DN}) + (v_{CN} - v_{EN}) + (v_{DN} - v_{AN}) + (v_{EN} - v_{BN})] = 0 \quad (7)$$

which uses the non-adjacent modulating waveforms and is called Method2. Although the two methods are using two different waveforms, their weighted total harmonic distortion (WTHD)

performances are similar, which will be shown in Section VII.

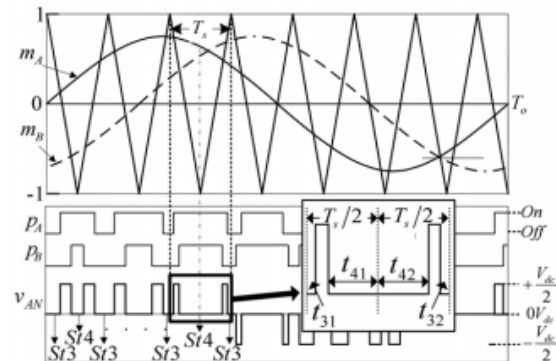


Fig. 4. Schematic of CBPWM with CM voltage elimination for five-phase inverters: m_A and m_B are the modulating waveforms of Phase A and Phase B; p_A and p_B are the results of the comparisons between m_A and the carrier, and between m_B and the carrier; v_{AN} is the expected output voltage of Phase A.

Fig. 4 shows the waveforms of Method1, the output waveform of Phase A and uses the same legends as Fig. 3. Fig. 5 displays the flowchart of realizing Method1.

Step1: PWM signals (p_A and p_B) are obtained by comparing the modulating waveforms of Phase A and Phase B (m_A and m_B) respectively with the carrier;

Step2: signal v^*_{AN} is obtained by subtracting p_B from p_A ; this signal will also be the pattern of the output voltage of Phase A (v_{AN});

Step3: An encoder is designed to translate v^*_{AN} into control signals of two switches in Phase A. The signals F_1 , F_2 and F_3 , Fig. 5, are additional signals for the CII system. After these three steps, the gate driver signals of the two switches in Phase A are obtained.

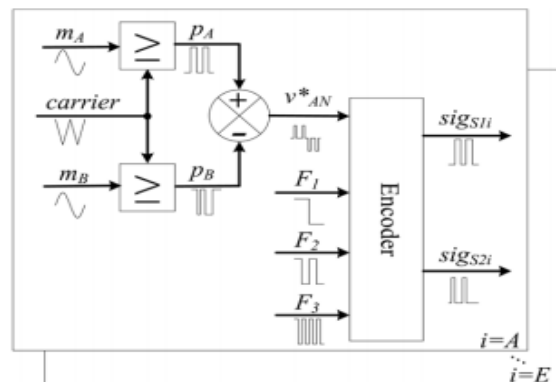


Fig. 5 Flowchart of the proposed Method1.

For the conventional three-level inverters, completion of the above steps will help the inverters cancel the CM voltage. However, for the

CII system, an extra step is required to identify the position of two 0Vdc states so that the volt-second is balanced. **CM Voltage Reduction for Five-phase CII with CBPWM methods**

If the methods are implemented directly on the CII with State3 and State4 appearing in turns, large in-phase currents are generated in the coupled inductors (greater than ten times the current rating in the simulation). As shown in Fig. 4, because the phase displacement of mA and mB is not 180°, the durations of State3 and State4 are not equal: in the inset, t31 is much smaller than t41, and as is the case for t32 and t42.

The solution is demonstrated in Fig. 6 which shows three switching periods. Because the switching period is much shorter than the output period, mA (solid) and mB (dotted) are represented by straight lines; SigS1 and SigS2 represent the final gate signals of two switches in one leg.

TABLE I TRUTH TABLE OF THE FINITE STATE MACHINE

v^*_{AN}	F1	F2	F3	State	SigS1	SigS2
1	X	X	X	1	1	0
-1	X	X	X	2	0	1
0	0	0	0	4	0	0
0	0	0	1	3	1	1
0	0	1	0	4	0	0
0	0	1	1	3	1	1
0	1	0	0	3	1	1
0	1	0	1	3	1	1
0	1	1	0	4	0	0
0	1	1	1	4	0	0

Firstly, in order to reduce switching losses (because the transition between State3 and State4 requires two switches to change state at the same time), the end of one switching period and the beginning of its next switching period should have identical states.

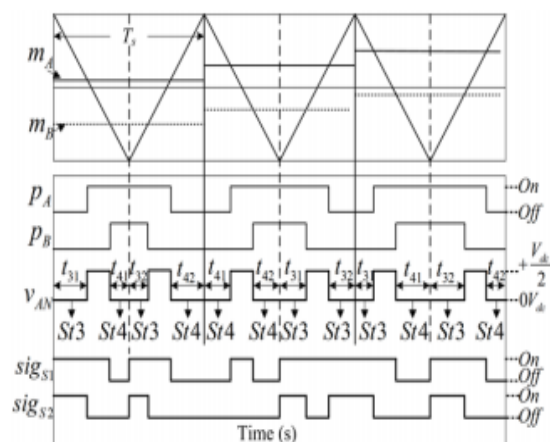


Fig. 6. Schematic of CBPWM with CM voltage elimination for CII: mA and mB are the modulating waveforms of Phase A and Phase B; pA and pB are

the results of the comparisons between mA and the carrier, and between mB and the carrier; t31 and t32 are the durations of State3; t41 and t42 are the durations of State4; SigS1 and SigS2 are the control signals for S1 and S2 in one phase leg.

For instance, in Fig. 6, the second switching period is joined to the first period by State4 and the third is joined to the second via State3. Secondly, in the middle of the switching period, the direct transition from State3 to State4 or from State4 to State3 is inevitable for the sake of volt-second balance. If State3 appears before State4, the two switches in the same leg have different turn-off times when they are conducting different currents:

TABLE II PARAMETERS IN SIMULATION

Parameters	Value
Modulation index	0.3/ 0.75/ 1.0
Dc-link voltage [V]	500
Dc-link capacitor [μ F]	3300
Switching frequency [kHz]	10
Fundamental frequency [Hz]	50
Coupled inductors* [mH]	3.2
Mutual inductance factor	0.95
Resistive load [Ω]	100
Inductive load [mH]	19.5
The number of turns in one arm of the coupled inductor	191

The truth table of the encoder for the CII system is given in Table I. F1, F2 and F3 are only considered when v^*_{AN} is 0. State3 and State4 respectively occupy four of eight states produced by the combination of the three additional signals.

SPACE VECTOR CONCEPT

The space vector concept, which is derived from the rotating field of induction motor, is used for modulating the inverter output voltage. In this modulation technique the three phase quantities can be transformed to their equivalent two-phase quantity either in synchronously rotating frame (or) stationary frame. From these two-phase components, the reference vector magnitude can be found and used for modulating the inverter output. The process of obtaining the rotating space vector is explained in the following section, considering the stationary reference frame. Considering the stationary reference frame let the three-phase sinusoidal voltage component be,

$$V_a = V_m \sin(\omega t) \quad (8)$$

$$V_b = V_m \sin(\omega t - 2\pi/3) \quad (9)$$

$$V_c = V_m \sin(\omega t - 4\pi/3) \quad (10)$$

When this three-phase voltage is applied to the AC machine it produces a rotating flux in the air gap of the AC machine. This rotating resultant

flux can be represented as single rotating voltage vector. The magnitude and angle of the rotating vector can be found by means of Clark's Transformation as explained below in the stationary reference frame. To implement the space vector PWM, the voltage equations in the abc reference frame can be transformed into the stationary dq reference frame that consists of the horizontal (d) and vertical (q) axes as depicted in Figure-2.

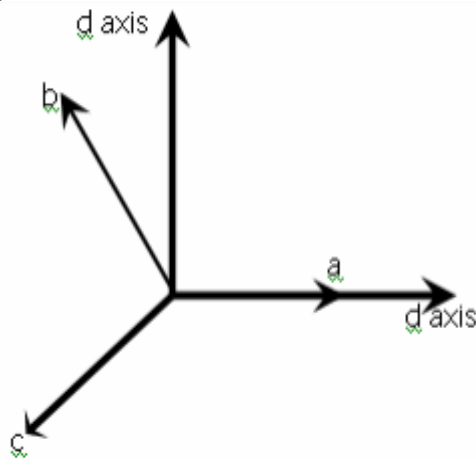


Fig.7 The relationship of abc reference frame and stationary dq reference frame.

As described in Figure-7. This transformation is equivalent to an orthogonal projection of [a b c] t onto the two-dimensional perpendicular to the vector [1 1 1] t (the equivalent d-q plane) in a three-dimensional coordinate system. As a result, six non-zero vectors and two zero vectors are possible. Six non-zero vectors (V1-V6) shape the axes of a hexagonal as depicted in Figure-8, and supplies power to the load.

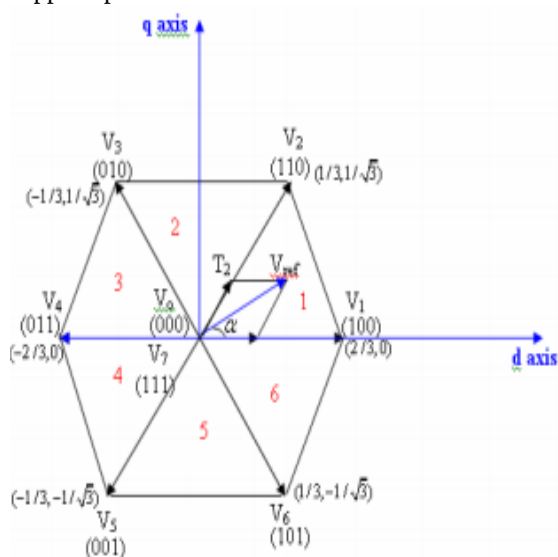


Fig.8. Basic switching, vectors and sectors

The angle between any adjacent two non-zero vectors is 60 degrees. Meanwhile, two zero vectors (V0 and V7) and are at the origin and apply zero voltage to the load. The eight vectors are called the basic space vectors and are denoted by (V0, V1, V2, V3, V4, V5, V6, V7). The same transformation can be applied to the desired output voltage to get the desired reference voltage vector, Vref in the d-q plane. The objective of SVPWM technique is to approximate the reference voltage vector Vref using the eight switching patterns. One simple method of approximation is to generate the average output of the inverter in a small period T to be the same as that of Vref in the same period.

Table:III Switching patterns and output vectors

Voltage vectors	Switching vectors			Line to neutral voltage			Line to line voltage		
	A	B	C	V _{an}	V _{bn}	V _{cn}	V _{ab}	V _{bc}	V ₀
V ₀	0	0	0	0	0	0	0	0	0
V ₁	1	0	0	2/3	-1/3	-1/3	1	0	-1
V ₂	1	1	0	1/3	1/3	-2/3	0	1	-1
V ₃	0	1	0	-1/3	2/3	-1/3	-1	1	0
V ₄	0	1	1	-2/3	1/3	1/3	-1	0	1
V ₅	0	0	1	-1/3	1/3	2/3	0	-1	1
V ₆	1	0	1	1/3	-2/3	1/3	1	-1	0
V ₇	1	1	1	0	0	0	0	0	0

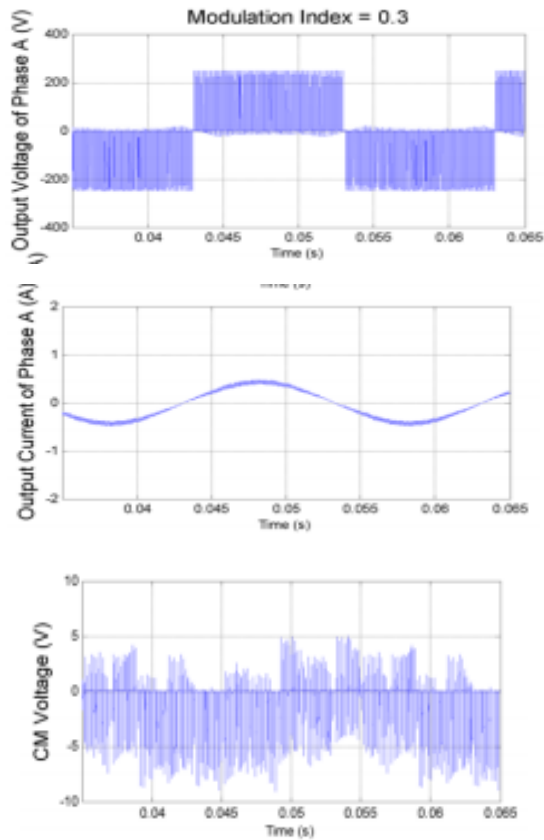
SIMULATION RESULTS

In this section, the methods are simulated in MATLAB, and simulated results of both Method1 and Method2 are shown. The simulations are performed with three modulation indices: 0.3, 0.75 and 1.0 which represent the linear modulation range of the CII. The modulation index is defined as:

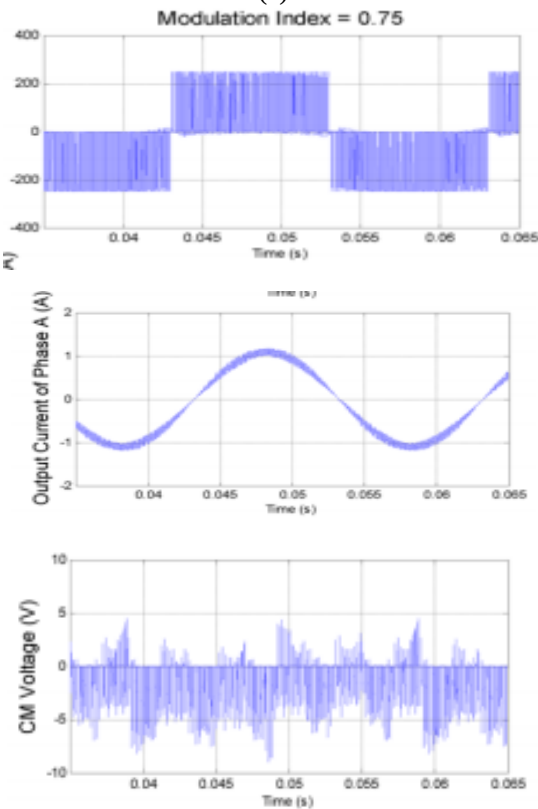
$$M = \frac{V_{ref}}{V_{dc}\sqrt{2}} \quad (11)$$

where Vref is the reference voltage and Vdc is the dc-link voltage. Simulations and experiments share the parameters in Table II. Fig. 7 shows the simulated results of Method1 at different modulation indices. It is clear that the CM voltages at all three modulation indices are almost zero (less than 10V, which is 2% of the dc-link voltage). Fig. 8 shows the simulated results of Method2.

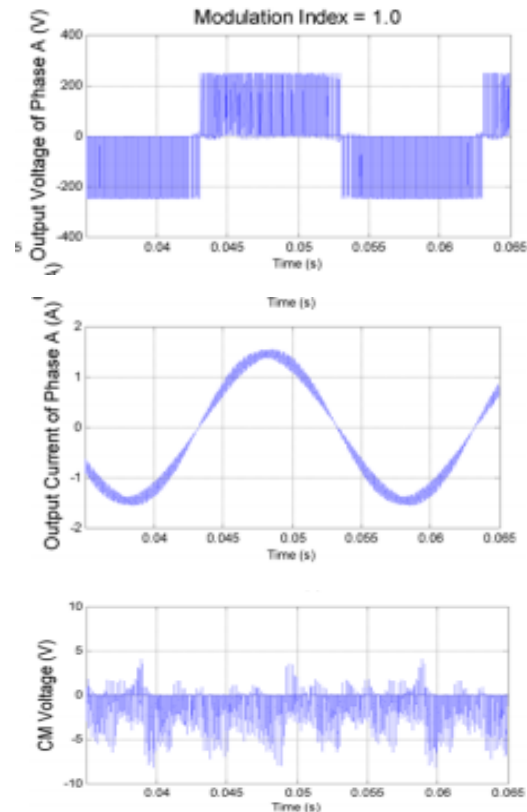
The arrangement of waveforms is identical to Fig. 9. As Method2 uses the non-adjacent modulating waveforms to cancel the CM voltage whereas Method1 uses adjacent modulating waveforms voltage, the root-mean-square (RMS) of output voltage generated by Method 2 is higher than that by Method 1 by the factor 1.618. Method2 is in use, the modulation index should be divided by 1.618 to get the same output voltage.



(a)



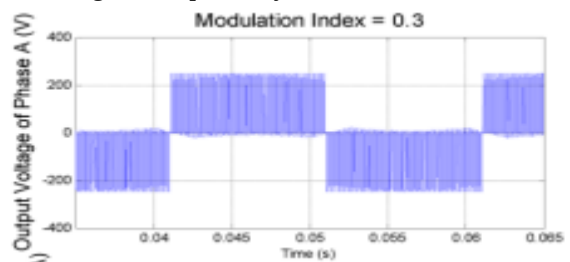
(b)

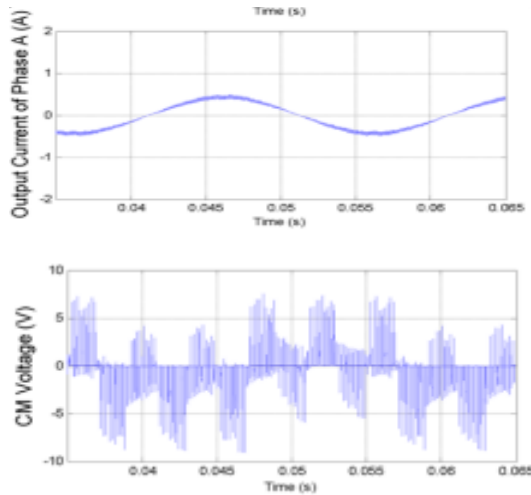


(c)

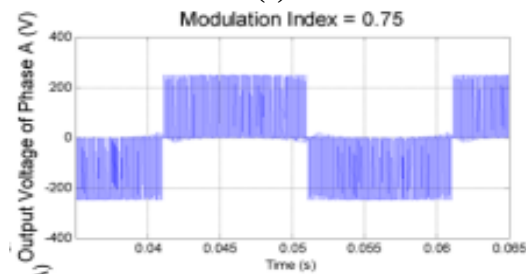
Fig. 9. Simulated results of Method1 (time scale 5ms/div): (a) modulation index = 0.3; (b) modulation index = 0.75; (c) modulation index = 1.0; the first row: the load voltage of Phase A, 200V/div; the second row: the load current of Phase A, 1A/div, the third row, the CM voltage, 5V/div.

Both methods are successfully applied to five-phase CII to generate three-level output voltage. The load currents only have the fundamental-frequency and high-frequency elements. This is in a good agreement with the analysis in Section II. The CM voltages produced in two methods are shown in the third rows in Fig. 9 and Fig. 10, respectively.

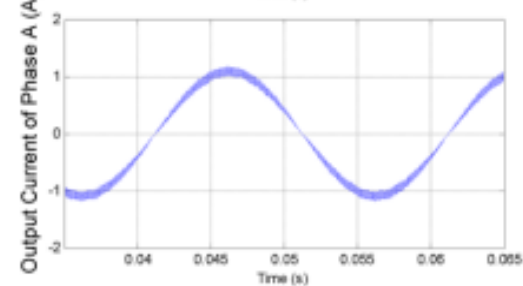




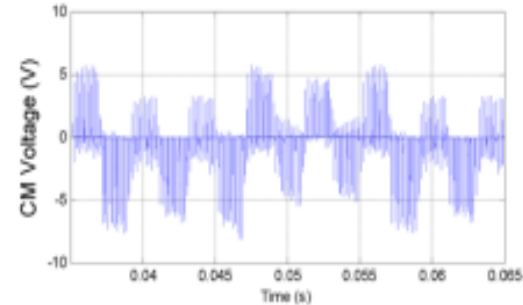
(a)



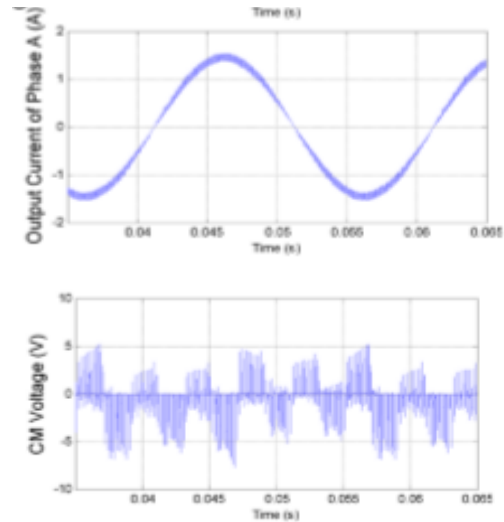
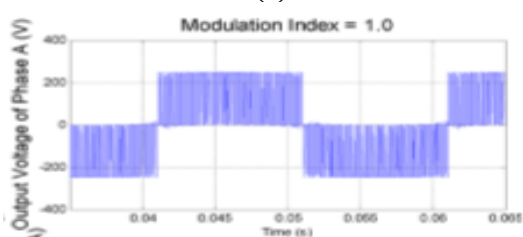
(b)



(c)



(d)



(e)

Fig.10. Simulated results of Method2 (time scale 5ms/div): (a) modulation index = 0.3; (b) modulation index = 0.75; (c) modulation index = 1.0; the first row: the load voltage of Phase A, 200V/div; the second row: the load current of Phase A, 1A/div, the third row, the CM voltage, 5V/div.

It is seen that the CM voltage is successfully reduced to almost zero, in spite of some residual CM voltages which are less than 5V.

CONCLUSION

A carrier-based PWM technique for the five-phase coupled inductor inverter (CII) is proposed in this paper. This method uses two opposite sinusoidal waveforms which are compared with a carrier to control the switches in one phase leg. This technique is a more intuitive method of PWM compared with existing techniques and helps develop a better understanding of the operating principle of the coupled inductor in the inverter. Space vector PWM is an advanced technique used for variable frequency drive applications. It utilizes dc bus voltage more effectively and generates less THD in the Three Phase Voltage Source Inverter. Two alternative carrier-based PWM methods are then proposed for the five-phase inverter so as to reduce the common-mode (CM) voltage. These two methods are further improved to balance the volt-second in the coupled inductors; hence, in-phase currents in the coupled inductors are avoided. The two methods are verified in simulation and they successfully reduce the CM voltage to almost zero.

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