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Novel approach for Exchanges Briefs Concept, Design, and Implementation of Reconfigurable CORDIC

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Abstract:

This brief presents the key concept, design strategy, and implementation of reconfigurable coordinate rotation digital computer (CORDIC) architectures that can be configured to operate either for circular or for hyperbolic trajectories in rotation as well as vectoring-modes. It can, therefore, be used to perform all the functions of both circular and hyperbolic CORDIC. We propose three reconfigurable CORDIC designs: 1) a reconfigurable rotation-mode CORDIC that operates either for circular or for hyperbolic trajectory; 2) a reconfigurable vectoring-mode CORDIC for circular and hyperbolic trajectories; and 3) a generalized reconfigurable CORDIC that can operate in any of the modes for both circular and hyperbolic trajectories. The reconfigurable CORDIC can perform the computation of various trigonometric and exponential functions, logarithms, square-root, and so on of circular and hyperbolic CORDIC using either rotation-mode or vectoring-mode CORDIC in one single circuit. It can be used in digital synchronizers, graphics processors, scientific calculators, and so on. It offers substantial saving of area complexity over the conventional design for reconfigurable applications.

Keywords: CORDIC, 3-D Graphics Processor, MUX

I. INTRODUCTION

The coordinate rotation digital computer (CORDIC) algorithm involves a simple shift-add iterative procedure to perform several computing tasks by operating in either rotation-mode or vectoring-mode following any one among linear, hyperbolic, and circular trajectories. Applications such as singular value decomposition, eigenvalue estimations, QR decomposition, phase and

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frequency estimations, and synchronization in digital receivers, 3-D graphics processor, and interpolators require the CORDIC to operate in both rotation and vectoring-modes. The 3-D structures such as hyperboloids, paraboloids, and ellipsoids require the CORDIC to be operated in both circular and hyperbolic trajectories. The hardware implementation of these applications requires more than one CORDIC processor operating in different modes and different trajectories. A reconfigurable CORDIC, which can operate in rotation and vectoring-modes, for both circular and hyperbolic trajectories can replace multiple CORDIC processors, and would be highly useful for such applications. A reconfigurable CORDIC can be utilized for a variety of applications in communication systems, signal processing, 3-D graphics, robotics apart from general scientific calculations, and waveform generations. In the last five decades, several algorithms have been proposed for area-delay-efficient and power-efficient implementation of CORDIC algorithms, either for circular trajectory [2]–[7] or for hyperbolic trajectory. But, we do not find any systematic study ondesign and implementation of reconfigurable CORDIC in the existing literature. A basic design of reconfigurable CORDIC based on a unified CORDIC algorithm has been proposed recently. The reconfigurable design of is found to involve high reconfiguration overhead and results in low hardware utilization efficiency.

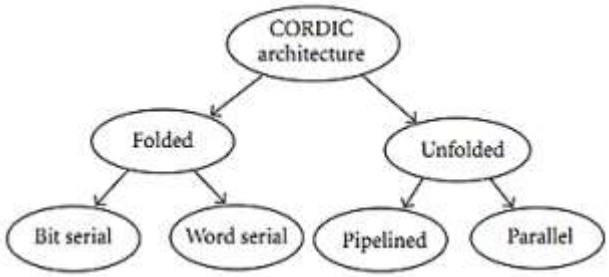

Fig 1: Classification of CORDIC architecture

Figure1 above gives us an idea of classification of CORDIC architectures., This classification is based on three iterative equations . Folded architectures is realised by duplicating each of the difference equations of the CORDIC algorithm into hardware and time multiplexing all the iterations into a single functional unit. Folding gives an option of trading area for time in signal processing architectures. The folded architectures are further subdivided into bit-serial and word-serial architectures

on the basis of functional unit implemented. The CORDIC algorithm conventionally has been implemented using bit serial architecture with all iterations executed within same hardware [3] and this slows down the computational device rendering it unsuitable for high speed implementations. The word serial architecture [7, 48] is an iterative CORDIC architecture obtained by realizing the iteration equations and employs the modified shifters in each iteration to cause the desired shift for the iteration.

II. LITERATURE SURVEY

Coordinate Rotation Digital Computer is shortened as CORDIC. Two-dimensional geometry forms the basis of CORDIC arithmetic however the iterative method of a computational algorithm to implement this was presented by Jack E. Volder to compute multiplication, division and trigonometric functions in 1959[1], [2].

Concept, Design, and Implementation of Reconfigurable CORDIC SupriyaAggarwal, Pramod K. Meher, and KavitaKhare IEEE Transactions On Very Large Scale Integration (VLSI) Systems 2016.

The proposed scheme allows CORDIC to work in different modes and trajectories of operations. It is employed in synchronizers, waveform generators, lowcost scientific calculators with almost no effect on the maximum operating frequency. This presented scheme save approximately 60% of the area compared to the conventional CORDIC architecture.

Implementation of a Fast Hybrid CORDIC Architecture BhawnaTiwari, NidhiGoel 2016 Second International Conference on Computational Intelligence & Communication Technology IEEE 2016.

In this work the authors have shown that the proposed architecture is faster in execution at expense of reduced accuracy and high power consumption as compared to the reference architecture.

CORDIC-based FFT Real-time Processing Design and FPGA Implementation Aimei Tang*, Li Yu, Fangjian Han, Zhiqiang Zhang, 2016 IEEE 12th International Colloquium on Signal Processing & its Applications (CSPA2016), 4 - 6 March 2016, Melaka, Malaysia.

The proposed method minimizes the hardware complexity of the system sue to the usage of pipelined structure, the dual-port RAM, butterflies of the radix-2Decimation-InTime (DIT) algorithm.It also improves the Signal Noise Ratio.

CORDIC II: A New Improved CORDIC Algorithm Mario Garrido, Member, IEEE, PetterKällström, Martin Kumm and Oscar Gustafsson, Senior Member, IEEE IeeeTransactions On Circuits And Systems Part Ii: Express Briefs 2016.

With lots of versions of CORDIC algorithm being available the authors have presented a scheme for substitution of CORDIC micro-rotation and have proposed a new algorithm called CORDIC II which uses minimum number of adders as compared with the other CORDIC algorithm as it uses new variety of rotators.

CORDIC Architectures: A Survey B. Lakshmi and A. S. Dhar, Hindawi Publishing Corporation VLSI Design Volume 2010, doi:10.1155/2010/79489

This paper does a brief survey and classifies different CORDIC algorithm and also focuses on algorithm that pre compute the direction of rotations. Special focus and more stress have been given on higher radix and redundant algorithms.

III. EXISTING METHOD

The scheme for reducing the area of the CORDIC using multiplexer is proposed for the ASIC implementation in paper [3]. This is adopted for the FPGA based implementation in this paper. The area is reduced by removing some of the stages of Fig.2. The first stage output of original unrolled CORDIC architecture is equal to xi, therefore we can directly write the output of first stage as

$$y_1 = x_i$$

$$x_1 = x_i$$

If the first stage output is positive, then

$$y_2 = y_1 - \frac{x_1}{2} = \frac{x_i}{2}$$

$$x_2 = x_1 + \frac{y_1}{2} = \frac{3 \times x_i}{2}$$

The vector coordinates corresponding to negative output is

$$y_2 = y_1 + \frac{x_1}{2} = \frac{3 \times x_i}{2}$$

$$x_2 = x_1 - \frac{y_1}{2} = \frac{x_i}{2}$$

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The output of the second stage is fixed. So we can implement the second stage using two Muxes and choosing select line as the MSB bit of the previous angle accumulator output. Fig.3 shows the circuit of second stage using Muxes with MSB select line

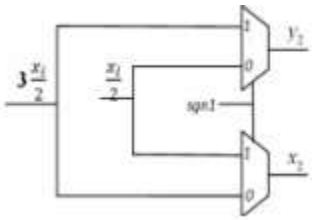

Fig 2: First stage of mux based cordic

To reduce the area, we replace the third stage with Muxes. Since the third stage output also depends only on xi, we can express the outputs as

$$y_3 = y_2 + \frac{x_2}{4} = \frac{x_i}{2} + \frac{3\times x_i}{8} = \frac{7\times x_i}{8}$$

$$x_3 = x_2 - \frac{y_2}{4} = \frac{3\times x_i}{2} - \frac{x_i}{8} = \frac{11\times x_i}{8}$$

for $sgn_1=1, sgn_2=0$

$$y_3 = y_2 - \frac{x_2}{4} = \frac{3\times x_i}{2} - \frac{x_i}{8} = \frac{11\times x_i}{8}$$

$$x_3 = x_2 + \frac{y_2}{4} = \frac{x_i}{2} + \frac{3\times x_i}{8} = \frac{7\times x_i}{8}$$

for $sgn_1=0, sgn_2=1$

$$y_3 = y_2 - \frac{x_2}{4} = \frac{x_i}{2} - \frac{3\times x_i}{8} = \frac{x_i}{8}$$

$$x_3 = x_2 + \frac{y_2}{4} = \frac{3\times x_i}{2} + \frac{x_i}{8} = \frac{13\times x_i}{8}$$

for $sgn_1=1, sgn_2=1$

$$y_3 = y_2 + \frac{x_2}{4} = \frac{3\times x_i}{2} + \frac{x_i}{8} = \frac{13\times x_i}{8}$$

$$x_3 = x_2 - \frac{y_2}{4} = \frac{x_i}{2} - \frac{3\times x_i}{8} = \frac{x_i}{8}$$

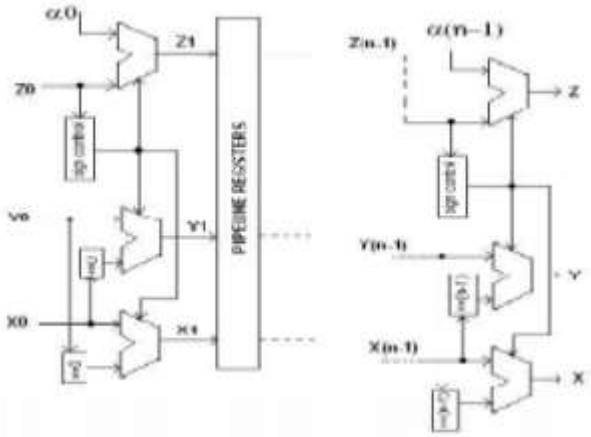

Fig 3: Second stage of mux based cordic

The block diagram of the CORDIC when the adders till third stage are replaced with Muxes is shown in Fig.3. As the adders are replaced with Muxes, the area of the circuit

is reduced till 3rd stage. The pipelined CORDIC use registers in between each iteration stage. Theadvantage of pipelined unrolled CORDIC over the unrolled CORDIC is its higher frequency of operation. This property can be used in high speed applications. The number of registers depends on the number of stages in pipelining and there will be an increase in area. The first output of an Nstage pipelined CORDIC core is obtained after N clock cycles. Thereafter, outputs will be generated during every clock cycle. In this paper, pipelined registers are placed after fourth and seventh stages. The Mux based pipeline unrolled CORDIC architecture in which pipeline registers are inserted at the output of fourth and seventh stage.

IV. PROPOSED METHOD

The coordinate calculation matrices for circular and hyperbolic CORDICs differ by the sign of operands, and to realize that additions are to be replaced by subtractions and vice-versa. This can be easily realized by a reconfigurable add/subtract circuit. In both cases, the basic-shift could be either 2 or 3, but the number of micro rotations varies with the mode of operation. Besides, each case will have its own circuit to enable the extension of RoC. Based on these observations, we design three reconfigurable CORDIC architectures: 1) rotation-mode reconfigurable CORDIC; 2) vectoring-mode reconfigurable CORDIC; and 3) generalized reconfigurable CORDIC.

A. Rotation-Mode Reconfigurable CORDIC

The proposed design for reconfigurable rotation-mode CORDIC (shown in Fig. 4) consists of three parts: 1) preprocessing unit; 2) reconfigurable CORDIC rotation unit; and 3) post processing unit. The preprocessing unit ensures that the input rotation angle to the CORDIC processing structure always lies in the range [0, π/4], as the maximum rotation angle that can be handled by micro rotation sequence generator is π/4. The post processing unit is required only for circular trajectory to swap/complement the sine/cosine values depending on the octant of the rotation angle. The user can control the trajectory of the reconfigurable CORDIC by changing a 1-bit signal T. The rotation matrix for reconfigurable rotation-mode CORDIC is

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obtained after unifying the rotation matrices of circular

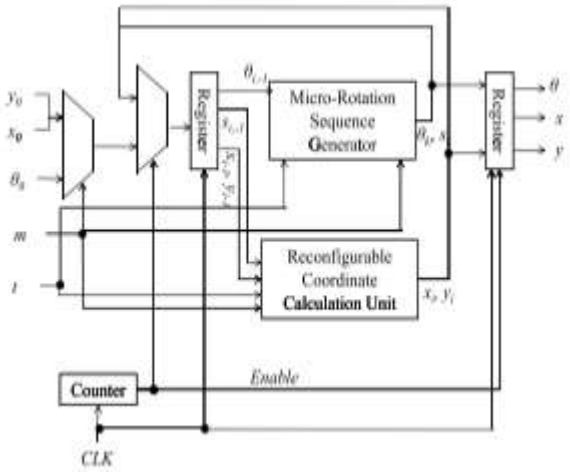

Fig 4: Structure of the proposed reconfigurable recursive CORDIC architectures.

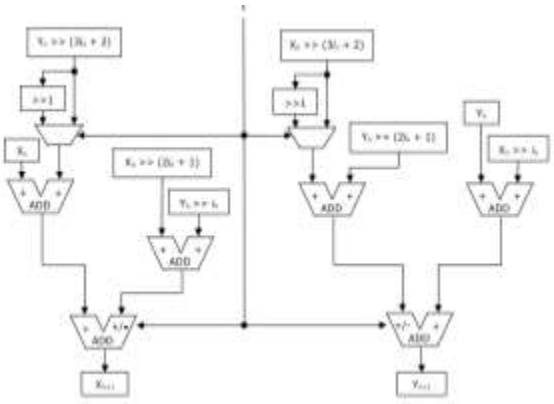

Fig 5: RCCU for recursive design.

B. Pipelined Architecture Proposed

Fig. 6 shows the reconfigurable CORDIC rotation unit for basic-shift 2. The shift-index si is fixed in every RCCU, and hence the shifters are hardwired and do not involve high complexity barrel-shifters. The implementation of RCCUs varies according to the basic-shift si. With slight modifications, the pipeline can be extended for basic-shift 3

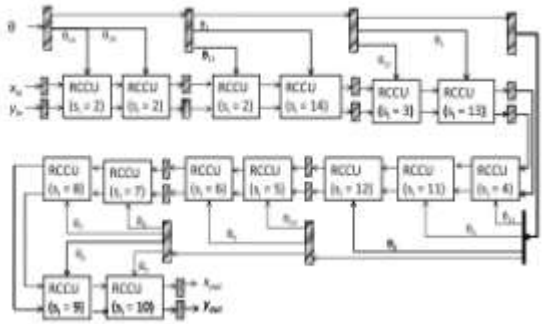

Fig 6: Reconfigurable rotation-mode CORDIC unit for basic-shift 2.

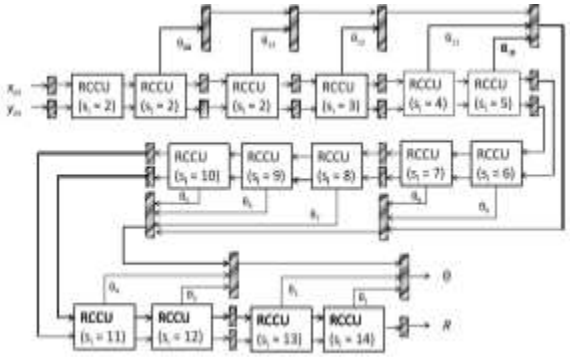

Fig 7: Proposed pipeline reconfigurable vectoring-mode CORDIC unit**RESULT**

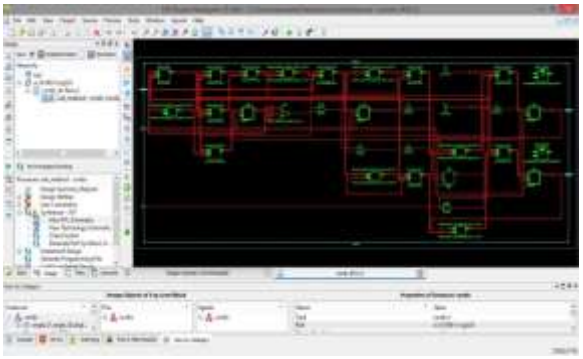

Fig 8: RTL schematic of the proposed system

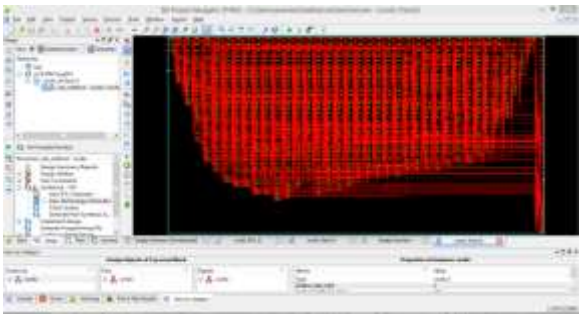

Fig 9: Technology schematic of the proposed system

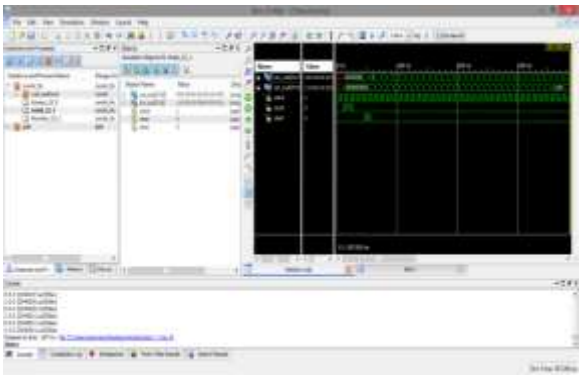

Fig 10: Simulation result of the proposed system

V. CONCLUSION

In this brief, for the first time a systematic design method for reconfigurable CORDIC is proposed to let a CORDIC function in different modes and different trajectories of operations. The proposed reconfigurable CORDIC architectures can be used in a variety of applications, such as synchronizers, waveform generators, low-cost scientific calculators, and so on. Approximately 60% of the area is saved by the proposed rotation or vectoring-mode reconfigurable CORDIC designs over the reference recursive reconfigurable CORDIC, without any effect on the maximum operating frequency. On the other hand, the proposed pipelined rotation and vectoring-mode reconfigurable CORDIC designs save 30%–50% area compared with the reference reconfigurable design, with nearly the same maximum operating frequency.

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