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Review: Non – Volatile Floating Gate Flash Memory

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Abstract

NON-VOLATILE EMBEDDED FLASH MEMORY can be defined in terms of a Single-polysilicon or a Dual-polysilicon with the help of NAND or NOR flash memory architecture. Either of these two method, it can open doors to newly system storages capabilities and new application for embedded SOC & non volatile VLSI chips in standard logic process technology. This paper provides an analysis on knowledge discovery of non volatile embedded flash memory in different logic process technology and Program methods & Erase methods voltages respectively to store data and to erase data from the embedded flash memory cells. The proposed method will use different Tunnel Oxide thickness and Channel Width to obtain better performance of non volatile embedded flash memory and reduction in program & erase voltage and it will improve threshold voltage window for floating gate transistor cell.

Key Words:

Embedded Flash Memory; High Speed; Erase Voltage; Floating Gate; NAND Flash Memory; Non Volatile Memory; NOR Flash Memory; Program Voltage; SOC.

Introduction

Nowadays, newly low power systems are introduced such as embedded microcontroller, microprocessor and wireless sensors to minimize the leakage at long stand-by mode. So one of the important requirement at stand-by periods is to retain critical data (information) in memory. For that purpose non volatile memory comes in picture because data will available when power goes off. There are few non volatile memory present such as Flash memory, Programmable Read-only Memory(PROM), Electrically Erasable Programmable Read-only Memory(EEPROM) and some are high density non volatile memories on development such as RRAM, STT-MRAM, SONOS, Racetrack memory and millipede memory. How-ever there are a few attempts made to develop high density cost effective non - volatile memory and low power consumption compare to other non volatile memory.

Embedded flash memory developed by using NAND and NOR logic gates so there are to embedded flash memory name given after that existence characteristic according to those two gates “NAND Flash” and “NOR Flash”. These two types can be design on single polysilicon layer or dual poly silicon layer. Nowadays single polysilicon implementation is used because it has only one p-type or n-type later and using single layer, embedded flash memory size can be reduce and fabricate memory with small size has high integrity, high density and threshold voltage for floating gate transistor can reduce and because of that program & erase voltage will reduce.

The NAND flash application is used in mass storage device such as USB drive, main memory and memory cards for store data and easy to transfer. Whereas NOR flash used for microcontroller memory which is near to CPU like small memory for example cache memory.

Basic cell structure and working

To develop embedded flash memory cell, it required floating gate between control gate and substrate where channel formed between source and drain. In embedded flash memory, in top control gate deposited and below that floating gate deposited floating gate stored data (information) in form of electrons which is shown in Fig.1 and transistor is shown in Fig.2.

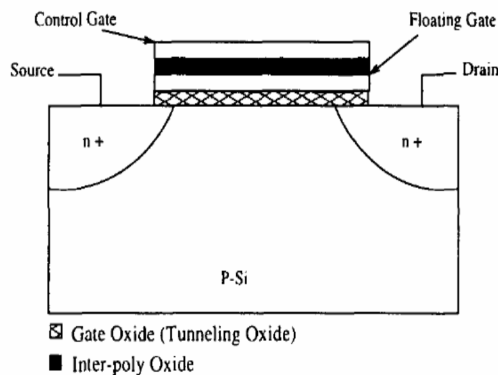

Fig. 1. Basic flash cell

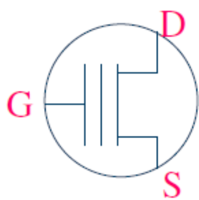

Fig.2 transistor cell

Programming embedded flash cell.

Embedded flash memory is program (write) by FN-Tunneling (Fowler Nordheim tunneling). In FN-tunneling positive voltage applied to drain, during this condition tunneling channel will formed between drain to source and electrons travel from source to drain. When channel formed, apply higher positive voltage compare to drain at control gate. By doing these electrons in channel attract to control gate positive voltage and attracted electron stored floating gate. This is how embedded flash memory programmed.

Erasing and Reading embedded flash cell.

For erasing embedded flash cell also FN-Tunneling method apply. In erasing positive voltage is applied to substrate or negative voltage is applied to control gate. During this process whatever electrons present in floating gate will attract to substrate positive voltage or reflect form floating gate to substrate because of negative voltage of control gate and embedded flash memory will erase.

To reading the data from embedded flash cell, only positive voltage apply to control gate and will read data present in floating gate. If electron present in floating gate, flash memory read as one otherwise zero.

Literature survey

H. Kojima et al. develop 1-T flash memory on dual-polysilicon layer at 90nm process logic technology and established flash cell at 10nm tunnel oxide between substrate and floating gate. High plus & minus 10V voltage for program and erase a cell [1]. A 2-T dual polysilicon development given by Y. Lee. In that very high 16V apply for write flash cell at 7nm tunnel oxide [2]. A 3-T dual polysilicon at 0.4um process logic technology is done by T. Ikehashi. For that very high voltage 22V FN-Tunneling apply to control gate. Where

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other hand addition mask used for reduce power consumption [3-5]. Later, J. Yater presented a Split-Gate embedded flash memory which reduces the write voltage and also capability of electrons injection. But it required addition process step like split-gate (SG) which is half on source and other half between drain and source, and it also require Nano-Crystal (NC) layer compares to standard cell [6]. Because of split-gate implementation Source Side Injection (SSI) method used for program a embedded flash memory.

Proposed logical method

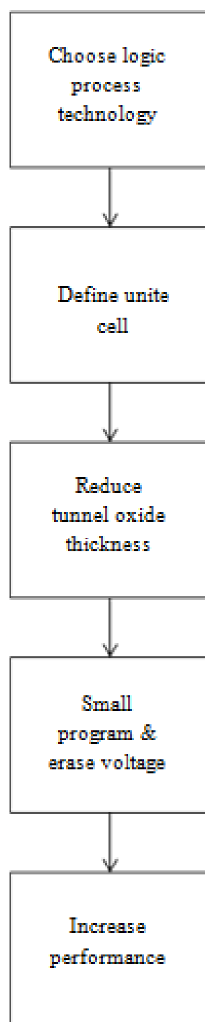

Fig. 3 process steps

The most important thing in memory is the performance and storage capability within short time period. The proposed method exits on the single-poly silicon layer and by using single-poly, complexity reduced. In this paper, embedded flash memory develops on below 65nm logic process technology like 45nm. By using lesser technology, the width and length of the transistor automatically reduces and hence the size of the transistor becomes smaller. The type of unit cell is any of previous architecture. The oxide thickness of the unite cell transistor is below 5nm thickness. In this paper, the tunnel oxide thickness is around 1nm to 3nm, by doing this less program voltage and erase voltage can be achieved due to the thickness of oxide layer. As the voltage reduces, the electrons easily attract to small positive voltage at word line (control gate) and by using small voltage at substrate, erase operation takes place. As result, the performance increases due to reduce in time of programming & erasing.

For this implementation, Tanner v13 and Microwind v3.1 tools are used for designing as the transistor W/L ratio and tunnel oxide thickness can be set dynamically. Constant voltage around 5V to7V use to program and erase unit-cell and 4x4 architecture develop by using combination of unit cells. If 45nm or beyond that technology used then the unit cell size reduces, performance increases and power decreases due to increase in speed of program and erase operation of unit cell and storage capability increase. There may be an increase in power dissipation due to increase in leakage current because the unit cell tunnel oxide thickness is below 5nm.

Application

`The embedded flash memory is small and it is very useful in firmware storage like small RAM for DDR2 SDRAM modern SRAM in controller and processor. The flash memory replaces hard disks (mass storage device) as well. It is used as solid state drive (SSD) as a long term storage device. It can also use as small storage memory which is near to microcontroller so whenever data needed, controller uses direct data stored in memory like cache memory.

Conclusion

Many approaches are made to develop embedded flash memory by using different process technology as well as different program and erase voltage. By reducing tunnel oxide thickness a memory performance can be increased and newer flash memory can be produced which provides high performance and less power consumption due to small size of cell and complex architectures can be developed using combination of different unit cells which can provide more storage as per requirement. Due to small size and thickness of tunnel oxide there might be a chance of current leakage in cell which can be overcome by controlling threshold voltage which can varry transistor by transistor.

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