International Journal of Research
Available at https://edupediapublications.org/journals
e-ISSN: 2348-6848
p-ISSN: 2348-795X
Volume 06 Issue 06
May 2019

Digital Sensor less Current Mode Control Based on Charge Balance Principle and Dual Current Error Compensation for DC-DC Converters in DCM

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ABSTRACT

For Discontinuous Conduction Mode (DCM) dc– dc converters with digital sensor less current mode (DSCM) control, a watched current mistake happens, inferable from a low-exactness current eyewitness. In addition, a reference current mistake happens because of a low-precision current controller or a finite dc increase of current circle. Ordinarily, the watched current is repaid to expand current guideline exactness, though the reference current mistake is dismissed. Notwithstanding, for charge balance principle (CBP)- based DSCM (CBP-DSCM) control, this paper demonstrates that the reference current ought to be remunerated in an equivalent amount to that of watched current. Something else, single or unequal pay prompts yield voltage consistent state mistake. Consequently, a double present mistake pay methodology for CBP-DSCM control is proposed. It repays the blunders in an equivalent amount through a present mistake spectator, which considers parasitics and figures the present blunders without guess. To confirm the proposed methodology, little sign models with parasitics for both the converter and the controller are developed by differential elements of key factors. Moreover, converter security is examined at regular task condition, while the dependability at different activity conditions is verified through vigor examination. At long last, recreations and trial al results confirm the examination and the improved transient reaction of the converter.

Key words: Discontinuous Conduction Mode, Charge balance, pulse frequency modulation, Dual Current Error, Electromagnetic Interface.

INTRODUCTION

DISCONTINUOUS conduction mode (DCM) dc– dc converters have been broadly utilized in power factor correction (PFC) and low-to medium-power applications [1]–[3]. They sometimes fall short for high-power applications, inferable from the high current swell, which builds weight on gadgets, electromagnetic obstruction (EMI), and power misfortune. Moreover, they experience the ill effects of a low power factor in PFC applications [4]. By and by, they have points of interest, for example, end of diode turn around recuperation, basic compensation for voltage circle, high data transfer capacity, com-agreement and minimal effort inductor, and so forth [5]–[7]. To research DCM converters, fundamental little sign models were proposed, basing on a regular state-space averaging technique [8]. Time-space models

were proposed in [9], where the converter soundness was examined. With the thought of parasitics, a formally dressed model was likewise proposed in [10]. All previously mentioned models give a manual for breaking down and control of DCM converters.

To improve the presentation of DCM converters, different control systems with various balance techniques have been explored. As for tweak type, beat width adjustment (PWM), beat recurrence balance (PFM), and hysteretic balance are broadly utilized. Among them, hysteretic tweak is outstanding for its intrinsic effortlessness and wide unique range [11], [12]. As a huge sign strategy, it utilizes a hysteretic comparator in the control circle to block the danger of modulator immersion [13]. PFM regulation abatements exchanging recurrence in extent to stack current, which improves transformation efficiency at light burden by diminishing exchanging misfortunes [14].

In any case, hysteretic and PFM converters have variable exchanging frequencies and along these lines can't be modeled and broke down by the state-space averaging technique [15]. Also, hysteretic tweak converters have huge yield voltage swell in view of their variable obligation proportions in relentless state. For PWM converters, distinctive propelled control methodologies are examined. Among them, CBP-based techniques are considered as a sort of "ideal control" since they are fit for limiting voltage deviation and recuperation time of a converter experiencing a heap or line transient occasion. Meyer et al. utilized the rule and proposed a simple control procedure, which is straightforward, quick, and without enduring state error [16]. Be that as it may, this methodology can't be acknowledged through computerized control.

Moreover, they proposed a "mixture" analog– advanced (AD) acknowledgment for this procedure [17], [18]. By and by, the simple inspecting circuit was as yet used, so as to obtain a nonstop yield voltage. For advanced control, Qiu et al. structured a CBP-DSCM controller, which does not require a constant yield voltage and along these lines separates simple testing circuits. [19] It performs current-mode control with a current eyewitness, which spares a current sensor like other DSCM controllers for ceaseless conduction mode converters [20], [21]. Notwithstanding, current errors and yield voltage relentless state error have not been contemplated. Current guideline exactness can be additionally improved. What's more, converter security ought to be broke down, and heartiness investigation ought to be additionally completed to confirm framework solidness at different task conditions [22].

This paper contemplates current errors and yield voltage enduring state error in a CBP-DSCM-controlled dc– dc converter. Customarily, the watched current is remunerated to expand current guideline exactness, while the reference current error is dismissed. In any case, investigation demonstrates that compensation for watched current ought to be equivalent to that of reference current. Something else, single or unequal compensation prompts yield voltage unfaltering state error. To maintain a strategic distance from this disadvantage, a dual current error compensation (DCEC) procedure for CBP-DSCM control is proposed. It depends on a current error eyewitness, which considers parasitics and computes the current errors without estimate. The proposed control technique has points of interest of quick transient reaction and high heartiness against line voltage, yield voltage, and

International Journal of Research
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e-ISSN: 2348-6848
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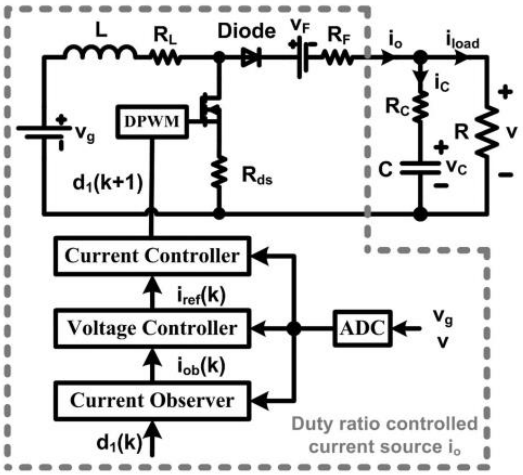

Fig. 1. CBP-DSCM-controlled boost converter.

A non-isolated Ćuk converter comprises two inductors, two capacitors, a switch (usually a transistor), and a diode. Its schematic can be seen in figure 1. It is an inverting converter, so the output voltage is negative with respect to the input voltage.

The capacitor C is used to transfer energy and is connected alternately to the input and to the output of the converter *via* the commutation of the transistor and the diode (see figures 2 and 3).

The two inductors L_1 and L_2 are used to convert respectively the input voltage source (V_i) and the output voltage source (C_o) into current sources. Indeed, at a short time scale an inductor can be considered as a current source as it maintains a constant current. This conversion is necessary because if the capacitor were connected directly to the voltage source, the current would be limited only by (parasitic) resistance, resulting in high energy loss. Charging a capacitor with a current source (the inductor) prevents resistive current limiting and its associated energy loss.

As with other converters (buck converter, boost converter, buck-boost converter) the Ćuk converter can either operate in continuous or discontinuous current mode. However, unlike these converters, it can also operate in discontinuous voltage mode (i.e., the voltage across the capacitor drops to zero during the commutation cycle).

Continuous mode

In steady state, the energy stored in the inductors has to remain the same at the beginning and at the end of a commutation cycle. The energy in an inductor is given by:

$$E = \frac{1}{2}LI^2$$

This implies that the current through the inductors has to be the same at the beginning and the end of the commutation cycle. As the evolution of the current through an inductor is related to the voltage across it:

$$V_L = L\frac{dI}{dt}$$

it can be seen that the average value of the inductor voltages over a commutation period have to be zero to satisfy the steady-state requirements.

If we consider that the capacitors C and C_o are large enough for the voltage ripple across them to be negligible, the inductor voltages become: in the off-state, inductor L_1 is connected in series with V_i and C (see figure 2). Therefore $V_{L1} = V_i - V_C$. As the diode D is forward biased (we consider zero voltage drop), L_2 is directly connected to the output capacitor. Therefore $V_{L2} = V_o$

 in the on-state, inductor L_1 is directly connected to the input source. Therefore $V_{L1} = V_i$. Inductor L_2

International Journal of Research
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e-ISSN: 2348-6848
p-ISSN: 2348-795X
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is connected in series with C and the output capacitor, so $V_{L2} = V_O + V_C$

The converter operates in on-state from t=0 to t=D·T (D is the duty cycle), and in off state from D·T to T (that is, during a period equal to (1-D)·T). The average values of V_{L1} and V_{L2} are therefore:

$$\bar{V}_{L1} = D \cdot V_i + (1-D) \cdot (V_i - V_C) = (V_i - (1-D) \cdot V_C)$$

$$\bar{V}_{L2} = D\,(V_o + V_C) + (1-D) \cdot -V_o = (V_o + D \cdot V_C)$$

As both average voltage have to be zero to satisfy the steady-state conditions we can write, using the last equation:

$$V_C = \frac{V_o}{D}$$

So the average voltage across L_1 becomes:

$$\bar{V}_{L1} = \left(V_i + (1-D) \cdot \frac{V_o}{D}\right) = 0$$

$$\frac{V_o}{V_i} = \frac{D}{1-D}$$

It can be seen that this relation is the same as that obtained for the Buck-boost converter.

Discontinuous mode

Like all DC-DC converters Cuk converters rely on the ability of the inductors in the circuit to provide continuous current, in much the same way a capacitor in a rectifier filter provides continuous voltage. If this inductor is too small or below the "critical inductance", then the current will be discontinuous. This state of operation is usually not studied too much depth, as it is not used beyond a demonstrating of why the minimum inductance is crucial.

The minimum inductance is given by:

$$L_1 min = \frac{(1-D)^2 R}{2 D f_s}$$

Where f_S is the switching frequency.

BASIC CBP-DSCM CONTROLLER FOR DCM CONVERTERS

For DCM converters, the inductor current must reach zero before the end of switching cycle. Thus, it is not related to currents of previous cycles and can be tightly controlled by PWM duty ratio. As a result, the converter can be regarded as a duty-ratio-controlled current source, which charges the output network. This is the fundamental for CBP-DSCM control.

Here, a boost converter is used as a demonstration. The control strategy is generalized for other basic converters later in Section III.

A CBP-DSCM-controlled boost converter is shown in Fig. 1, where k denotes the switching cycle, d_1 is the duty ratio of digital PWM (DPWM) signal, C is the output capacitance, R is the load resistance. i_C , i_{ob}, i_o, i_{load}, i_{ref} , v_g , v_C , and v are the charge current of the capacitor, the observed current, the output current, the load current, the reference current, the line voltage, the voltage on the ideal capacitor, and the output voltage, respectively. R_C , R_L , R_F , v_F , and R_{ds} denote the equivalent series resistance (ESR) of the capacitor, the equivalent resistance of the inductor, the diode conduction resistance, the diode forward voltage, and the MOSFET conduction resistance, respectively.

The CBP-DSCM controller consists of three basic modules, which are the voltage controller, the current observer, and the current controller. Among them, the

International Journal of Research
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e-ISSN: 2348-6848
p-ISSN: 2348-795X
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voltage controller calculates i_{ref} based on i_{ob}, v, and CBP. The current observer estimates i_o and outputs i_{ob} to the voltage controller, while the current controller outputs d_1 to control i_o. Next, all the modules will be discussed in detail.

A. Voltage Controller

According to CBP, variation of v_C in one switching cycle depends on the capacitor charge current $i_C = i_o - i_{load}$. Therefore, variation of v can be controlled by i_o since $v \approx v_C$. As shown in Fig. 2, v is lower than v_{ref} in the kth switching cycle

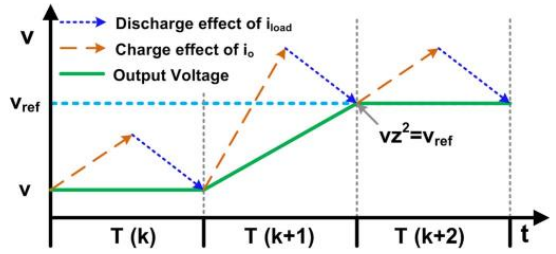

Fig. 2. Voltage regulation process based on CBP.

In order to control the output voltage, i_o is regulated according to $v_{ref} - v$ and i_{ob}. By increasing (or decreasing) the charge effect of i_o in the $(k+1)$th switching cycle, v is regulated to v_{ref} at the beginning of the $(k+2)$th switching cycle.

Since capacitor voltage is determined by its charge current, variation of v_C in one switching cycle T is given by

$$v_C z - v_C = \frac{T}{C} i_C = \frac{T}{C}(i_o - i_{load}). \quad (1)$$

where i_{load} is substituted by v/R. In order to achieve the voltage control strategy, the relationship between $i_o z$ and vz^2 should be derived. However, vz and R cannot appear in the control strategy since they are unknown. Therefore, (2) is multiplied by a differential factor $(z + 1 - z^{-1} - z^{-2})$ and is given by

$$vz - v = \frac{T}{C}(i_o - i_{load}) - i_{load} R_C (z-1)$$
$$= \frac{T}{C}\left(i_o - \frac{v}{R}\right) - \frac{R_C v}{R}(z-1) \quad (2)$$

Supposing that T RC and R_C R, then the relationship between $i_o z$ and vz^2 is given by

$$v(z^2 - 2 + z^{-2}) = \frac{T}{C} i_o (z + 1 - z^{-1} - z^{-2})$$
$$- \frac{vT}{RC}(z + 1 - z^{-1} - z^{-2}) - \frac{R_C v}{R}(z^2 - 2 + z^{-2}). \quad (3)$$

Finally, $i_o z$ and vz^2 are taken as the reference current and the reference voltage, respectively. After replacing i_o by i_{ob}, the voltage control strategy is given by

$$v(z^2 - 2 + z^{-2}) \approx \frac{T}{C} i_o (z + 1 - z^{-1} - z^{-2}). \quad (4)$$

$$i_{ref} = i_o z = i_{ob}(z^{-1} + z^{-2} - 1) + \frac{C}{T}(v_{ref} - 2v + vz^{-2}). \quad (5)$$

Based on (5), the reference current is calculated by the reference voltage, which can be used to regulate the output voltage. However, i_{ob} must be acquired from the current ob- server. Furthermore, i_{ref} must be processed to d_1 to control the output current.

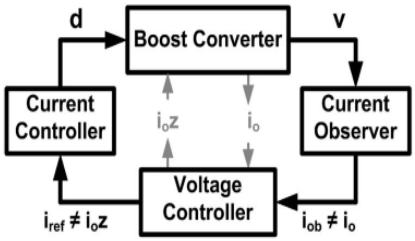

Fig. 3. Current errors in the converter.

B. Current Observer and Current Controller

Both the current observer and the current controller exploit the energy conservation principle of inductor. For DCM converters, charge and discharge energy of the inductor are equal in one switching cycle since the inductor current must reach zero before the end of the cycle. For an ideal boost converter, the charge and discharge energy

International Journal of Research
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e-ISSN: 2348-6848
p-ISSN: 2348-795X
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are v)T , respectively [23]. Therefore, the energy conservation equation is given by

$$\frac{v_g^2 d_1^2 T^2}{2L} = i_o(v - v_g)T. \quad (6)$$

Based on (6), an output current is derived according to v_g , v, and d_1 , which obtains (7) for the current observer. That is

$$i_{ob} = \frac{d_1^2 T v_g^2}{2(v - v_g)L}. \quad (7)$$

For the current controller, (8) is derived by substituting i_{ref} for i_O in (6). That is,

$$d_1 = \sqrt{\frac{2(v - v_g)Li_{ref}}{Tv_g^2}}. \quad (8)$$

The basic CBP-DSCM controller is implemented with (5), (7), and (8). According to Fig. 2, the output voltage can be regulated to v in two switching cycles. However, parasitics are not considered, which lead to errors in both I . These errors degrade the dynamic response by decreasing cur- rent regulation accuracy. Therefore, compensation is required to reduce the errors.

$$i_o = \frac{d_1^2 T v_g^2}{2L(v + v_F - v_g)}. \quad (9)$$

D

CEC FOR CBP-DSCM CONTROL

As shown in Fig. 3, the voltage controller is designed to regulate I are not considered in the energy conservation equation (6). This causes errors in both observed current and reference current. The observed current error Δi , whereas the reference current error Δi .Current errors occur in a basic CBP-DSCM controller. Con- is compensated to increase current regulation is neglected. However, the following analysis proves that the reference current should be compensated in a same quantity to that of the observed current. Otherwise, single or unequal compensation leads to output voltage steady-state error (Δv) , a DCEC strategy is proposed. It compensates the errors in a same quantity through a current error observer, which considers parasitics and calculates the errors without approximation.

$$\Delta i_{ob} = i_{ob} - i_o = \Delta i_{ref} = i_{ref} - i_o = \frac{v_F}{v - v_g} i_o. \quad (10)$$

A. Observed and Reference Current Errors

Parasitics lead to current errors by affecting the charge and discharge energy of the inductor. For example, the discharge energy changes to I affects the voltage on the inductor when the main switch is off. Therefore, energy conservation equation (6) should be modified, which derives an output current

$$i_o = \frac{v}{Z} = \frac{v_g M_1}{Z} \quad (11)$$

As a result, current errors are induced as

$$\Delta i_{ob} = \Delta i_{ref} = \frac{v_g}{Z}(M_0 - M_1). \quad (12)$$

Other parasitics also enlarge the current errors by causing more energy loss in the converter. This can be proved by the relationship between current errors and the conversion ratio of the converter.

Equation (12) indicates that Δi_{ob} and Δi_{ref} are equal and proportional to conversion ratio error $M_0 - M_1$. Owing to the energy loss caused by parasitics, M_0 is always larger than M_1 , which ensures positive current errors. Large parasitics cause high energy loss, conversion ratio error, and current errors.

B. Output Voltage Steady-State Error

To reduce the current errors, compensation is required. How- ever, for CBP-DSCM control, this could lead to steady-state error on the output voltage. From (4) and (5), voltage error is given by

$$v_{ref} - vz^2 = \frac{T}{C}\left[\Delta i_{ref} + \Delta i_{ob}(1 - z^{-1} - z^{-2})\right]. \quad (13)$$

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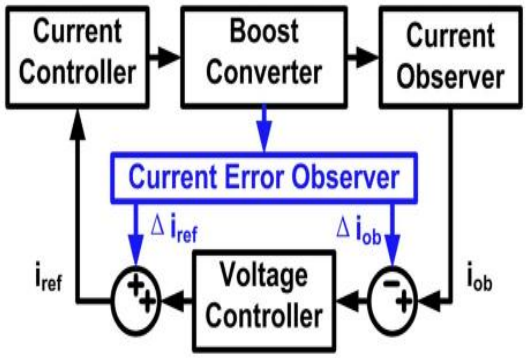

Fig. 4. DCEC for CBP-DSCM-controlled boost converter.

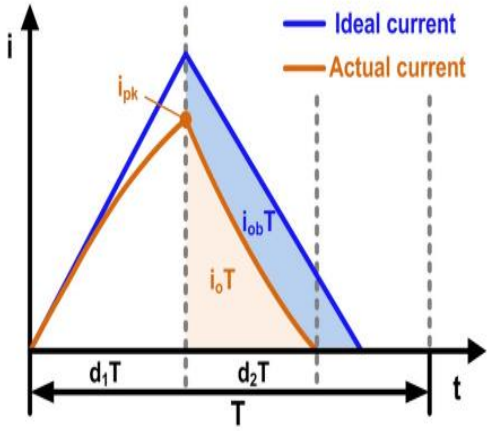

Fig. 5. Actual and ideal inductor currents.

In steady state, all variables in (13) do not change along with k. Therefore, the output voltage steady-state error is given by

$$(\Delta v)_{\rm ss} = (v_{\rm ref} - v)_{\rm ss} = \frac{T}{C}(\Delta i_{\rm ref} - \Delta i_{\rm ob})_{\rm s}$$

$$(\Delta v)_{\rm ss} = \frac{T}{C}(\Delta i_{\rm ref})_{\rm ss} = \frac{T v_g}{RC}(M_0 - M_1)_{\rm ss}.$$

Since the output voltage steady-state error is led by single or unequal compensation, $i_{\rm ob}$ and $i_{\rm ref}$ should be compensated in a same quantity.

B. DCEC

DCEC compensates the observed and reference currents in a same quantity. This increases current regulation accuracy without inducing output voltage steady-state error. As shown in Fig. 4, the compensation is realized by using a current error observer, which calculates the current errors and compensates for both $i_{\rm ob}$ and $i_{\rm ref}$.

To derive the observation strategy, parasitics are considered, and the current errors are calculated without approximation. Both ideal and actual inductor currents are given in Fig. 5, where $i_o\,T$ is the charge to the output network, $i_{\rm ob}T$ is the observed charge, and $i_{\rm pk}$ is the peak value of actual current.

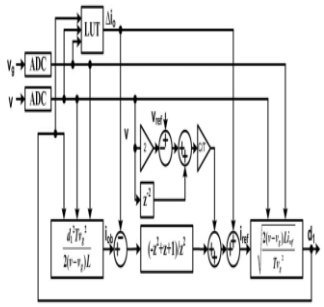

Fig. 6. Block diagram of the converter.

When the main switch is on, the voltage on the inductor is $v_g - (R_L + R_{ds})i_{d1}(t)$, where $i_{d1}(t)$ denotes the actual induc- tor current during $d_1\,T$. Therefore, the difference equation of $i_{d1}(t)$ is given by

$$\begin{cases} L\frac{di_{d1}(t)}{dt} = v_g - (R_L + R_{ds})i_{d1}(t) \\ i_{d1}(t)|_{t=0} = 0 \end{cases} \quad (16)$$

where $i_{d1}(t)$ is given by

$$i_{d1}(t) = \frac{v_g}{R_L + R_{ds}}\left(1 - e^{-\frac{R_L+R_{ds}}{L}t}\right). \quad (17)$$

Moreover, substituting $t = d_1 T$ into (17) yields

$$\begin{cases} i_{\rm pk} = P_{\rm damp1} v_g d_1 T/L \\ P_{\rm damp1} = \frac{L\left(1-e^{-(R_L+R_{ds})d_1 T/L}\right)}{d_1 T(R_L+R_{ds})} \end{cases} \quad (18)$$

where $P_{\rm damp1}$ denotes the damping ratio of peak current, i.e., the ratio of $i_{\rm pk}$ to the ideal peak current. It equals to 1 when all parasitics are zero.

Furthermore, the actual inductor current during $d_2\,T$ is de- rived, which is denoted by $i_{d2}(t)$. Since the voltage on the inductor is $v_g - v_F - v - (R_L + R_F)i_{d2}(t)$

International Journal of Research
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e-ISSN: 2348-6848
p-ISSN: 2348-795X
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when the main switch is off, the difference equation of $i_{d2}(t)$ is given by

$$\begin{cases} L\frac{di_{d2}(t)}{dt} = v_g - v_F - v - (R_L + R_F)i_{d2}(t) \\ i_{d2}(t)|_{t=d_1T} = i_{\rm pk} \end{cases} \quad (19)$$

where $i_{d2}(t)$ is given by

$$i_{d2}(t) = \frac{v_g - v_F - v}{R_L + R_F} + \left(i_{\rm pk} - \frac{v_g - v_F - v}{R_L + R_F}\right) e^{-\frac{R_L+R_F}{L}(t-d_1T)}. \quad (20)$$

Since i_oT is an integration of i_{d2} (t) during d_2T, substituting $i_{d2}(t)|_{t=d_1T+d_2T} = 0$ into (20) derives d_2T as

$$\begin{cases} d_2T = \frac{i_{\rm pk}L}{v - v_g} P_{\rm damp2} \\ P_{\rm damp2} = \frac{v - v_g}{i_{\rm pk}(R_L + R_F)} \ln\left[1 + \frac{i_{\rm pk}(R_L + R_F)}{v + v_F - v_g}\right] \end{cases} \quad (21)$$

where $P_{\rm damp2}$ is the damping ratio of d_2T. Similarly, $P_{\rm damp2}$ equals to 1 when all parasitics are zero. By integration, i_o is written as

$$\begin{cases} i_o = \frac{1}{T}\int_{d_1T}^{d_1T+d_2T} i_{d2}(t)dt = \frac{d_1^2Tv_g^2}{2(v - v_g)L} P_{\rm damp3} \\ P_{\rm damp3} = \frac{(v - v_g) - (v + v_F - v_g)P_{\rm damp2}}{i_{\rm pk}(R_L + R_F)} 2P_{\rm damp1}^2 \end{cases} \quad (22)$$

where $P_{\rm damp2}$ is the damping ratio of i_o, which also equals to 1 when all parasitics are zero.

Finally, based on (7), (8), and (22), current errors are given by

$$\Delta i_{\rm ob} = \Delta i_{\rm ref} = \frac{d_1^2Tv_g^2}{2(v - v_g)L} - \frac{(v_g - v_F - v)d_2 + i_{\rm pk}L/T}{R_L + R_F}. \quad (23)$$

Equation (23) can be used to compensate for both I . Since the currents are compensated in a same quantity, current regulation accuracy is increased, while the output voltage steady-state error is eliminated. Although the calculation process is relatively complex, it can be carried out offline. As shown in Fig. 6, the compensation strategy is implemented by a lookup-table method. A 3-D table is used to acquire the current error, which is calculated according to nominal values of parasitics and parameters of devices.

D .Generalization for Other Basic Converters

The proposed control strategy can be easily generalized for other basic converters, i.e., buck converter and buck–boost converter. Since capacitor CBP is still valid for the basic converters, the voltage controller remains the same, which is based on (5). However, since the converters have different inductor currents, some modifications have to be made for current observer, current controller, and current compensation strategy. To generalize the control strategy for buck and buck–boost converters, relevant equations are given in Table I. Equations of are basic current observation and control strategies, while Δi is used for DCEC. Among isolative converters, the fly back converter is widely used for DCM applications. Since it is based on buck–boost converters, the basic CBP-DSCM control strategy remains the same. However, transformer winding ratio, winding resistances, and leakage inductances should be considered for compensation strategy modification, which will be studied in future work.

MODELING AND STABILITY AND ROBUSTNESS ANALYSIS

The small-signal model for CBP-DSCM-controlled converter is shown in Fig. 7, where Gvd(s) and hdv(z) are (z) are transfer functions from d1 to v and from Δv to d, respectively. To verify the converter stability and robustness, accurate,

TABLE I
GENERALIZATION FOR BUCK AND BUCK–BOOST CONVERTERS

	Buck	Buck-boost
i_{ob}	$\frac{d_1^2Tv_g^2}{2vL}$	$\frac{d_1^2Tv_g^2}{2vL}$
d_1	$\sqrt{\frac{2vLi_{ref}}{v_g(v_g-v)T}}$	$\sqrt{-\frac{2vLi_{ref}}{v_g^2T}}$
i_{pk}	$\begin{cases} i_{pk} = P_{damp1}(v_g - v)d_1T/L \\ P_{damp1} = \frac{L(1-e^{-(R_L+R_{ds})d_1T/L})}{d_1T(R_L+R_{ds})} \end{cases}$	$\begin{cases} i_{pk} = P_{damp1}v_gd_1T/L \\ P_{damp1} = \frac{L(1-e^{-(R_L+R_{ds})d_1T/L})}{d_1T(R_L+R_{ds})} \end{cases}$
d_2T	$\begin{cases} d_2T = P_{damp2}(v_g - v)d_1T/v \\ P_{damp2} = \frac{vL}{(v_g-v)d_1T(R_L+R_F)}\ln[1+\frac{i_{pk}(R_L+R_F)}{v_F+v}] \end{cases}$	$\begin{cases} d_2T = P_{damp2}v_gd_1T/v \\ P_{damp2} = \frac{vL}{v_gd_1T(R_L+R_F)}\ln[1+\frac{i_{pk}(R_L+R_F)}{v_F+v}] \end{cases}$
i_o	$\begin{cases} i_o = \frac{d_1^2T(v_g-v)v_g}{2vL}P_{damp3} \\ P_{damp3} = \frac{2vL}{d_1v_gT}[\frac{1-P_{damp1}}{R_L+R_{ds}} - \frac{P_{damp1}[P_{damp2}(v_F+v)-v]}{v(R_L+R_F)}] \end{cases}$	$\begin{cases} i_o = -\frac{d_1^2Tv_g^2}{2vL}P_{damp3} \\ P_{damp3} = \frac{2L[vP_{damp1}-(v+v_F)P_{damp2}]}{d_1Tv_g(R_L+R_F)} \end{cases}$
Δi_o	$d_1(v_g-v)[\frac{d_1Tv_g}{2vL} - \frac{1-P_{damp1}}{R_L+R_{ds}} + \frac{P_{damp1}[P_{damp2}(v_F+v)-v]}{v(R_L+R_F)}]$	$-\frac{d_1^2Tv_g^2}{2vL} + d_1v_g\frac{P_{damp1}-(1+v_F/v)P_{damp2}}{R_L+R_F}$

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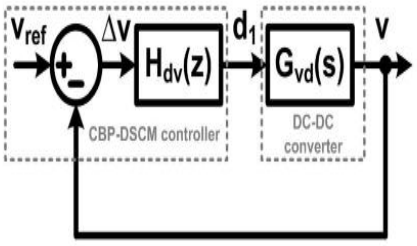

Fig. 7. Small-signal model for CBP-DSCM-controlled converter.

expressions for both $G_{vd}(s)$ and $H_{dv}(z)$ should be derived with consideration of parasitics.

In the following, $G_{vd}(s)$ is constructed by the differential function of i_o and the transfer function of output filtering network, while $H_{dv}(z)$ is derived by differential functions of d_1 i_{ob} and i_{ref} Furthermore, converter stability is proved by the system open-loop Bode diagram. Finally, converter robustness is verified by the system closed-loop root locus versus parasitics and inductor value.

A. Accurate Models for Both the Converter and the CBP-DSCM Controller With DCEC

An accurate model for the converter is derived through the differential function of i_o.According to (22), v, v_g and $d_1$determine i_o. . Therefore, their small-signal variations $\{d_1, v_g, v\}$ are introduced to derive the differential function of i_o as follows:

$$\begin{cases} \hat{i}_o = X_1\hat{d}_1 + X_2\hat{v}_g + X_3\hat{v} \\ X_1 = \dfrac{i_{pk}[v_g - i_{pk}(R_L+R_{ds})]}{(v+v_F-v_g)+i_{pk}(R_L+R_F)} \\ X_2 = i_{pk}^2\dfrac{L}{T}\dfrac{(v-v_g)/v_g + P_{damp2} - P_{damp3}/(2P_{damp1}^2)}{[v+v_F-v_g+i_{pk}(R_L+R_F)](v-v_g)} \\ X_3 = \dfrac{Li_{pk}^2}{T}\dfrac{P_{damp3}/(2P_{damp1}^2) - P_{damp2}}{(v-v_g)[v+v_F-v_g+i_{pk}(R_L+R_F)]} \end{cases} \quad (24)$$

Where X_1, X_2, X_3 denote partial differential functions $\partial i_o/\partial d_1$, $\partial i_o/\partial v_g$, $\partial i_o/\partial v$, respectively. On the other hand, according to the transfer function of output filtering network, the relationship between $\hat{v}$ and $\hat{i}_o$ is given by

$$\hat{v} = \hat{i}_o\frac{(sCR_C+1)R}{sC(R+R_C)+1}. \quad (25)$$

Based on (24) and (25), $G_{vd}(s)$ is obtained as

$$G_{vd}(s) = \left.\frac{\hat{v}}{\hat{d}_1}\right|_{\hat{v}_g=0} = \frac{X_1R(sR_CC+1)}{sC(R+R_C-X_3RR_C)+1-X_3R}. \quad (26)$$

Furthermore, the transfer function of CBP-DSCM controller is derived through differential functions of d_1, i_{ob} and i_{ref} . Based on (8), the differential function of d_1 is given by

$$\hat{d}_1 = \frac{1}{v_g}\sqrt{\frac{L}{2(v-v_g)Ti_{ref}}}\left[i_{ref}\hat{v} + \frac{v_g-2v}{v_g}i_{ref}\hat{v}_g + (v-v_g)\hat{i}_{ref}\right]. \quad (27)$$

Based on the observed current with compensation, the differential function of i_{ob} is derived through (7) and (23), which is shown as follows:

$$\hat{i}_{ob} = X_1\hat{d}_1 + X_2\hat{v}_g + X_3\hat{v}. \quad (28)$$

Based on the reference current with compensation, (5) and (23) yield the differential function of i_{ref} as follows:

$$\hat{i}_{ref} = (z^{-1}+z^{-2}-2)\hat{i}_{ob} + \frac{d_1^2Tv_g(2v-v_g)}{v-v_g}\hat{v}_g + \frac{d_1Tv_g^2}{(v-v_g)L}\hat{d}_1 + \left[\frac{C}{T}(-2+z^{-2}) - \frac{d_1^2Tv_g^2}{2L(v-v_g)^2}\right]\hat{v}. \quad (29)$$

Since (27)–(29) contain five variables $\{\hat{i}_{ob}, \hat{v}, \hat{v}_g, \hat{d}_1, \hat{i}_{ref}\}$, they give the differential function $\hat{d}_1 = f(\hat{v}_g, \hat{v})$. Furthermore,since $\Delta v = v_{ref} - v$, where v_{ref} can be taken as constant, $H_{dv}(z)$ is obtained as

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$$H_{dv}(z) = \left.\frac{\hat{d}_1}{\Delta\hat{v}}\right|_{\hat{v}_g=0} = -\left.\frac{\hat{d}_1}{\hat{v}}\right|_{\hat{v}_g=0}$$
$$= \frac{X_3}{X_1}\frac{2(1+C/T/X_3) - z^{-1} - (1+C/T/X_3)z^{-2}}{2 - z^{-1} - z^{-2}} \quad (30)$$

where the dominator can be transformed to the continuous-time domain as

$$2 - z^{-1} - z^{-2}\big|_{z=e^{sT}} = sT\sum_{n=0}^{+\infty}\frac{1+2^{n+1}}{(n+1)!}(-sT)^n. \quad (31)$$

Since the dominator contains an integral factor, an infinite dc gain is made from Δv to d_1, which eliminates the output voltage steady-state error.

B. Stability Analysis

In order to explore frequency characteristics, system stability is analyzed in the s-domain. The transition between continuous- and discrete-time domains is done using transformation techniques. Based on the approximation of discrete-time domain operator z, Euler's transformation method is used to derive a continuous-time domain transfer function from Δv to d_1, which is shown as follows:

$$H_{dv}(s) = \frac{X_3}{X_1}\frac{C/T/X_3 + sT(3+2C/T/X_3)}{3sT}. \quad (32)$$

Therefore, the system open-loop transfer function is given by

$$G_{vd}(s)H_{dv}(s) = \frac{R(sR_CC+1)}{3sT}\frac{C/T+sT(3X_3+2C/T)}{sC(R+R_C-X_3RR_C)+1-X_3R}. \quad (33)$$

To obtain the crossover frequency and phase margin, parasitics are ignored, which yields

$$G_{vd}(s)H_{dv}(s) \approx \frac{RC}{3sT^2}\frac{1+sT\{3vT/[(v-v_g)RC]+2\}}{sRC+1+v/(v-v_g)}. \quad (34)$$

Supposing that the frequency of RC pole is much lower than both switching frequency and crossover frequency, then (34) approximates (35) near the crossover frequency. That is,

$$G_{vd}(s)H_{dv}(s) \approx \frac{1+2sT}{3s^2T^2}. \quad (35)$$

Based on (35), the crossover frequency and phase margin are solved as $f_c \approx 0.8/2\pi T$ Hz and and 58° respectively. In order to verify the analysis, a DCM boost converter is constructed in Simulink. Its main specifications are v_g = 10v, v_{ref} =15, V, L =3.8 μH, C =25 μF, R =30 Ω, and T =10μs. Parasitics are Rc=30mΩ, R_F = 100 mΩ, v = 0.7 V, R_L = 100 mΩ, and R = 100 mΩ. System open-loop Bode diagrams are plotted, which are based on (33) and (34),

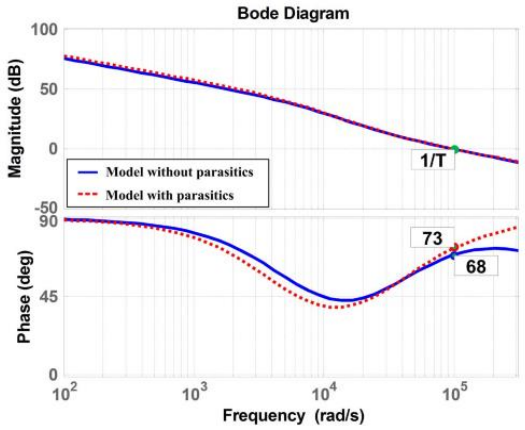

Fig. 8. System open-loop Bode diagrams.

respectively, to verify the effect of parasitics. As shown in Fig. 8, parasitics have minor impact on the open-loop frequency characteristic. The crossover frequencies are $f_c \approx 1/2\pi T$ Hz, which are close to one-sixth of switching frequency. The phase margins are 68° for the ideal system and 73° when parasitics are considered.

C. Robustness Analysis

Robustness analysis is carried out, in order to verify system stability at various operation conditions. Both operations of the converter and controller should be considered. Suppose that the converter operates with parameters {v_g ,v, R, L, C, R_{ds}, R_L,R_F,R_C,V_F}, whereas the controller is set with parameter values $\{v_g', v', L', C', R_{ds}', R_L', R_F', R_C', v_F'\}$.

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Among all these parameters, $\{L', C', R'_{ds}, R'_L, R'_F, R'_C, v'_F\}$ are measured offline as nominal values, {v'g, v'} are sampled and thus {v'g, = vg, v'= v}whereas R is not required by the controller. As a result, the damping ratios and partial differential functions are rewritten as $\{P'_{damp1}, P'_{damp2}, P'_{damp3}, X'_1, X'_2, X'_3\}$ for the controller and $\{P_{damp1}, P_{damp2}, P_{damp3}, X_1, X_2, X_3\}$ for the converter, respectively.

Since the controller is digital, the following analysis is carried out in the z-domain to acquire a more accurate result. Converter robustness is verified by the system closed-loop root locus. Models for the converter and controller in the z-domain are given by

$$\begin{cases} G_{vd}(z) = X_1 R \frac{R_C z - R_C + T/C}{(R + R_C - X_3 R R_C) z + (1 - X_3 R)(R_C + T/C) - R} \\ H'_{dv}(z) = \frac{X'_3}{X'_1} \frac{2(1 + C/T/X'_3) - z^{-1} - (1 + C/T/X'_3) z^{-2}}{2 - z^{-1} - z^{-2}}. \end{cases} \quad (36)$$

As a result, the system closed-loop transfer function is given by

$$\frac{G_{vd}(z) H'_{dv}(z)}{1 + G_{vd}(z) H'_{dv}(z)}. \quad (37)$$

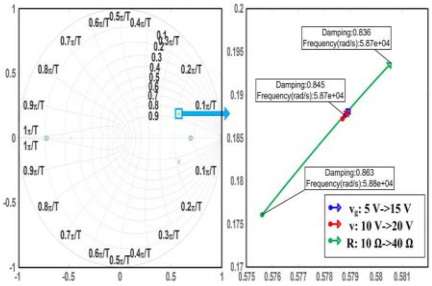

Fig. 9. System closed-loop root locus versus v_g, v, and R.

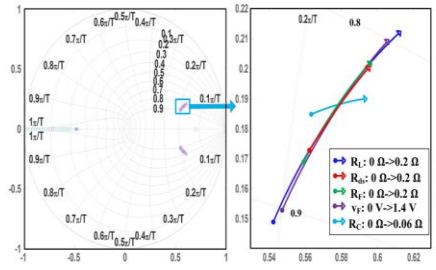

Fig. 10. System closed-loop root locus versus R_{ds}, R_L, R_F, R_C, and v_F.

Based on (37), the root locus versus $\{v_g, v, R, L, C, z\, R_{ds}, R_L, R_F, R_C, v_F\}$ are plotted, respectively. When $\{v_g, v, R\}$ change by {vg:5 V− > 1V, v:10 V− > 20 V, R : 10 Ω− > 40 Ω}, the root loci are shown in Fig. 9.The simulation results indicate that both the natural resonant frequency and the damping factor of the system have slight change along variations of {vg,v ,R}Because {vg,v}are fed to duty ratio, while the controller regulates output voltage based on CBP, which does not concern load resistance, the system is highly robust against variations of {vg,v ,R}.In addition $\{L, C, R_{ds}, R_L, R_F, R_C, v_F\}$ are measured offline and set as nominal values $\{L', C', R'_{ds}, R'_L, R'_F, R'_C, v'_F\}$ in the controller. Therefore, system performance is degraded when these parameters change according to temperature, time and electromagnetism environment, etc. As shown in Fig. 10, when $\{R_{ds}, R_L, R_F, R_C, v_F\}$ change from zero to twice of their nominal values, both natural resonant frequencies and damping factors decrease, which indicate a degraded transient response. Nevertheless, the variations are small and acceptable. The system remains stable since all poles are inside the unit circle. When L and C change by L :1.9 μH− > 7.6 μHand C :12.5 μF− > 50 μF, respectively, the root loci are given in Fig. 11. Both natural resonant frequency and damping factor decrease. However, all poles are inside the unit circle, and the system remains stable.

SIMULATION RESULTS

A DCM boost converter is constructed in MATLAB Simulink to verify the proposed control strategy. Specifications of the converter are shown in Table II. Simulation results for both current errors and the output voltage steady-state error are given at full load.

A. Current Errors

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In Section III, the relationship between parasitics and cur- rent errors is derived. According to (10), the observed current error is $i_o/(v-v_g)$ = 0.3 times proportional to v_F , when other parasitics are zero. As shown in Fig. 12(a),the simulated error is Δi_{ob} = $0.32v_F$, , which proves (10). Further- more, Fig. 12(b) shows the simulated relationship between current errors and the conversion ratio error in steady state. When the duty ratio varies from 0.1 to 0.8, $(M_0 - M_1)_{ss}$ and

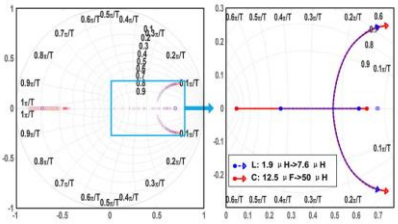

Fig. 11. System closed-loop root locus versus L and C.

TABLE II
SPECIFICATIONS OF THE TESTED BOOST CONVERTER

Inductance of the power inductor	3.8 μH
Capacitance of the output capacitor	25 μF
Line voltage	10 V
Output voltage	15 V
Rated output current (ROC)	0.75 A
Full load output current	1.5 A
Voltage ripple under ROC	2 %
Switching frequency	100 kHz

EXPERIMENTAL RESULTS

A DCM boost converter is constructed to verify the ef- fectiveness of the CBP-DSCM controller with DCEC (see Fig. 14). Experimental settings are as follows. System hard- ware includes a control part and a power part (see Table III). The control part and other software features are implemented using a Texas Instruments Digital Signal Processor (DSP) TMS320F2812. The power part includes a main power stage and signal sampling circuits. The switching device of the power stage is BSZ110N06NS3 MOSFET, the output capacitor is EEHZC1E101XP, and the diode is SB350. Line and output voltages are sampled by a 4-channel 12-bit AD converter chip (AD7934-6). Observed and reference currents are outputted in synchronization by 12-bit digital–analog chips (TLV5616) with a resolution of 0.2 V/A.

A. Current Errors

CBP-DSCM controllers with no compensation, single com- pensation, and DCEC are carried out by experiments to verify current errors. Output current equals to load current at steady state and reaches 1.5 A at full load. According to (23), current errors are 0.86 A for CBP-DSCM controller without compen- sation. As shown in Fig. 15, the measured errors are 0.9 A. For CBP-DSCM controller with single compensation, the observed current error decreases to 0.05 A, while the reference current error remains the same. For CBP-DSCM controller with DCEC, both current errors decrease to 0.05 A. All results prove the analysis about current errors in Section III.

B. Output Voltage Transients

To verify output voltage responses to line voltage and load disturbances, experiments are carried out for different control strategies. A voltage-mode controller and the CBP-DSCM con- trollers with no compensation, single compensation, and DCEC are tested for comparison.

1) Voltage-Mode Controller:

A voltage-mode controller with conventional proportional–integral (PI) feedback is carried out for comparison. The controller parameters are set as P = 0.15, I = 2400, to acquire a crossover frequency of 12 kHz. As shown in Fig. 16, when the line voltage steps up from 7.5 to 10 V, the output voltage increases by 700 mV and restabilizes in 120 μs. When the load steps from 20 Ω to the full-load resistance of 10 Ω, the output voltage decreases by 600 mV and restabilizes in 120 μs. Since integral feedback is used, steady- state error on the output voltage is eliminated. The results are used as a reference of performance.

2) CBP-DSCM Controller Without Compensation:

According to Section II, the CBP-DSCM controller regulates

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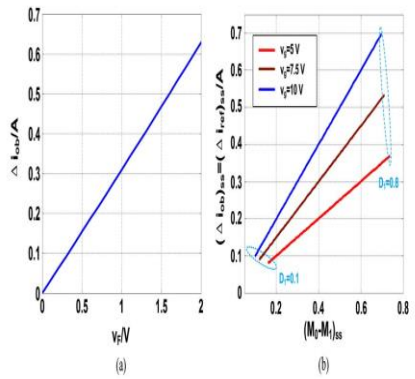

Fig. 12. Relationship between (a) $(\Delta i)_{ss}$ and v_F; (b) current errors and the conversion ratio error in steady state.

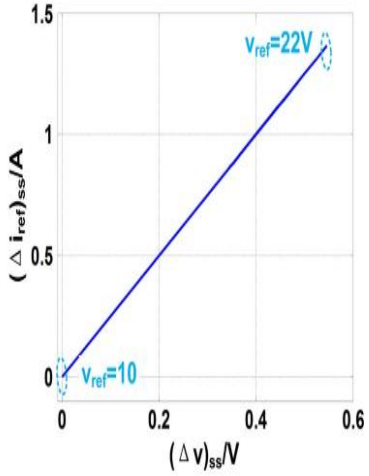

Fig. 13. Relationship between $(\Delta v)_{ss}$ and $(\Delta i_{ref})_{ss}$ for CBP-DSCM control with single compensation for observed current.

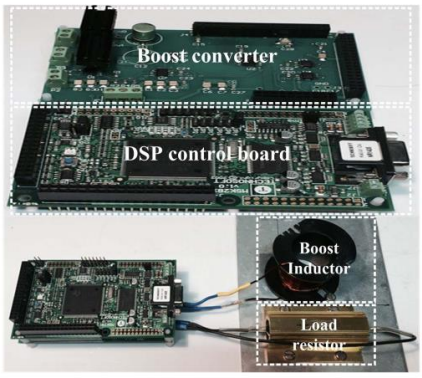

Fig. 14. Photograph of the prototype.

output voltage to its reference value in two switching cycles, which effectively increase the transient responses to line voltage and load disturbances. As shown in Fig. 17, for CBP- DSCM controller without compensation, when the line voltage steps up from 7.5 to 10 V, the output voltage increases by

TABLE III
SPECIFICATIONS OF HARDWARE PLATFORM

Inductance of power inductor	3.8 μH
Inductor winding resistance	0.105 Ω
Capacitance of the output capacitor	25 μF
ESR value of the output capacitor	0.03 Ω
MOSFET threshold voltage	3.5 V
MOSFET R_{ds}	0.1 Ω
Diode forward voltage	0.7 V
Diode forward resistance	0.1 Ω

400 mV and restabilizes in 80 μs. When the load steps from 20 Ω to 10 Ω, the output voltage decreases by 550 mV and restabilizes in 120 μs. The responses have smaller deviations and shorter regulation time than that of voltage-mode controller. However, the controller has not considered parasitics and can be improved by compensations.

3) CBP-DSCM Controller With Single Compensation:

For CBP-DSCM controller with single compensation, the observed current error is decreased, while the reference current error remains the same. According to (15), this causes steady- state error on the output voltage, which is verified by experimental results, as shown in Fig. 18. When the line voltage steps up from 7.5 to 10 V, the output voltage increases by 350 mV and restabilizes in 40 μs. When the load steps from 20 Ω to 10 Ω,the output voltage decreases by 500 mV and restabilizes in 80 μs. Although transient responses are improved by compensation, a steady-state error occurs on the output voltage. The error is 0.144 V according to (15) and the current errors measured earlier (typical operation), whereas in the experiments, it is 0.15 V under typical operation and 0.35 V when the load steps to 10 Ω.

4) CBP-DSCM Controller With DCEC

To eliminate the steady-state error, observed and reference currents are compensated in the same quantity by

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DCEC. The experimental results are shown in Fig. 19. When the line voltage steps up from 7.5 to 10 V, the output voltage decreases by 350 mV and restabilizes in 40 μs. When the load steps from 20 Ω to 10 Ω, the output voltage decreases by 500 mV and restabilizes in 60 μs. Compared with single-compensated CBP-DSCM, the controller achieves similar dynamic response, while eliminating the steady-state error on the output voltage. The

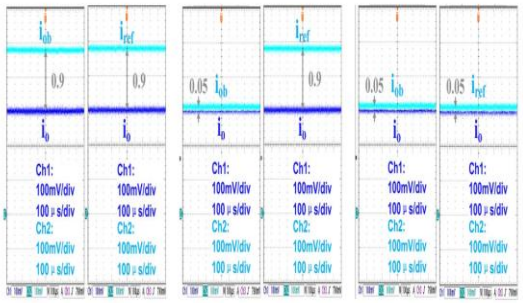

Fig. 15. Observed, reference, and output currents for CBP-DSCM controller with (a) no compensation, (b) single compensation, and (c) DCEC.

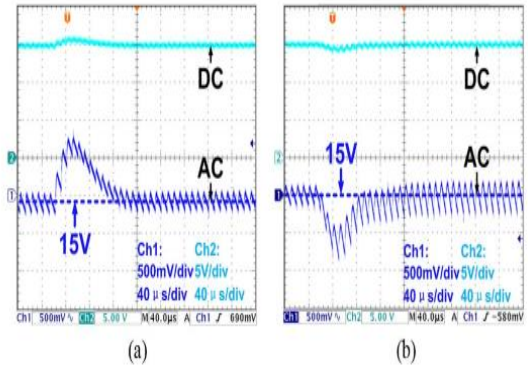

Fig. 16. For voltage-mode controller, output voltage transients when (a) line voltage steps from 7.5 to 10 V and (b) load steps from 20 Ω to 10 Ω.

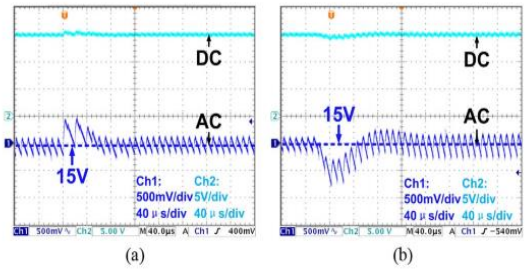

Fig. 17. For CBP-DSCM controller without compensation, output voltage transients when (a) line voltage steps from 7.5 to 10 V and (b) load steps from 20 Ω to 10 Ω.

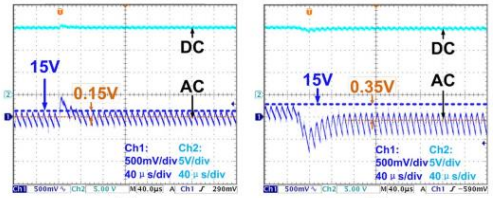

Fig. 18. For CBP-DSCM controller with single compensation, output voltage transients when (a) line voltage steps from 7.5 to 10 V and (b) load steps from 20 Ω to 10 Ω.

results verify the analysis in Section III and prove the effec- tiveness of DCEC.

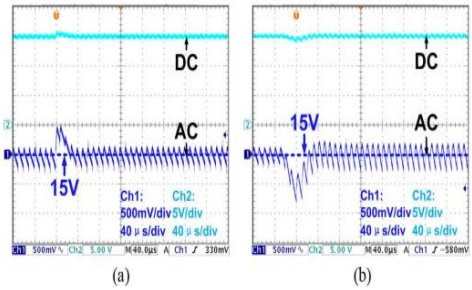

Fig. 19. For CBP-DSCM controller with DCEC, output voltage transients when (a) line voltage steps from 7.5 to 10 V and (b) load steps from 20 Ω to 10 Ω.

CONCLUSION

This paper has examined the watched current error, the reference current error, and the yield voltage relentless state error in the CBP-DSCM-controlled dc– dc converter. To repay the current errors, a DCEC methodology is proposed. It repays the errors in an equivalent amount by a current error eyewitness, which considers parasitics and computes the errors without guess. In spite of the fact that the compensation system requires more equipment assets than advanced PI controllers, it is as yet an alluring alternative. The system expands current guideline air conditioning curacy, while taking out the yield voltage relentless state error. Likewise, precise little sign models for both the converter and the controller are developed. In light of these models, converter steadiness and power are dissected and verified through recreation. At last, trial results approve the viability of the DCEC-remunerated CBP-DSCM controller.

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