International Journal of Research
Available at https://journals.pen2print.org/index.php/ijr/
e-ISSN: 2348-6848
p-ISSN: 2348-795X
Volume 06 Issue 07
June 2019

A method to reduce circulating current and common mode voltage for paralleled converters using three-level space vector modulation.

Chimnabaigari Nazeer Hussain & G.Sudhir Kumar
[1]P.G. Scholar, [2]Asst., Professor,
[1,2] SVR Engineering College
[1,2]Nandyal, Kurnool Dist. A.P

ABSTRACT

For high power applications, paralleling converters is a popular approach to increase the power capacity of the system. Circulating current has been a major concern for the implementation of paralleled converters. This project proposes a three-level space vector modulation (SVM) scheme for a system with two paralleled voltage source converters (VSCs) with common mode inductor (CMI) or single phase inductors.

The proposed scheme aims to reduce the zero-sequence circulating current (ZSCC) and the magnitude of common mode voltage (CMV) of the system simultaneously. The ZSCC pattern with respect to modulation schemes are first analyzed to provide a clear understanding of the generation of ZSCC. Based on the analysis, the proposed three-level modulation scheme is introduced. Furthermore, performance regarding the ZSCC peak value, impact on the common mode current (CMC), CMI scaling analysis, and switching losses are analyzed and compared with the existing methods. The proposed method has been verified in both simulation and experiment.

Keywords:- Space Vector, Modulation, Voltage Source Converters, Common Mode Inductor, Zero Sequence Circulating, Current, Magnitude of Common Mode Voltage.

INTRODUCTION

Three-phase voltage source converters (VSCs) have been very popular in many power conversion applications such as electric motor drives and renewable energy integrations. There is an increasing interest in using VSCs in paralleled manner to meet the increasing requirement of power rating through current sharing among the VSCs [1], [2]. Paralleling converters also provides benefits like improved reliability by enabling implementation of flexible fault-tolerant techniques [3], [4]. Fig.1.1 shows an example configuration of paralleled VSCs.

An important concern for implementing parallel VSCs is the circulating current. Due to parameter and control asymmetries, the terminal voltages of the paralleled phase legs may be different, generating circulating current among the VSCs [5]. If not dealt with properly, such circulating current brings adverse effects like higher current stresses and conduction losses of the switching devices [6]. On the other hand, interleaving the paralleled VSCs has been increasingly attractive due to its capability of providing multilevel output, and therefore line current harmonics reduction, and passive component size reduction [7]- [9].

In the case of interleaving operation, circulating current can be enlarged since the voltage differences of the paralleled phase legs are always created intentionally. Therefore different circulating current suppression methods for paralleled VSCs have been proposed in literature.

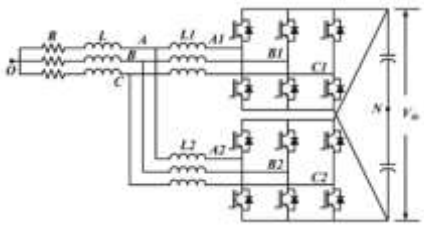


Fig 1.1 Two parallel connected VSCs with common DC link

Basically, the methods can be classified into three categories, passive methods,

control methods and modulation methods. For passive methods, galvanic isolated transformer [10] and separated DC voltage sources [11] have been considered to cut off the zero-sequence circulating path among VSCs. However the size and cost of the system will be increased significantly.

Alternatively, coupled inductor CI) [12], [13]or common mode inductor (CMI) [14] can be used to provide large impedance to suppress circulating current. To be specific, the CI and CMI are actually used to suppress different kinds of circulating currents. The flux of CI is influenced by the differential mode circulating current (DMCC, the difference between the output currents of two VSCs in the same phase). The flux of CMI is generated by the zero-sequence circulating current (ZSCC, the summation of the three-phase output currents of one VSC).

Although the mechanisms are similar, these two kinds of circulating current usually have different pattern and peak values. But one common feature is that the sizes of both CI and CMI are strongly influenced by the pattern of the circulating current. If the peak value of the circulating current can be reduced through active methods, then the size of CI and CMI can be effectively reduced. Currently, systems with CMI are more popular, since for most applications CMI is used not only to suppress circulating current but also to suppress the common mode noises generated by the Pulse width Modulation (PWM) actions [14]. Therefore the suppression of ZSCC has been particularly important.

To further suppress ZSCC, active control methods are also proposed. Ye et al. proposed a method that adjusts the distribution of the null-vectors in conventional SVM scheme by a PI controller [15]. Based on this principle, nonlinear control method and deadbeat control method have been further proposed to enhance the ZSCC control performance [16], [17]. One drawback of this control principle is that it can only be used when conventional SVM strategy is applied.

A similar control idea that can be used for more modulation methods is the common mode injection method [18]-[20]. A closed-loop ZSCC controller is applied to generate a common mode signal which is then injected to the modulation signals of the current controllers, such that the ZSCC can be controlled around the reference value (0 in normal condition). The active control based methods feature the merit of simple implementation but a common limitation is the limited bandwidth, meaning that only low-frequency components of ZSCC can be suppressed through control methods.

However, the fundamental component of ZSCC is at the switching frequency, which can only be regulated by proper PWM strategies. Different PWM strategies have also been investigated in literature. Selective Harmonic Elimination (SHE) PWM scheme was proposed to reduce ZSCC by eliminating the triple harmonics [21]. With the increasing adoption of interleaved operation of parallel VSCs, the interleaved modulation methods have received more attentions recently.

A modified Discontinuous PWM (DPWM) was proposed for the system using three-limb CI [22]. Interleaved Discontinuous SVM (DSVM) or the 60° clamped SVM was applied to the paralleled two VSCs [23], [24]. Due to the possible co- occurrence of different null-vectors, low-frequency component can be generated to push up the peak value of ZSCC in DSVM. To eliminate the low-frequency component, modified DSVM method that introduces additional switching at each sector change point was proposed to make sure that the same null- vector is applied in both VSCs [24]. However the high frequency component of ZSCC cannot be suppressed using this method. Moreover, due to the possible co-occurrence of null- vector and active vectors, high ZSCC di/dt occurs to generate high peak value [25].

To overcome this drawback, a modified DPWM is proposed in [25] which adjusts the position of null- vectors to make sure that the

conditions of application of different null-vectors or one null-vector and one active vector are avoided. Hence both low- frequency and switching frequency ZSCC can be suppressed. The reduction of the peak value of ZSCC can lead to the reduction of the size of CMI, which is always preferred for system cost and size concerns. But this method as additional switching action during each sampling period, two phases in one VSC may be switched simultaneously which makes this method less practical.

Another group of modulation methods treats the paralleled VSCs as a single multilevel converter since coordinated modulation scheme can achieve optimum performance for ZSCC suppression by specially designing the modulation schemes. As the ZSCC is regulated through modulation process, there is no need to implement current sensors for each converters, thus possible cost reduction may be achieved. Also the system can be simply controlled like a single three-phase converter.

This is particularly interesting for system with only two VSCs since the coordinated modulation scheme is not complicated for design. For this condition, the VSCs are modulated using one multilevel modulation scheme. Several schemes have been proposed and discussed for parallel VSCs using CI as circulating current filter [20, 26, 27]. But these methods cannot be directly implemented when CMI is used.

One common drawback of above modulation methods is that the reduction of common mode voltage (CMV) of the converter system is not considered. For applications like grid connected PV inverters and motor drives, there is a requirement on the level of CMV. And in practical applications, the size of CMI is determined by both ZSCC and common mode current (CMC). High CMV peak will also bring high peak value of CMC, which in turn increases the size of CMI[28].For paralleled VSCs, the maximum value of CMV (Vdc/2) happens when the same null-vectors are applied in the VSCs.

Therefore the interleaved modulation methods introduced in [24] and [25] always have the peak CMV of Vdc/2 since they suppress ZSCC by intentionally applying the same null-vector at the VSCs. In [25], although the ZSCC in low modulation index range is suppressed significantly, the dwell time of null-vectors will be long, resulting in large CMCin low modulation index range [29]. As will be analyzed in Section III in this paper, existing methods cannot achieve both CMV and ZSCC reduction. The ZSCC performance of the interleaved SVM is poor [25], although its CMV magnitude is limited to be within Vdc/6. The ZSCC peak value of interleaved DSVM is smaller than that of interleaved SVM but is still larger compared to the method in [25], and its maximum CMV magnitude is Vdc/2. Therefore a method that can reduce both CMV and ZSCC peak values is desired to further reduce the size ofCMI.

This project proposes a three-level SVM method for the system with two paralleled VSCs as shown in Fig. 1. The proposed method can reduce the peak values of both ZSCC and CMV, and at the same time does not negatively influence the quality of the three-level output. In addition, the proposed method is simple for implementation as it is a typical three- level SVM scheme using redundant switching states to limit ZSCC peak values. Compared to [25], the peak value of ZSCC is suppressed to the same level but CMV of the system is reduced from Vdc/2 to Vdc/6, lowering the peak value of CMC. Thus the size of CMI can be further educed. In addition, the overall efficiency of the proposed method is higher than that of the interleaved SVM and DPWM in [25], making it suitable for practical implementation.

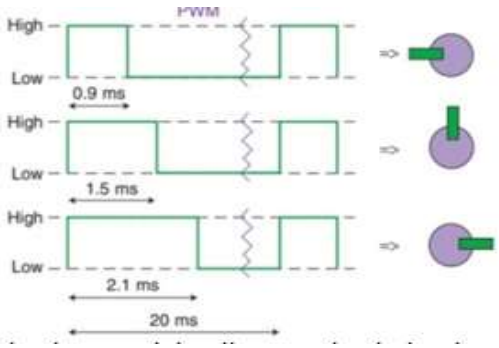
Pulse width modulation(PWM)has been actively used in circuits and systems for many years. Its unique features help it participate in various applications, including motor control, telecommunications, switch-mode power supplies (SMPS), and classD power amplifiers(PA).The PWM is an inevitable part

International Journal of Research
Available at https://journals.pen2print.org/index.php/ijr/
e-ISSN: 2348-6848
p-ISSN: 2348-795X
Volume 06 Issue 07
June 2019

of the SMPSs and the class D PAs among the other major applications. Being a part of these circuits and systems makes the PWM be a part of a huge family of products addressing various markets such as consumer electronics, wearable electronics, automotive, healthcare, industrial, military/defense, and aerospace.

The evolution of a simple PWM chip was first started by Silicon General's cofounder and power electronics engineer, Bob Mammano, in 1975 [1]. Constant advances in the electronics technology have triggered the evolution of the first PWM integrated circuit (IC) so that the transition from a simple chip to a complete power management IC (PMIC) was achieved.

The significant role of the PWM in wide range of circuits and systems has been motivating many researchers and engineers to develop its theoretical and practical background for many years. Today, the PWM can be implemented in various platforms with different methods. The PWM can be implemented by an analog or a digital application specific integrated circuit (ASIC) or general purpose digital ICs such as a field-programmable gate array (FPGA) or a digital signal processor (DSP). Besides, the PWM can be



implemented in discrete circuit level with active and passive electronic components.

2.1BRIEF DESCRIPTION OF PULSE WIDTH MODULATION:

The Pulse Width Modulation (PWM) is a technique in which a reference signal is coded into a pulse train whose widths correspond to the interpretation of the signal itself [6], [10]. The PWM requires two signals; the original signal, also called the "modulating signal", which will be coded into a pulse train, and the "carrier signal", which can be either a triangle wave or a saw-tooth wave. The resulted pulse train is called "modulated signal" which isthe PWM signal itself. The PWM signal is generated by comparing the modulating signal with the high frequency carrier signal as depicted in
Figure 2.1.

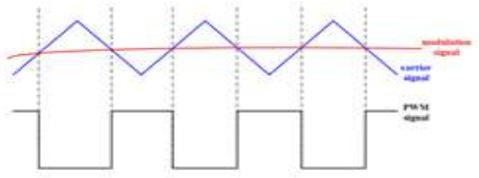


Fig 2.1 pulse width modulation

As can be seen in Figure 2.1, the PWM signal is made of rectangular pulses, which switch between high and low levels. Figure 2 shows a close-up view of a sample PWM signal with a defining function y(t), period T, low level value ymin, high level value ymax, and a duty cycleD.

The average value of the PWM signal shown in Figure 2 can be expressed as
This relation reveals the direct dependence between the average value of the PWM signal and its duty cycle. The ability of controlling the average value of the PWM signal with its duty cycle creates many application areas for the PWM. The following sub-section summarizes some of the major application areas of the PWM.

2.2 MAJOR APPLICATIONS OF PULSE WIDTH MODULATION:

The pulse width modulation has been playinga critical role in many circuits and systems for a long time. Its unique structure makes the PWM participate in various applications. The major applications of the PWM can be listed as follows:

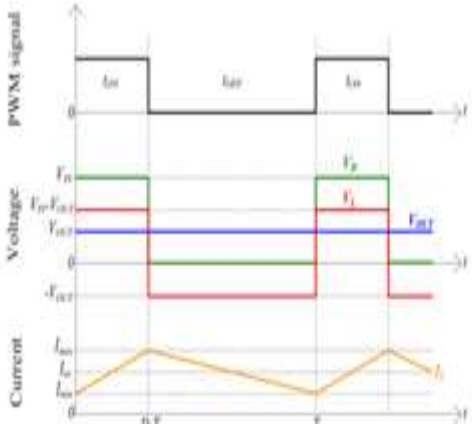
2.2.1MOTORCONTROL:

International Journal of Research
Available at https://journals.pen2print.org/index.php/ijr/
e-ISSN: 2348-6848
p-ISSN: 2348-795X
Volume 06 Issue 07
June 2019

Motor control is one of the major applications of the PWM for many years [11], [12], [5]. Controlling the speed of an electric motor is achieved by controlling the power delivered to it, which is directly proportional to the voltage applied. This control mechanism is perfectly matched with the idea of the PWM in such a way that the duty cycle of the PWM signal should be decreased to slow down the motor or increased to speed it up. By changing the duty cycle of the PWM signal, its average value is adjusted to control the power delivered to a motor as it is expressed in (1). In PWM-controlled servomotors on the other hand, the servo position is determined by the width of the pulse instead of the duty cycle of the pulse. Controlling a servomotor with respect to the widths of the PWM signal is shown in Figure3withanexample,wheretheservomotoruse d is HS-322HD of Hitec RCD, USA [13]. As can be seen in Figure 2.3, the specific values of the pulse widths of the PWM signal correspond to the specific rotation angles.

2.2.2 SWITCH-MODE POWER SUPPLIES:

All electronic circuits and systems need power supplies to function. Power supplies can be categorized into two linear power supplies and switch-mode power supplies (SMPS). Linear power supplies contain transistors working in the active



operation region, causing high voltage drops at high currents. Thus, these types of supplies have large power dissipation resulting in low efficiency [10],[14].

SMPSs use transistors as switches in such a way that they allow current passing through them when they are “ON” and they do not conduct any current when they are “OFF”. For both cases, the power dissipation over the transistors are ideally zero. Therefore, the switch-type operation of the transistors dramatically reduces the power dissipation of the system resulting in a large improvement in the efficiency. High efficiency, small size and light-weight are the dominant characteristics of SMPSs over linear power supplies helping SMPSs employed in a variety of electronic systems such as personal computers, laptops, and televisions[15].

The PWM is an essential part of most of the SMPS circuits. Kazimierczukin [10] defines a family of PWM-based circuits consisting of the buck, boost, buck-boost, fly- back, forward, SEPIC (single-ended primary input converter), and dual SEPIC, which are all single-ended types. Moreover, there are three multiple-switch PWM-based SMPS circuits such as the half-bridge, full-bridge, and push-pull converters. All of these circuits utilize the PWM in their control loop to adjust the output voltage.

The detailed analysis of all PWM-based SMPS circuits are beyond the scope of this work, however for the sake of completeness, the PWM operation will briefly be covered for the buck and boost converter circuits. The circuit topology for the buck converter is shown in Figure 4. Fig 2.3 controlling hs-322hd servomotor with pwm2

The circuit operates under the control of the pulse width modulation as follows: when the PWM signal is high, the transistor M will be “ON” making the diode D reverse- biased. Thus, there will be a current flowing through the inductor L charging the capacitor C. When the PWM signal is low, the transistor will be “OFF” and the diode will be forward- biased. Also, the input voltage will be separated from the output since the transistor is “OFF”. Within this time interval, the inductor will behave like a voltage source.

In other words, the input voltage will supply the current when the PWM signal is high and

International Journal of Research
Available at https://journals.pen2print.org/index.php/ijr/
e-ISSN: 2348-6848
p-ISSN: 2348-795X
Volume 06 Issue 07
June 2019

the inductor will supply the current when the PWM signal is low. If the value of the current never falls to zero, the operation is called continuous mode and the voltage/current waveforms for this operation is shown in Figure5.

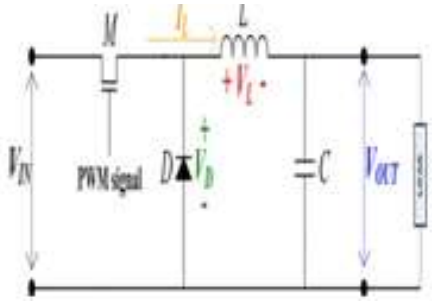


Fig 2.4 The circuit topology of the BUCK CONVERTER

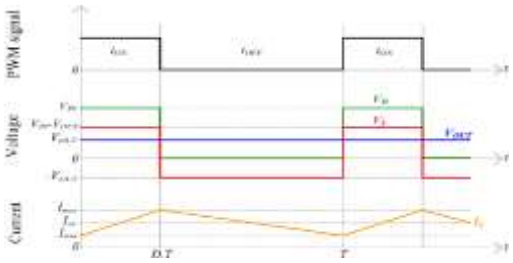


Fig 2.5 voltage /current waveforms for the continuous mode buck converter

The relation between the input and the output voltages for the buck converter can be expressed Since the duty cycle of the PWM signal is not more than 1, the output voltage will always be less than the input voltage causing the buck converter is also called as the step-down converter. As it can be seen from (2), the PWM signal directly controls the operation of the buck converter by adjusting its duty cycle.

Another PWM-based DC-DC converter type is the boost converter and its circuit topology is shown in Figure 6. The circuit has the same components with the buck converter however, its design and working principle are different than the buck converter.

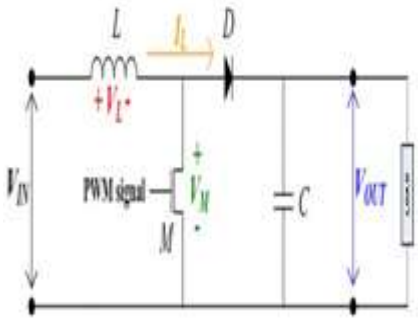


Fig 2.6the circuit topology of the boost converter

When the PWM signal is high, the transistor M will be "ON", the diode D will be reverse biased, and the current will flow through the inductor L returning back to the input power supply. Meanwhile, the current will be increased resulting in stored energy on the inductor.

This stored energy will create a magnetic field in which the positive polarity is at the left side of the inductor. Within this time interval, the current, which will be supplied to the load, is obtained by the discharge of the capacitor C. When the PWM signal is low, the transistor will be "OFF" forcing the current drawn from the input supply flow through the inductor and the diode. Within this time interval, the current will be reduced and the magnetic field will be reversed.

Thus, the induced voltage on the inductor will act as a voltage source in series with the input voltage charging the capacitor to the output voltage. In other words, when the PWM signal is high, the capacitor will be the source of the current for the load while the current will be drawn from the input voltage supply and it will flow through the inductor and the diode. Similar to the buck converter, the operation is called continuous mode if the value of the current never falls to zero and the voltage/current waveforms for this operation is shown in Figure7.

The direct dependence of the output voltage on the duty cycle of the PWM signal is expressed as

International Journal of Research
Available at https://journals.pen2print.org/index.php/ijr/
e-ISSN: 2348-6848
p-ISSN: 2348-795X
Volume 06 Issue 07
June 2019

Fig 2.7 voltage /current waveforms for the continuous mode boost converter

The output voltage generated in the boost converter is always greater than the input voltage as can be seen in (3).

CLASS D POWERAMPLIFIER:

Class D power amplifiers (PA) have been employed by many electronic devices in which an audio signal amplification is required. There are different types of power amplifiers such as class A, B, and AB classified with respect to the transistor's quiescent point. The theoretical efficiency values for class A, B, and AB are 25%, 78.5%, and slightly more than 78.5%, respectively [16]. However, battery- powered devices such as cell-phones, portable audio devices, and laptops necessitate low- power circuits in their electronics.

For such applications, to achieve higher power efficiency numbers switching mode power amplifiers (i.e. class D) with their theoretical efficiencies of 100% are usually employed. Although this value will be limited due to the switching and the conduction losses in the switching power transistors, class D PAs are still much more efficient than the other classes. The circuit topology for a half- bridge class D power amplifier is shown in Figure8.

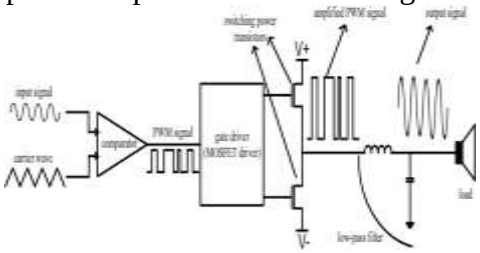


Fig 2.8 the circuit topology of a half-bridge class D power amplifier

The input signal to be amplified is compared with a high frequency carrier wave so that the PWM signal is generated. The PWM signal is fed to a gate driver, which can be an integrated circuit or a discrete circuit design. The gate driver boosts the current rating of the PWM signal and adjusts its voltage level to be able drive the switching power transistors. After the switching is done, the PWM signal is obtained in such a way that its rails are between the positive and the negative supply voltages. To re- obtain the amplified input signal without harmonics, the amplified PWM signal is filtered with a low-pass filter.

With filtering, high frequency components generated due to the carrier wave are removed and we end up with the amplified input signal, which drives the load. The higher efficiency of the class D power arises from the switching architecture of the circuit, for which the PWM operation is perfectlysuited.As mentioned earlier, class D power amplifiers are generally used in cell- phones, laptops and portable audio devices to generate high power audio signal, which drives a speaker.Another usage of classD power amplifies is in SONAR(sound Navigation and Ranging) systems. SONAR systems use acoustic waves to detect and classify a target underwater. They are also used for communication and navigation underwater. There are two types of SONAR systems; passive and active [17].

A passive SONAR works based on evaluating the echo coming from the under watertargets. On the other hand, an active SONAR emits acoustic waves using its transmitter and it processes the reflected acoustic signals from the targets. A transmitter of an active SONAR consists of power amplifiers and acoustic transducers. An acoustic transducer is a sensor, which converts an electrical signal into an acoustic signal and it is driven by power amplifiers to generate high acoustic powers [18].

To be able to detect a target from a longer range, the power transmitted by the power amplifiers should be as high as possible [17]. It is required to satisfy high power values with high efficiency, which makes class D power amplifiers be a good solution for SONAR transmitters. Until this point, the major applications of the pulse width modulation have been covered. The next part includes the types and the general characteristics of the PWM signal.

International Journal of Research
Available at https://journals.pen2print.org/index.php/ijr/
e-ISSN: 2348-6848
p-ISSN: 2348-795X
Volume 06 Issue 07
June 2019

SPACE VECTOR PULSE WIDTH MODULATION METHOD (SVPWM)

INTRODUCTION:

Space vector pulse width modulation method is best among all the PWM techniques for drive applications and the three phase voltage source inverters (VSI). Compared to sinusoidal pulse width modulation Method (SPWM), SVPWM has many advantages, which are less switching losses, less total harmonic distortion, it is easy to digitalize and better utilization of dc-bus voltage. The performance of the SVPWM inverter is based on the following criteria: switching losses of the inverter, total harmonic distortion (THD) andmaximum output voltage.

Originally the SVPWM method is developed as a vector approach to pulse width modulation (PWM) for three phase inverters. In SVPWM inverter the reference wave is revolving reference voltage vector andthe carrier signal is high frequency triangular or saw tooth waveform. The intersection of these two will give the gate pulses to inverter to control the voltage and frequency of the inverter.

FEATURES OF SVPWM

The SVPWM is better than the other PWM methods due to the following features. It has the wide linear modulation range including with PWM third harmonic injection automatically. It has lesser switching losses because only one switch is operating at a time in the SVPWM inverter. It gives 15.5% more utilization of DC-Link voltage than the conventional PWM methods. phase voltage is V_{dc} , output line voltage is $3V_{dc}$,therefore SVPWM gives more output phase and line voltages than the SPWM inverter.

It is a digital modulating technique.

CONCEPT OF VECTOR:

The space vector concept is derived from rotating magnetic field theory of three phase induction motor which is used for modulating the inverter output voltage. In this method three phase voltages are transformed to two phase voltages either in stationary reference frame or synchronous rotating reference frame. Using this two phase voltage reference components the inverter output can bemodulated. Let us take the three phase balanced voltages as shown below,

$$V_{as} = V_m \sin\left(\omega t + \frac{2\pi}{3}\right)$$

If we apply these three phase balanced voltages to the three phase induction motor, it produces rotating flux vector in the air gap of the induction machine rotating with a velocity of □. This rotating flux vector magnitude and angle can be calculated using the Clark's transformation method in stationary reference frame as shown below

$$\vec{V}_{ref} = \vec{V}_\alpha + j\vec{V}_\beta = \frac{2}{3}\left(V_a + V_b e^{j\frac{2\pi}{3}} + V_c e^{j\frac{4\pi}{3}}\right)$$

$$V_\alpha = \frac{2}{3}\left(V_a \cos 0 + V_b \cos\frac{2\pi}{3} + V_c \cos\frac{4\pi}{3}\right)$$

$$V_\beta = \frac{2}{3}\left(V_a \sin 0 + V_b \sin\frac{2\pi}{3} + V_c \sin\frac{4\pi}{3}\right)$$

The above equations can be represented in matrix form as shownbelow

$$\begin{bmatrix} V_\alpha \\ V_\beta \end{bmatrix} = \begin{bmatrix} 1 & \frac{-1}{2} & \frac{-1}{2} \\ 0 & \frac{\sqrt{3}}{2} & \frac{-\sqrt{3}}{2} \end{bmatrix} \begin{bmatrix} V_{as} \\ V_{bs} \\ V_{cs} \end{bmatrix}$$

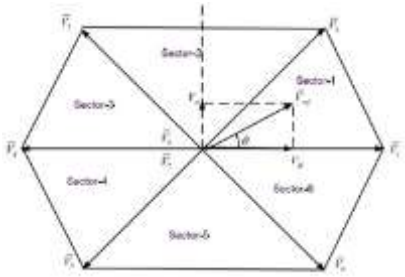


Fig 4.1. representation of rotating vector in complex plane

PRINCIPLE OF SPACE VECTOR PWM:

International Journal of Research
Available at https://journals.pen2print.org/index.php/ijr/
e-ISSN: 2348-6848
p-ISSN: 2348-795X
Volume 06 Issue 07
June 2019

The three phase voltage source inverter (VSI) with BLDC motor load is shown in figure 2. It has three legs that have two switching devices and those are complimenting each other. i.e. only one switch is operating at a time. Therefore the output voltage of the inverter is determined by the ON/OFF of the three switching devices (S1, S3, and S5).

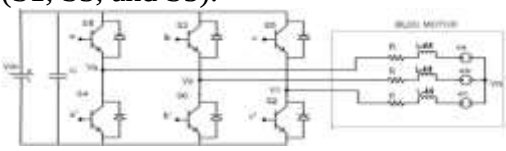


Fig 4.2 three phase vsi with bldc motor

The output voltage is controlled by the switching variables a, b, c, a', b' and c'. If the upper switch is ON then the switching variable a, b, or c is 1, then the corresponding switching device is OFF, then the switching variable a', b', or c' is 0. The following matrix gives the relation between switching variable and the output phase voltages and output line voltages.

$$\begin{bmatrix} V_{an} \\ V_{bn} \\ V_{cn} \end{bmatrix} = V_{dc} \begin{bmatrix} 1 & -1 & 0 \\ 0 & 1 & -1 \\ -1 & 0 & 1 \end{bmatrix} \begin{bmatrix} a \\ b \\ c \end{bmatrix}$$

$$\begin{bmatrix} V_{ab} \\ V_{bc} \\ V_{ca} \end{bmatrix} = \frac{V_{dc}}{3} \begin{bmatrix} 2 & -1 & -1 \\ -1 & 2 & -1 \\ -1 & -1 & 2 \end{bmatrix} \begin{bmatrix} a \\ b \\ c \end{bmatrix}$$

Inverter has eight possible switching states out of which six switching states gives six active voltage vectors and two switching states gives two null vectors. Based on the equations (2.4), (2.9) and (2.10) inverter output phase voltages, output line voltages and voltage vectors are determined which are in the tabular form-1

Table 4.1 Inverter output voltages switching states and corresponding voltage vectors

Voltage vectors ($\times V_{dc}$)	Switching vectors			Output phase voltages ($\times V_{dc}$)			Output line voltages ($\times V_{dc}$)		
	a	b	C	Van	Vbn	Vcn	Vab	Vbc	Vca
$\bar{V}_0 = 0$	0	0	0	0	0	0	0	0	0
$\bar{V}_1 = \frac{2}{3}e^{j0}$	0	0	1	$\frac{2}{3}$	$\frac{-1}{3}$	$\frac{-1}{3}$	1	0	-1
$\bar{V}_2 = \frac{2}{3}e^{j\frac{\pi}{3}}$	0	1	0	$\frac{1}{3}$	$\frac{1}{3}$	$\frac{-2}{3}$	0	1	-1
$\bar{V}_3 = \frac{2}{3}e^{j\frac{2\pi}{3}}$	0	1	1	$\frac{-1}{3}$	$\frac{2}{3}$	$\frac{-1}{3}$	-1	1	0
$\bar{V}_4 = \frac{2}{3}e^{j\frac{3\pi}{3}}$	1	0	0	$\frac{-2}{3}$	$\frac{1}{3}$	$\frac{1}{3}$	-1	0	1

5 IMPLEMENTATION OF SPACE VECTORPWM:

SVPWM can be implemented in three steps which are

Calculation of,*Vd Vq* and □.

Calculation of *T*1 ,*T*2 and *T*0 .

Calculation of switching time of each switching device (S1TO S6).

4.5.1 CALCULATION OF V_d ,V_q AND :

Using Clark's transformation three phase voltages are transformed to two phase voltages in stationary reference frame that is shown in figure.

$$= V_a - \frac{1}{2}V_b - \frac{1}{2}V_c$$

$$= \frac{\sqrt{3}}{2}V_b - \frac{\sqrt{3}}{2}V_c$$

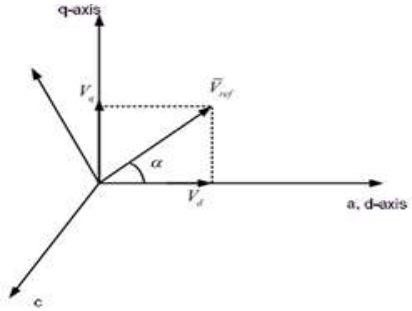


Fig 4.3 reference vector in the two and three dimensional plane

$$\begin{bmatrix} V_d \\ V_q \end{bmatrix} = \begin{bmatrix} 1 & \frac{-1}{2} & \frac{-1}{2} \\ 0 & \frac{\sqrt{3}}{2} & \frac{-\sqrt{3}}{2} \end{bmatrix} \begin{bmatrix} V_{an} \\ V_{bn} \\ V_{cn} \end{bmatrix}$$

$$\text{Where } |V_{ref}| = \sqrt{(V_d^2 + V_q^2)} \text{ and } \alpha = \tan^{-1}\frac{V_q}{V_d}$$

Calculation of T1 , T2 andT0

Calculation of T1 , T2 andT0 insector-1:

For generating a voltage vector Vref in sector-1 at a sampling Tztime of , it requires two active voltage vectors and two null vectors.Let V 1 is the active voltage vector

International Journal of Research
Available at https://journals.pen2print.org/index.php/ijr/
e-ISSN: 2348-6848
p-ISSN: 2348-795X
Volume 06 Issue 07
June 2019

applied at fraction of time T1/Tzinterval, and V 2 is the active voltage vector applied at time T2/Tz and two null vectors which are applied at a time intervals .respectively.

Below figure represents the generation of Vref vector in sector-1.

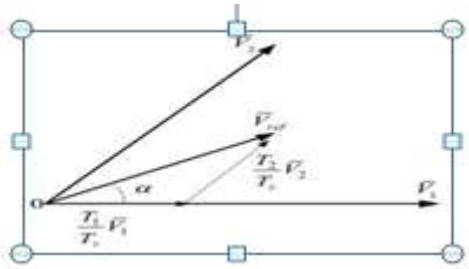


Fig 4.4 calculation v_{ref} insector-1

$$T_1 = \frac{\sqrt{3}T_z |V_{ref}| \sin\left(\frac{n\pi}{3} - \alpha\right)}{V_{dc}}$$

$$T_0 = T_z - T_1 - T_2$$

CALCULATION OF SWITCHING TIME OF EACH SWITCHING DEVICE (S1 TO S6):

The following table shows the switching sequence corresponds to each sector. For each cycle there are 7 switching states in each sector. The odd sector numbers travels in anti-clockwise direction and even sector numbers travels in clockwise direction. The following table represents the switching sequence each sector

Table 4.2 Switching sequence of the modulation

Sector no:	Switching sequence
1	
2	
3	
4	
5	
6	

In sector-1 the switching states sequence is *V*0-*V*1-*V*2-*V*7-*V*2-*V*1*V*0 . Here sampling time period is equal to the switching time period *Ts* , which is divided among the 7 switching states, out of which three are zero vectors.

$$T_z = \frac{T_0}{4} + \frac{T_1}{2} + \frac{T_2}{2} + \frac{T_0}{4} + \frac{T_2}{2} + \frac{T_1}{2} + \frac{T_0}{4}$$

The following figure 4 shows the switching pulse pattern in all the sectors. The following symmetrical pulse patterns gives the less harmonics. Based on the symmetric pulses waveforms switching times of all theswitching devicesin all thesectors are derived.

Sector no	Rotor position in each sector	Upper switching Devices(S1, S3, S5)	Lower switching Devices(S4, S6, S2)
1	$0^\circ \le \theta \le 60^\circ$	$S_1 = T_1 + T_2 + \frac{T_0}{2}$; $S_3 = T_2 + \frac{T_0}{2}$; $S_5 = \frac{T_0}{2}$;	$S_4 = \frac{T_0}{2}$; $S_6 = T_2 + \frac{T_0}{2}$; $S_2 = T_1 + T_2 + \frac{T_0}{2}$;
2	$60^\circ \le \theta \le 120^\circ$	$S_1 = T_1 + \frac{T_0}{2}$; $S_3 = T_2 + T_1 + \frac{T_0}{2}$; $S_5 = \frac{T_0}{2}$;	$S_4 = T_1 + \frac{T_0}{2}$; $S_6 = \frac{T_0}{2}$; $S_2 = T_1 + T_2 + \frac{T_0}{2}$;
3	$120^\circ \le \theta \le 180^\circ$	$S_1 = \frac{T_0}{2}$; $S_3 = T_1 + T_2 + \frac{T_0}{2}$; $S_5 = T_1 + \frac{T_0}{2}$;	$S_4 = T_1 + T_2 + \frac{T_0}{2}$; $S_6 = \frac{T_0}{2}$; $S_2 = T_2 + \frac{T_0}{2}$;
4	$180^\circ \le \theta \le 240^\circ$	$S_1 = \frac{T_0}{2}$; $S_3 = T_2 + \frac{T_0}{2}$; $S_5 = T_1 + T_2 + \frac{T_0}{2}$;	$S_4 = T_1 + T_2 + \frac{T_0}{2}$; $S_6 = T_2 + \frac{T_0}{2}$; $S_2 = \frac{T_0}{2}$;
5	$240^\circ \le \theta \le 300^\circ$	$S_1 = T_2 + \frac{T_0}{2}$; $S_3 = \frac{T_0}{2}$; $S_5 = T_1 + T_2 + \frac{T_0}{2}$;	$S_4 = T_2 + \frac{T_0}{2}$; $S_6 = T_1 + T_2 + \frac{T_0}{2}$; $S_2 = \frac{T_0}{2}$;

Table 4.3 Switching times in each sector

ZSCC AND CMV OF PARALLELED VSCS

5.1ZSCC AND CMVPATTERNS:

Considering a system with two paralleled two-level VSCs, each VSC has eight switching states. The states are presented as: V0 [0 0 0], V1 [1 0 0], V2 [1 1 0], V3 [0 1 0], V4 [0 1 1], V5 [0 0 1], V6 [1 0 1], V7 [1 1 1]. The space vector diagram is shown in Fig. 5.1 When different switching states are applied to the two converters, ZSCC and CMV can have different patterns.

ZSCCPATTERN:

Seen from Fig. 5.1, when the terminal voltages of a paralleled phase leg are different, circulating current will be generated in this phase leg. For instance, when the voltages of

International Journal of Research
Available at https://journals.pen2print.org/index.php/ijr/
e-ISSN: 2348-6848
p-ISSN: 2348-795X
Volume 06 Issue 07
June 2019

A1 and A2 are different, there will be a voltage applied across the inductance of L1+L2, then current will flow through the

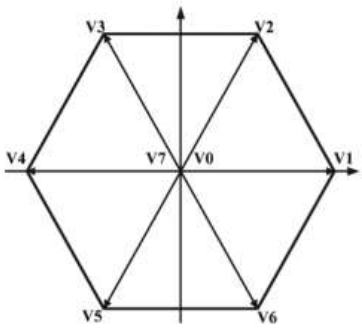


Fig 5.1 space vector diagram of two-level VSC

Inductance and circulating within phase A, as common DC link is used. The circulating current in a single phase leg can be expressed as

$$\frac{di_{X,0}}{dt} = \frac{v_{X1N} - v_{X2N}}{L_1 + L_2} \qquad (1)$$

where X is A, B, or C; N is the neutral point of the DC link; iX,0 stands for the circulating current of phase X; L1 and L2 are the filter inductance of the two converters. For each converter, the ZSCC can be given by

$$I_{01} = I_{A1} + I_{B1} + I_{C1} = -I_{02} \qquad (2)$$

PROPOSED SVM SCHEME

From both Table II and Table III, one can see that the null vectors are the major reason for both large ZSCC variation and high CMV peak. If null vectors are not used in modulation, the ZSCC variation speed and CMV peak are naturally reduced. This principle is similar to the 'Reduced CMV SVM' method for single two-level VSCs [31], [32]. But the difference is, for single VSC, the null vector is replaced by active vectors, thus zero voltage vectors are completely eliminated from the output voltages. The output quality will be negatively influenced. While for the paralleled VSCs, although null vectors for single VSC are not used, zero voltage vectors for the three-level output can still be realized. This ensures that the output current quality will not be negatively influenced. The voltage vectors for three-level output are listed in Table IV.Itis shown that there are redundancies for voltage vectors from V7 to V18, thus the switching sequence design can be very flexible to regulate the waveforms of ZSCC andCMV.

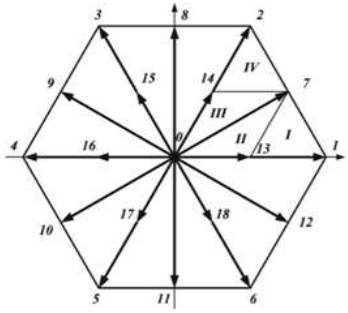
		VSC2					
		V1	V2	V3	V4	V5	V6
VSC1	V1	1	7	14	0	18	12
	V2	7	2	8	15	0	13
	V3	14	8	3	9	16	0
	V4	0	15	9	4	10	17
	V5	18	0	16	10	5	11
	V6	12	13	0	17	11	6

Table 6.1 Complete voltage vectors for three level output

DESIGNED SWITCHING SCHEME:

In the proposed three-level SVM scheme, each sector is divided into four subsectors. The locations of the voltage space vectors and the division of subsectorsare shown in Fig. 6. The voltage vectors can be classified by magnitude, i.e., zero vector (V0), large vectors VL (V1-V6), medium vectors VM (V7-V12), and mall vectors VS (V13-V18). Taking sector 1 as an example, the designed switching sequences within subsector I and II, as well as the switching action of each phase are listed in Table V to Table VI respectively.

With subsector division shown in Fig. 6, the switching sequence pattern in each 30 degreeis the same. For example, in subsector I and IV of all sectors, the switching sequence is [VS VM VL VM VS VM VL VM VS]. In subsector II and III of all sectors, the switching sequence is [V0 VS VM VM VS V0 VS VM VM VS V0]. In practical implementation, the selection of redundant states can simply



International Journal of Research
Available at https://journals.pen2print.org/index.php/ijr/
e-ISSN: 2348-6848
p-ISSN: 2348-795X
Volume 06 Issue 07
June 2019

FIG 6.1The division of sectors and locations of vectors

Table 6.2 switching sequence in subsector I of sector 1

	Vector								
	V_{13}	V_7	V_1	V_7	V_{13}	V_7	V_1	V_7	V_{13}
VSC1	2	2	1	1	6	1	1	2	2
VSC2	6	1	1	2	2	2	1	1	6
A1	1	1	1	1	1	1	1	1	1
B1	1	1	0	0	0	0	0	1	1
C1	0	0	0	0	1	0	0	0	0
A2	1	1	1	1	1	1	1	1	1
B2	0	0	0	1	1	1	0	0	0
C2	1	0	0	0	0	0	0	0	1

Table 6.3 Switching sequence in subsector II of sector 1

	Vector										
	V_0	V_{13}	V_7	V_7	V_{13}	V_0	V_{13}	V_7	V_7	V_{13}	V_0
VSC1	3	2	2	1	6	6	6	1	2	2	3
VSC2	6	6	1	2	2	3	2	2	1	6	6
A1	0	1	1	1	1	1	1	1	1	1	0
B1	1	1	1	0	0	0	0	0	1	1	1
C1	0	0	0	0	1	1	1	0	0	0	0
A2	1	1	1	1	1	0	1	1	1	1	1
B2	0	0	0	1	1	1	1	1	0	0	0
C2	1	1	0	0	0	0	0	0	0	1	1

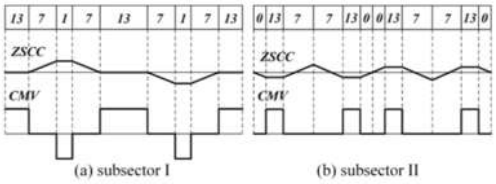


Fig 6.2 zscc and cmv pattern in sub-sector i and ii of sector

The ZSCC and CMV variation patterns can be illustrated in Fig. 7, taking sub-sectors I and II as examples. Sub-sectors III and IV have the same pattern. Seen from Fig. 7, the peak value of ZSCC is limited by quarterly dividing the dwell time of voltage vectors and reversing the direction of ZSCC by redundant switching vectors. As a result, the average ZSCC value is controlled to 0 in each sampling cycle, which means low frequency ZSCC iseliminated.

Moreover, as can be seen from Table V and Table VI, for each VSC, there is only one switching action at a time within each sampling period (for example, in Table V when the three-level vector is switched from V7 (2, 1) to V1 (1, 1), for VSC1 only the voltage of phase B1 is switched from 1 to 0 while phase A1 and C1 are un switched), meaning that the problem of instantaneous line-to-line voltage reversal is avoided. This feature makes the proposed scheme practical for real application [33]. Meanwhile no additional switching action is introduced in each sampling period. The switching frequency is limited within the sampling frequency, as will be discussed later in thispaper.

The dwell time calculation of the voltage vectors is given in Table VII, where T0, Ta, Tb, and Tc respectively represent the dwell time of zero vector, small vectors, medium vectors, and large vectors; Ts represents the sample period; θ stands for the reference voltage vector angle within the sector; and M stands for the modulation index (range from 0 to 1) which is defined in (10)[34].

$$M = \frac{\sqrt{3}\left|V_{ref}\right|}{V_{dc}}$$

RELATIONSHIP OF ZSCC PEAK VALUE AND MODULATION INDEX:

The relationship between ZSCC peak value and M can be theoretically calculated. For a certain M, the ZSCC reaches its peak value when θ is 30°. At this point, only medium vectors and zero vector are applied (when M≠1), hence the peak value of ZSCC is determined by the dwell time of these two vectors. The ZSCC patterns with respect to different modulation index range are shown in Fig. 8, where sector 1 is taken as an example. It can be seen that when M = 1, only medium vector V7 is applied. Thus the ZSCC peak is determined by quarter of the dwell time of V7. When M is between 0.5 and 1, the dwell time of V0 is smaller than that of V7. As the switching sequence is designed such that the ZSCC direction reverses when V0 and V7 are alternated, the peak value of ZSCC will be lower compared to the condition of M = 1. When M = 0.5, the application durations of V0 and V7 are equal. When M is between 0 and 0.5, the peak value of ZSCC is solely

International Journal of Research
Available at https://journals.pen2print.org/index.php/ijr/
e-ISSN: 2348-6848
p-ISSN: 2348-795X
Volume 06 Issue 07
June 2019

determined by the quarter of the dwell time of V0, as shown in Fig.8.

The above analysis can be mathematically expressed by the dwell time calculation equations listed in Table VII. The lowest ZSCC peak value occurs when the dwell time of V7 equals to two times of the dwell time of V0, when M = 2/3. After that, the ZSCC peak value is only determined by the dwell time of V0, since (Tb-T0) becomes smaller than T0. Considering that the sampling frequency, DC link voltage and ZSCC filter inductance are constant, the ZSCC peak value is solely determined by the application durations of V0 and V7, thus the ZSCC peak value, normalized with respect to Vdc·Ts/Lcm, under different modulation index range can be given by

$$I_{0,peak} = \left|\frac{1}{4}T_b - \frac{1}{4}T_0\right| = \left|\frac{1}{2}M - \frac{1}{4}\right| \qquad \frac{2}{3} < M \le 1$$

Table 6.4 The dwell time calculation in each subsector of the proposed scheme

	T_1	T_2	T_3	T_4
I		$T_s\left[2-2M\cdot\sin(\frac{\pi}{3}+\theta)\right]$	$2M\cdot\sin\theta T_s$	$T_s\left[2M\cdot\sin(\frac{\pi}{3}-\theta)-1\right]$
II	$T_s\left[1-2M\cdot\sin(\frac{\pi}{3}-\theta)\right]$	$2\sqrt{3}M\cdot\sin(\frac{\pi}{6}-\theta)T_s$	$2M\cdot\sin\theta T_s$	
III	$T_s[1-2M\cdot\sin\theta]$	$2\sqrt{3}M\cdot\sin(\theta+\frac{\pi}{6})T_s$	$2M\cdot\sin(\frac{\pi}{3}-\theta)T_s$	
IV		$T_s\left[2-2M\cdot\sin(\frac{\pi}{3}+\theta)\right]$	$2M\cdot\sin(\frac{\pi}{3}-\theta)T_s$	$T_s[2M\cdot\sin(\theta)-1]$

$$I_{0,peak} = \left|\frac{1}{4}T_0\right| = \frac{1}{4}|1-M| \qquad 0 \le M \le \frac{2}{3}$$

For the method proposed in [25], the normalized ZSCC peak value can be expressed by

$$I_{0,peak} = \frac{1}{4}M \qquad 0 \le M \le 1.$$

Fig 6.3 the zscc pattern under different modulation index range when reference voltage angle is 30 degrees

(11) to (13) are illustrated in Fig. 9 which shows that the calculated ZSCC pattern of the method in [25] is the same as analyzed in [25]. Both methods have the same maximum ZSCC peak value, which means the two methods have the same impact on the size of CMI. And within the modulation index range of (0.5, 1), the ZSCC peak value of the proposed method is smaller than that of the method in [25]. This can effectively reduce the semiconductor losses and current stress of the converters when operating in this M range. But when the modulation index is between 0 and 0.5, the ZSCC peak of the proposed method will increase. However, it should be noted that under normal operation condition, the modulation index of grid connected converter is usually at highervalue.

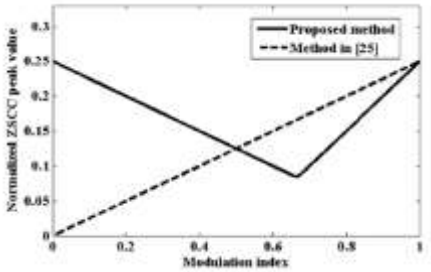


Fig 6.4 the zscc peak value with respect to modulation index

COMMON MODE CURRENT:

In addition to ZSCC, the size of CMI is also influenced by the value of CMC for paralleled VSCs. To further reduce the size of CMI, maximum value of CMC should be reduced in addition to the reduction of ZSCC. Reduction of CMV leads to smaller CMC [33]. In addition, modulation index is also an influential factor for CMC. For both conventional SVM and DSVM modulated inverters, the value of CMC usually becomes higher when M is small [29].

This is because when M is small, the dwell time of zero vector is long. In this case, the magnitude of CMV is Vdc/2, resulting in high CMC peaks. This problem also happens in paralleled VSCs if same null- vectors are applied simultaneously to suppress ZSCC, meaning a lower M causes larger CMC. However, in the proposed scheme, the CMV magnitude islimited to Vdc/6.

The CMC in the entire modulation index range will be reduce due to the reduction of

International Journal of Research
Available at https://journals.pen2print.org/index.php/ijr/
e-ISSN: 2348-6848
p-ISSN: 2348-795X
Volume 06 Issue 07
June 2019

CMV magnitude. At the same time, the zero vector V0 does not generate CMV, only small vectors contribute to the generation of CMV. Therefore, in the proposed method, lower M leads to smaller dwell time of small vectors, which gives lower value of CMC.

The method in [25] introduces additional control of the position of null vectors to ensure the simultaneous application of the same null vector. Therefore in the entire range of modulation index, the magnitude of CMV is high at Vdc/2, which will lead to higher CMC than the proposed method. Moreover, the value of CMC of the method in [25] increases as M decreases because of the long dwell time of null vectors in low M range. Thus the peak value of CMC in [25] will be higher than that of the proposed method. So considering both ZSCC and CMC, by reducing the peak value ofboth ZSCC and CMC, the proposed method will lead to a smaller CMI than the method in [25]. To demonstrate that the reduction of ZSCC and CMC will lead to the reduction of CMI size, analysis of CMI scaling is presented in the following part.

CMI SIZE ANALYSIS:

As has been indicated in [25], reduction of maximum value of ZSCC will result in smaller CMI size. In addition to ZSCC, CMC should also be considered for CMI sizing. In this paper, the summation of ZSCC and CMC is defined as zero sequence current (ZSC), which is the total current generating flux linkage in CMI. To provide a clear relationship between the maximum ZSC and the CMI size, CMI scaling analysis is presented based on the CMI equations in [35]. Assuming three-phase toroidal core CMI is applied, the common mode inductance of such CMI can be given by(14).

$$L_{CM} = \frac{N_c^2 \cdot \mu \cdot A_c}{\pi \cdot d_c}$$

Where Nc is the number of turns wound around the core,dc is the diameter of the core, Ac is the cross-sectional area of the core, μ is the permeability of the core material, Bsis the corresponding saturation flux density, and LCM is the common mode inductance of the CMI. The core size of the CMI SCMI can be simply determined by Ac and dc,as

$$S_{CMI} = \pi \cdot d_c \cdot A_c$$

To avoid core saturation, the maximum ratio of ZSC maximum value IZS and core diameter dc is defined according tothe Ampere's Law [35],

$$\left(\frac{I_{zsc}}{d_c}\right)_{max} < \frac{\pi}{N_c} \cdot \frac{B_s}{\mu}$$

Assuming same LCM, core material and Nc for ll modulation methods, the right side of

(16) will be same for all methods. Then the reduction of IZS means a smaller dc can be used. On the other hand, according to (14), Ac can also be reduced since LCM is same. In this way, the core size can be reduced since both Ac and dc can be smaller.

According to above analysis, the CMI sizes resulted by different modulation methods are directly related to the maximum ZSC generated by these methods. Compared with interleaved SVM, the maximum ZSCC of the proposed method is much smaller. Since both methods have the same CMV magnitude, the CMC should be similar, thus the ZSC of the proposed method will be smaller than that in the interleaved SVM. As to comparing with interleaved DSVM, the proposed method has smaller ZSCC and CMC, hence smaller ZSC. And compared with the method in [25], both methods have the same ZSCC maximum value. But since the proposed method has smaller CMC value as analyzed in previous part, the ZSC of the proposed method is smaller than the method in [25]. To sum up,compared with existing methods, a smaller CMI size can be used if the proposed method isapplied.

SWITCHING LOSSES:

When M is 1, the proposed scheme becomes DSVM. Hence the switching frequency is of 2/3 of the sampling frequency. The specific switching frequency of the proposed scheme cannot be directly calculated as it is affected by the modulation index and

International Journal of Research
Available at https://journals.pen2print.org/index.php/ijr/
e-ISSN: 2348-6848
p-ISSN: 2348-795X
Volume 06 Issue 07
June 2019

carrier-ratio. But the general relationship between switching frequency fswand M can be obtained. When M drops from 1 to 3 /3, the reference voltage vector starts entering sub-sector II and III, and the switching frequency increases. When M drops below 3 / 3, the reference voltage vector only passes sub-sector II and III. In this case, the proposed scheme becomes continuous SVM (CSVM) and the switching frequency is equal to the sampling frequency. Hence the switching loss is higher in low modulation index range than in high modulation index range. But the overall switching loss of the proposed scheme is somewhere between the CSVM and DSVM.

$$SLF_{M>1} = \begin{cases} 1-\frac{1}{2}\cos(\varphi) & 0 \le \varphi \le \frac{\pi}{3} \\ \frac{\sqrt{3}}{2}\sin(\varphi) & \frac{\pi}{3} \le \varphi \le \frac{\pi}{2} \end{cases}$$

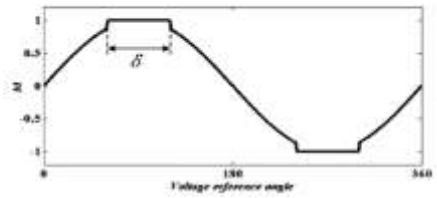


Fig 6.5 the modulating signal of the proposed method when m> root3/3

When M drops from 1 but is larger than 3 / 3 the clamping period of each phase is shortened. Then δ enters the SLF, as expressed in (18).
The relationship between δ and M can be obtained by

$$\delta = \frac{2\pi}{3} - 2\arcsin\left(\frac{1}{2M}\right) \qquad 0 < \delta < \frac{\pi}{3}$$

$$SLF_{0<M\le\frac{\sqrt{3}}{3}} = 1 \qquad -\frac{\pi}{2} \le \varphi \le \frac{\pi}{2}$$

When M is smaller than 3 / 3, the SLF constantly equals to 1, as indicated in (20). Substituting (19) into (18), the SLFof the proposed method with respect to M and power factor angle can be obtained. The SLF is plotted in Fig.11.

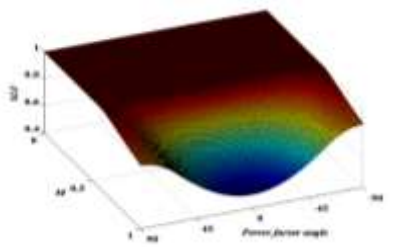


Fig 6.6 SLF of the proposed method with respect to modulation index and power factor angle

From Fig.6.6 one can see that when M is larger than 3 / 3 , the switching losses are always lower than that of conventional SVM over all power factor angle range. Compared to the method in [25], up to 55% loss reduction can be achieved when power factor is unity and M is 1, while 9% loss reduction is achieved when M is smaller than 3 / 3 . The lower switching losses make the proposed method suitable for various kinds of applications, not only for reactive power compensation.

SIMULATION:

Simulation verification of the proposed method is conducted using Simulink/Matlab. The simulation parameters are listed in Table VIII. The simulated waveforms of phase A current (IA), ZSCC, and CMV when M is 1, 0.7, 0.5, and 0.3, are shown in Fig. 12. The ZSCC and CMV waveforms under these conditions show that the simulation results are in agreement with the analysis presented in Section III. Low frequency fluctuation of ZSCC is eliminated by the designed switching sequence. And magnitude of CMV is limited within Vdc/6 (100V).

The interleaved SVM shows the same CMV magnitude. The maximum CMV magnitude of interleaved DSVM is 300V as expected. The simulation results of ZSCC peak value with respect to modulation index for the proposed method is obtained using a modulation index step of 0.01. The ZSCC peak values of interleaved SVM and interleaved DSVM are obtained using modulation index

International Journal of Research
Available at https://journals.pen2print.org/index.php/ijr/
e-ISSN: 2348-6848
p-ISSN: 2348-795X
Volume 06 Issue 07
June 2019

step of 0.1. The results are shown in Fig. 13, which is identical with the analytical results shown in Fig. 4 and Fig. 9.

Table 7.1 The simulation parameteres

Parameter	Value
DC link voltage, V_{dc}	600 V
Sampling frequency, f_s	3000 Hz
ZSCC filter, L_{cm}	7 mH
Load resistance, R	10 Ohm

The THD curve of phase A current of the proposed method is presented in Fig. 14, compared with the THD of interleaved SVM and inter leaved DSVM. It shows that the output quality of the proposed method is better than interleaved SVM but worse than the interleaved DSVM when M is low. But when M is larger than 0.7 the proposed method shows the best THD performance. In addition, the output current low-order harmonics with respect to the fundamental component are compared as shown in Fig. 15. Generally, the low-order harmonics of all three methods are very small. For both 5th order and 7th order harmonics, the interleaved DSVM method has the worst performances at high M range, while the interleaved SVM and the proposed method have comparable performances.

It should be noted that the load in simulation is resistive, thus the THD is influenced by the output current ripple as well. Since interleaved DSVM has much smaller ripple current than interleaved SVM when 0.3<M<0.8 [25], it is reasonable that the THD of interleaved DSVM is much lower than that of interleaved SVM in this M range as shown in Fig. 14. The output ripple current resulted from the proposed method should be between the interleaved DSVM and the interleaved SVM. But for practical applications, the load is usually inductive thus all three methods have comparable performance in terms of outputquality.

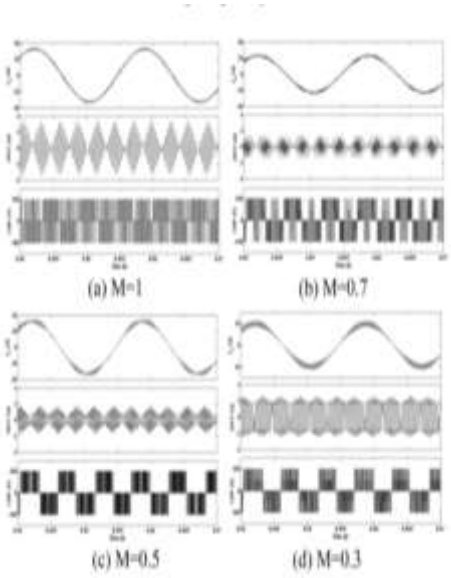


Fig 7.1simulation results of the proposed method under different modulation index.(upper trace: ia;middle:zscc;lower:cmv)

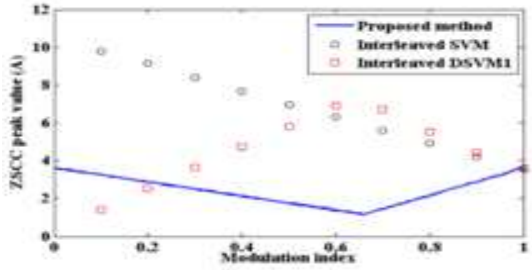


Fig 7.2 the simulation results of zscc peak value with respect to modulation index

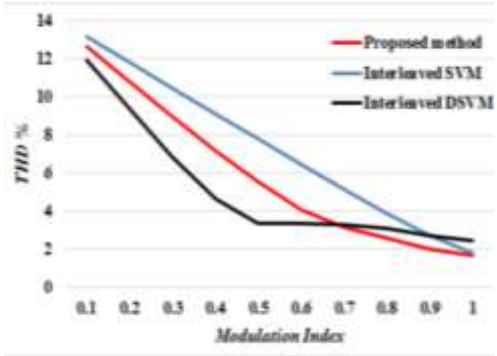


Fig 7.3thd comparison of the three methods

International Journal of Research
Available at https://journals.pen2print.org/index.php/ijr/
e-ISSN: 2348-6848
p-ISSN: 2348-795X
Volume 06 Issue 07
June 2019

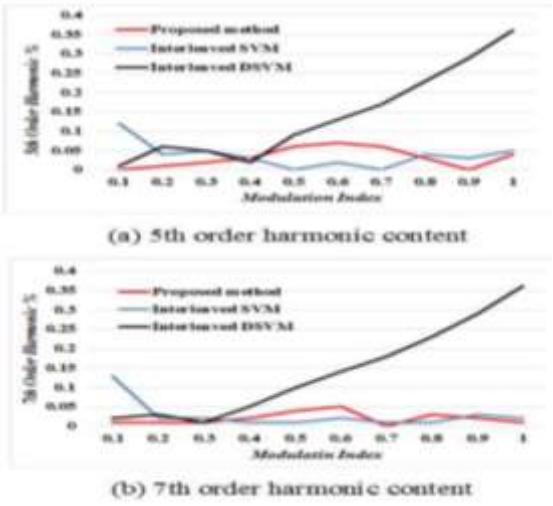


Fig 7.4 low order harmonic content comparision

EXPERIMENTAL RESULTS:

The proposed method is implemented on a lab prototype with two paralleled three-phase VSCs. Each VSC is constructed by Semi kron IGBT SKM75GD123D. The system is controlled by DSP TMS320F2812. The line inductor of 2.5mH is used. A resistive load of 10 Ohm is used. The DC link voltage is set to 200V. The sampling frequency is 2880Hz. The experimental results when M is 0.9, 0.6, and 0.3, are presented in Fig. 16. In the figures, the line current of phase A IA is illustrated in green, ZSCC is in red, and CMV is in blue. The ZSCC is measured by summating the three- phase current of one converter, as presented in (2). By its definition, the CMV is the measured voltage between the neutral point of DC link and the neutral point of the load.

As shown from the experimental results, the waveform of ZSCC haslittle low-frequency variations. But due to the existence of hardware asymmetric and uncertainties, the waveform cannot be as perfect as in simulation, and the experimental results of ZSCC peak value may be slightly higher than those in the simulation results. The ZSCC peak values in full modulation range are measured, as shown in Fig. 17. The relationship between ZSCC and modulation index can still be confirmed. The experiment results also show that the magnitude of CMV islimited to about 33V, which is identical with the analytical value of Vdc/6. Fig. 18 presents the THD of the measured line current. A comparison with the simulation results using the same parameters is also illustrated in Fig. 18. It showsthat the experiment results are very close to the simulation results, thus the output quality of the proposed method istestified.

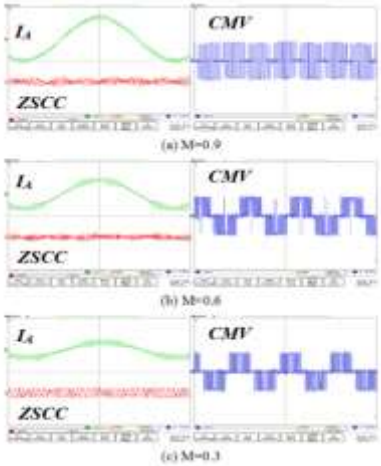


Fig 7.5 experimental results (.IA:2A/div,ZSCC:6A/DIV,CMV:20V/div)

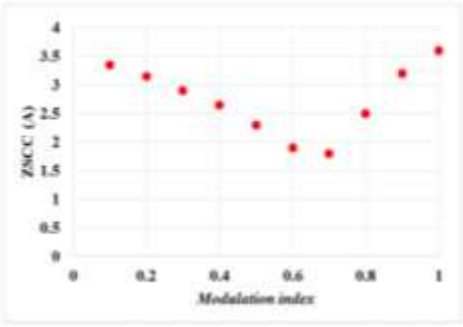


Fig 7.6 experimental results of zscc peak values with respect to modulation index

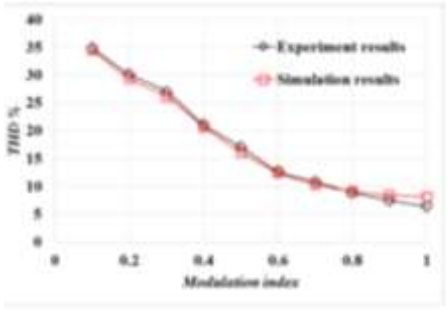


Fig 7.7 The experimental results and simulation results of line current THD

CONCLUSION

A SVM scheme is proposed in this paper for the parallel VSCs system with single phase inductor or CMI as filter. The proposed scheme aims to reduce the peak value of ZSCC and CMV at the same time. In the proposed scheme, the null- vectors for single converter are not used. But for three-level output, zero-vector can be realized by some combinations of active vectors of the two converters, thus the output quality is not seriously negatively affected. Through proper design of switching sequence, the magnitude of both ZSCC and CMV can be reduced in the proposed method. Compared with other modulation methods, the proposed method has the lowest ZSCC peak value when modulation index is between 0.5 and 1. It also has the same maximum ZSCC peak value as the method in [25]. On the other hand, the CMC of the proposed method is lower than the method in [25] since the magnitude of CMV is reduced from Vdc/2 to Vdc/6 during entire modulation index range.

Since both ZSCC and CMC contribute to the flux linkage of CMI, the reduction of both ZSCC and CMC makes the proposed method have smallest CMI size compared to existing methods. Further more,the proposed method is suitable for practical application since there is only one switching action at a time. When modulation index is higher than $3/3$, the switching losses are lower than that of conventional SVM for full power factor angle range. Otherwise the switching losses are the same as that of conventional SVM. The THD performance of the proposed method is verified through simulation and experimental study, suggesting that the proposed method has a similar THD performance compared with existing methods. The ZSCC and CMV suppression performances of the proposed scheme are also verified through experimental results

REFERENCES

[1] F. Ueda, K. Matsui, M. Asao, K. Tsuboi, "Parallel-connections of pulsewidth modulated inverters using current sharing reactors," IEEE Trans. Power Electron.,vol10, no.6, pp.673- 679, Nov 1995.

[2] C. L. Chen, Y. Wang, J. S. Lai, Yuang-Shung Lee, D. Martin, "Design of Parallel Inverters for Smooth Mode Transfer Microgrid Applications," IEEE Trans. Power Electron, vol.25, no.1, pp.6-15, Jan.2010.

[3] X. Yu, A.M. Khambadkone, "Reliability Analysis and Cost Optimization of Parallel-Inverter System," IEEE Trans. Ind. Electron., vol.59, no.10, pp.3881-3889, Oct.2012.

[4] Ko, Y.-J.; Lee, K.-B.; Lee, D.-C.; Kim, J.-M., "Fault diagnosis of three-parallel voltage-source converter for a high-power wind turbine," IET Power Electron., vol.5, no.7, pp.1058-1067, August2012.

[5] Chen, T.-P., "Circulating zero-sequence current control of parallel three-phase inverters," Proc. IEE Electr Power Appl, vol.153, no.2, pp.282-288, 2 March2006.

[6] Ching-Tsai Pan; Yi-Hung Liao, "Modeling and Coordinate Control of Circulating Currents in Parallel Three-Phase Boost Rectifiers," IEEE Trans. Ind. Electron., vol.54, no.2, pp825- 838, April2007.

[7] Prasad, J.S.S.; Narayanan, G., "Minimization of Grid Current Distortion in Parallel-Connected Converters Through Carrier Interleaving," IEEE Trans. Ind. Electron., vol.61, no.1, pp.76-91, Jan.2014.

[8] Di Zhang; Wang, F.; Burgos, R.; Rixin Lai; Boroyevich, D., "DC-Link Ripple Current Reduction for Paralleled Three-Phase Voltage-Source Converters With Interleaving," IEEE Trans. Power Electron., vol.26, no.6, pp.1741-1753, June2011.

[9] Di Zhang; Wang, F.; Burgos, R.; RixinLai; Boroyevich, D., "Impact of Interleaving on AC Passive Components of Paralleled Three-Phase Voltage-Source Converters," IEEE Trans. Ind. Appl., vol.46, no.3, pp.1042-1054, May-june2010.

[10] Simanjorang, R.; Miura, Y.; Ise, T.;

Sugimoto, S.; Fujita, H., "Application of Series Type BTB Converter for Minimizing Circulating Current and Balancing Power Transformers in Loop Distribution Lines," In Proc. PCC 2007 , pp.997-1004, 2-5 April 2007.
[11] Tsai-Fu Wu; Yu-En Wu; Hui-Ming Hsieh; Yu-Kai Chen, "Current Weighting Distribution Control Strategy for Multi-Inverter Systems to Achieve Current Sharing," IEEE Trans. Power Electron., vol.22, no.1, pp.160-168, Jan.2007.
[12] Baoming Ge; Xi Lu; Xianhao Yu; Maosong Zhang; Fang Zheng Peng, "Multiphase- Leg Coupling Current Balancer for Parallel Operation of Multiple MW Power Modules," IEEE Trans. Ind. Electron., vol.61, no.3, pp.1147-1157, March2014.
[13] Capella, G.J.; Pou, J.; Ceballos, S.; Zaragoza, J.; Agelidis, V.G., "Current-Balancing Technique for Interleaved Voltage Source Inverters With Magnetically Coupled Legs Connected in Parallel," IEEE Trans. Ind. Electron., vol.62, no.3, pp.1335- 1344, March2015.
[14] Asiminoaei, L.; Aeloiza, E.; Enjeti, P.N.; Blaabjerg, F., "Shunt Active-Power- Filter Topology Based on Parallel Interleaved Inverters," IEEE Trans. Ind. Electron., vol.55, no.3, pp.1175- 1189, March2008.
[15] Cougo, B.; Gateau, G.; Meynard, T.; Bobrowska-Rafal, M.; Cousineau, M., "PD Modulation Scheme for Three-Phase Parallel Multilevel Inverters," IEEE Trans. Ind. Electron., vol.59, no.2, pp.690-700, Feb.2012.
[16] Narimani, M.; Moschopoulos, G., "Three-Phase Multimodule VSIs Using SHE-PWM to Reduce Zero-Sequence Circulating Current," IEEE Trans. Ind. Electron.,vol.61, no.4, pp.1659- 1668, April2014.
[17] Ewanchuk, J.; Salmon, J., "Three-limb Coupled Inductor Operation for Paralleled Multi-level Three-Phase Voltage Sourced Inverters," IEEE Trans. Ind. Electron., vol.60,no.5, pp.1979-1988, May2013.
[18] Kun Xing; Lee, F.C.; Borojevic, D.; ZhihongYe; Mazumder, S., "Interleaved PWM with discontinuous space-vector modulation," IEEE Trans. Power Electron., vol.14, no.5, pp.906- 917, Sep1999.
[19] Di Zhang; Fei Wang; Burgos, R.; Boroyevich, D., "Common- Mode Circulating Current Control of Paralleled Interleaved Three-Phase Two-Level Voltage-Source Converters With Discontinuous Space-Vector Modulation," IEEE Trans. Power Electron., vol.26, no.12, pp.3925-3935, Dec.2011.
[20] Gohil, G.; Maheshwari, R.; Bede, L.; Kerekes, T.; Teodorescu, R.; Liserre, M.; Blaabjerg, F., "Modified Discontinuous PWM for Size Reduction of the Circulating Current Filter in Parallel Interleaved Converters," IEEE Trans. Power Electron., vol.30, no.7, pp.3457-3470, July2015.
[21] Cougo, B.; Meynard, T.; Gateau, G., "Parallel Three-Phase Inverters: Optimal PWM Method for Flux Reduction in Intercell Transformers," IEEE Trans. Power Electron., vol.26, no.8, pp.2184-2191, Aug.2011.
[22] Cougo, B.; Meynard, T.; Gateau, G., "Impact of PWM methods and load configuration in the design of intercell transformers used in parallel three-phase inverters," In Proc. IEEE ECMSM, 2013, pp.1-6, 24-26 June2013.
[23] Muetze, A.; Sullivan, C.R., "Simplified Design of Common- Mode Chokes for Reduction of Motor Ground Currents in Inverter Drives," IEEE Trans. Ind. Appl., vol.47, no.6, pp.2570- 2577, Nov.-Dec.2011.
[24] Tallam, R.M.; Leggate, D.; Kirschnik, D.W.; Lukaszewski, R.A., "Reducing Common-Mode Current: A Modified Space Vector Pulsewidth Modulation Scheme," IEEE Ind. Appl. Mag., vol.20, no.6, pp.24-32, Nov.-Dec.2014.
[25] Ogasawara, S.; Takagaki, J.; Akagi, H.; Nabae, A., "A novel control scheme of a parallel current-controlled PWM inverter," IEEE Trans. Ind. Appl., vol.28, no.5, pp.1023-1030, Sep/Oct1992.
[26] Hou, C-.C.; Shih, C-.C.; Cheng, P-.T.; Hava, A. M., "Common- Mode Voltage Reduction Pulsewidth Modulation Techniques for Three-Phase Grid-Connected Converters,"

IEEE Trans. Power Electron., vol.28, no.4, pp.1971-1979, April2013.
[27] Chung-ChuanHou, "A Multicarrier PWM for Parallel Three- Phase Active Front- End Converters," IEEE Trans. Power Electron., vol.28, no.6, pp.2753-2759, June2013.
[28] Hava, A.M.; Un, E., "Performance Analysis of Reduced Common-Mode Voltage PWM Methods and Comparison With Standard PWM Methods for Three-Phase Voltage-Source Inverters," IEEE Trans. Power Electron., vol.24, no.1, pp.241- 252, Jan.2009.
[29] B. Wu, High-Power Converters and AC Drives. Wiley-IEEE Press, 2006, pp. 101-115.
[30] Muetze, A., "Scaling Issues for Common-Mode Chokes to Mitigate Ground Currents in Inverter-Based Drive Systems," in IEEE Trans. Ind. Appl., vol.45, no.1, pp.286-294, Jan.-feb.2009.
[31] Hava, A.M.; Kerkman, R.J.; Lipo, T.A., "Simple analytical and graphical methods for carrier-based PWM-VSI drives," IEEE Trans. Power Electron., vol.14, no.1, pp.49- 61, Jan 1999.