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Low-Voltage Switched-Op Amp Circuits

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ABSTRACT

With the demand of low power applications, running circuits with reduced supply voltage can be of great advantage. Switched capacitor circuit is well known for their high linearity even with voltage supply variation since the capacitor value is only dependent on the process. However, when running the switched capacitor circuit with a reduced voltage supply, problems with the switches arise as they cease to function within a portion of the operating voltage range. A technique called switched OpAmp is proposed as a solution. The problematic switches are replaced with OpAmps that are capable of switching ON and OFF to mimic the operation of the switches. This method isproven to be feasible along with some power savings since the OpAmp is in operation for only half of the clock cycle. New research proposed a fully differential version of the switched OpAmp along with a fast common mode feedback circuit that reduce the "turn on" time of the OpAmp such that the sampling frequency can be greatly increased. This improved switched OpAmp circuit is capable of running at 1.0V in 0.35umprocess. Future research is targeted for further reducing the "turn on" time of the switched OpAmp by using new common mode feedback circuit. As a result, faster sampling frequency can be achieved.

KEYWORDS

capacitor circuits; mosfet; fet; poly-poly capacitor

INTRODUCTION

In the last decade, one of the aims of the electronic research is towards low power applications. With the need of portable devices in the market, an important specification is the available battery life of the equipment. For example, business users cannot tolerate to have their cell phones charged after a few conversations. Thus, the transceiver integrated circuit (IC), which usually is the main power consumer, should be designed such that it consumes as little power as possible when it is in operation. From the classical analysis of complementary metal oxide semiconductor (CMOS) [1], feasible ways to reduce the power consumption include reducing voltage swing and voltage supply of the circuit. There are two ways to reduce the voltage swing of the signals. First is tocreate special circuitry to generate the reduced signal swing with the regular power supply, which adds complexity. Second is to run the circuit under a lowered voltage supply and in effect, reduced the voltage swing of the signal. The second option seems to be very attractive because power consumption decreases withthe voltage supply in a square law relationship. With technology scaling, power supply voltage has been scaled down from 3.3V (0.35umCMOS) to currently 1.2V (0.13umCMOS). This definitely introduced a huge amount of power saving along with performance enhancement. However, it is even more advantageous if the device can operate with a supply voltage that is even lower than the normal specified level. Switched capacitor (SC) circuit has been a popular choice in circuit design. Not to mention that they can convert the signal into the digital domain, they also provide high linearity that is essential to moderncircuitry [1]. This paper will focus on the problems faced with switched capacitor circuits designed to run on a reduced voltage supply along with the proposed solutions.

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THE BASICS OF SWITCHED CAPACITOR CIRCUITS

Figure 3-1 shows a typical SC circuit used in an integrator. The circuit consists of four MOSFET switches, an OpAmp and two capacitors. The SC circuit requires a set of non-overlapping clocks, φ1and φ2. In φ1, the integrator is in sampling mode where the capacitor C1is charged to voltage VI. In φ2, the integrator is in integration mode where the charge in C1is transferred to C2. The components are described in details in the following sub-sections.

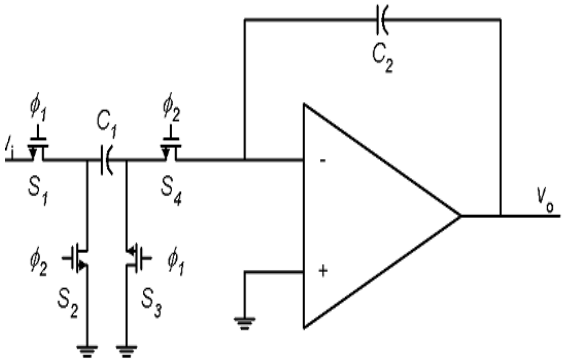

Figure 3-1 Switched capacitor circuit used in an integrator.

As the name of the switched capacitor circuit suggested, capacitor is an essential element in all SC circuits, i.e. integrators. There are several implementations of capacitor in an IC. Namely, the metal-metal and poly-poly are popular choice due to their high accuracy in matching between other capacitors in the circuit. An illustration of the poly-poly realized capacitor is shown in Figure 3-2.

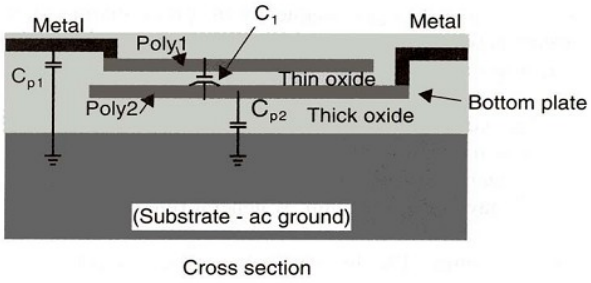

Figure 3-2 Cross sectional view of poly-poly capacitor.

Operational Amplifier (OpAmp) is the main driving component in the switched capacitor circuit. Thus, its performances, i.e. DC gain, unity gain frequency, slew rate and phase margin, directly affect the characteristic of the SC circuit. Modern popular OpAmp topology includes the folded cascade and two-stage Miller compensated OpAmp. They are suitable for working in today's low voltage supply environment due to the fact that they have less cascaded devices; thus, result in a larger signal swing.

MOSFET SWITCHES

MOSFET switch is implemented by either the choice of pMOS or nMOS, or both. Single MOSFET switch implemented by either pMOS or nMOS cannot pass logic '0' or logic '1' respectively. Figure 3-3 illustrates the reasoning.

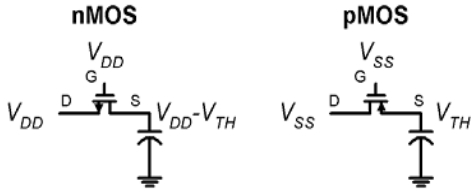

Figure 3-3 pMOS and nMOS implemented pass transistor switches.

To illustrate the idea, only nMOS version will be

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considered; however, the same reason can be applied for pMOS switch. For conduction, the nMOS must satisfy the following relationship, (V gs – V Th>0). The source of an nMOS is usually the side with the lower voltage and it is the right side of the nMOS in Figure 3-3. With the gate of the nMOS connected to Vdd, the maximum voltage that the capacitor can charge up is equal to (Vdd – Vth) before the nMOS goes into cut-off region. The same reasoning applies to the pMOS counterpart, which only passes voltage down to Vth. As a result, CMOS switch is usually used since they allow passing of full logic level, from Vss to Vdd. Figure 3-4 shows the range of voltages pass by the nMOS and pMOS in a CMOS switch. From Vss to 1.2V, only the nMOS is in conduction and pMOS is in cut-off. From 3.7Vto Vdd, only the pMOS is in conduction. Between 1.2Vand 3.7V, both device is ON and the conductance adds up.

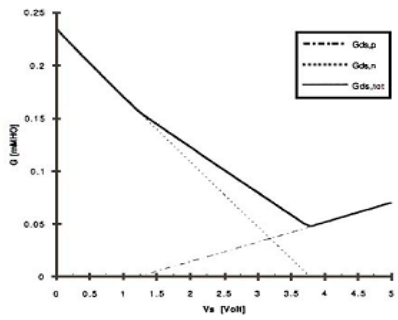

Figure 3-4 Conductance of CMOS a typical switch with $V_{DD} = 5V$.

PROBLEMS FACED BY SC CIRCUIT WITH LOW SUPPLY VOLTAGE

With the supply voltage lowered, i.e. 1.0V, capacitor faced no problem since it is only technology and fabrication dependent [2]. Nevertheless, OpAmp does have some impact when running with a reduced supply voltage. Due to the fact that transistors in an OpAmp are required to operate in the saturation region,(Vds> Vgs - Vth)cascading transistors to realize a higher equivalent impedance becomes more difficult because they reduce the available voltage swing. It is necessary to have the largest voltage swing to maintain a certain amount of noise margin when working with a reduced voltage supply. As a result, telescopic cascaded OpAmp is impractical when working with low voltage applications. A feasible OpAmp topology is the two-stage Miller compensated OpAmp. They provided the high DC gain by cascading a Trans conductance (Gm.) stage with an output stage (providing the large swing) together. The CMOS switch also has problem when working with a reduced voltage supply. For example, in the 0.35umprocess, the threshold voltage, Vth, of pMOS and nMOS is equal to 0.736V and 0.546V respectively [1]. When using allow voltage supply, Vdd =1.0V, the pMOS can pass 0.736V to Vdd and the nMOS can pass Vss to 0.454Vas explained previously. This is illustrated in Figure 4-1.

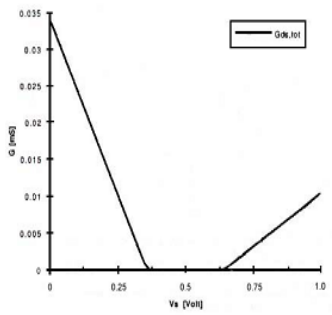

Figure 4-1 Conductance of CMOS a typical switch with $V_{DD} = 1V$.

Clearly, there is a region, 0.454Vto 0.736V, where both the pMOS and the nMOS are not conductive, which creates highnon-linearity in the SC circuit. From the above discussion, it is obvious that both the OpAmp and the MOSFET

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switches have problems when working with a reduced voltage supply. To find out the limiting factor, the simplified two-stage OpAmp circuit is shown in Figure 4-2.

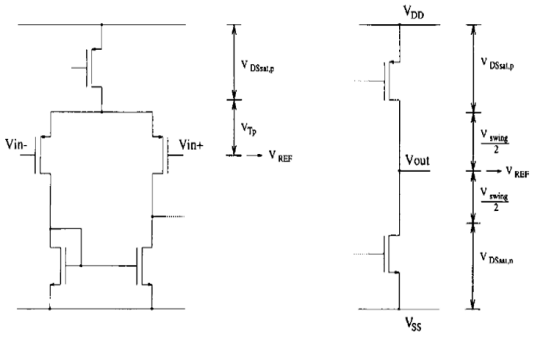

Figure 4-2 Simplified version of 2-stage OpAmp.

From Figure 4-2, it is apparent that the minimum Vdd to keep the OpAmp functional (i.e. all transistors in saturation) is equal to,

$$V_{DDopamp_{\min}} = V_{DSn_{sat}} + V_{swing} + V_{DSp_{sat}}$$

given that :

$$\frac{V_{swing}}{2} > V_{TH}$$

which is dominated by the output stage of the OpAmp [3]. For the MOSFET switch and assuming only nMOS is used, the gate voltage (clock signal) has to be at least Vth higher than the largest voltage that it wants to pass. With the configuration shown in Figure 4-2,the highest voltage that the nMOS switch needs to pass is the highest output voltage swing,

$$V_{DSn_{sat}} + V_{swing}$$

,

,so the gate voltage applied must be at least :

$$V_{Gswitch_{\min}} = V_{DSn_{sat}} + V_{swing} + V_{TH} = V_{DDswitch_{\min}} .$$

Therefore, the above analysis concluded that the switch is the limiting factor that dictates the minimum voltage supply since :-

$$V_{DDswitch_{\min}} > V_{DDopamp_{\min}} .$$

THE SWITCHED OP AMP TECHNIQUES

Another solution to the switch working with reduced voltage supply is the switched OpAmp technique. Switched OpAmp (SO) is introduced by Carols and Steyaert in 1994. The basic idea of the switched OpAmp is to replace the MOSFET switch with a special OpAmp that has an ON and OFF states. Carefully examining Figure 3-1 indicated that not all the MOSFET switches have problem with a low voltage supply. Switches 2, 3 and 4 have their source node always connected to Vss or a virtual ground; therefore, the problem is alleviated by using an nMOS, which can pass logic '0' completely. Switch 1 is connected to the output node of the previous stage and the capacitor. Its purpose is to let C1charges to the voltage of the previous output node. As a result, switch 1 is the only switch in the SC circuit that has the problem discussed above. It is not possible to remove that switch because it will short the output of the OpAmp to VSSin the φ2phase. However, since in φ2, the previous

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stage is in the sampling phase, the OpAmp can be switched off or turned into high impedance. This is equivalent to shutting off switch 1 in the signal path. Since the problematic switch is removed, the minimum power supply voltage is dictated by the OpAmp and is equal to :

$$V_{DDopamp_{\min}} = V_{DSn_{sat}} + V_{swing} + V_{DSp_{sat}}$$

if rail-to-rail voltage swing is desired [3]. Figure 6-1 shows the schematic of a switched OpAmp. This is the commonly known 2-stage Miller compensated OpAmp with two more transistors added, M9 and M10. They are driven by the same phase clock and served as the switches used to switch the OpAmp into a high impedance state.

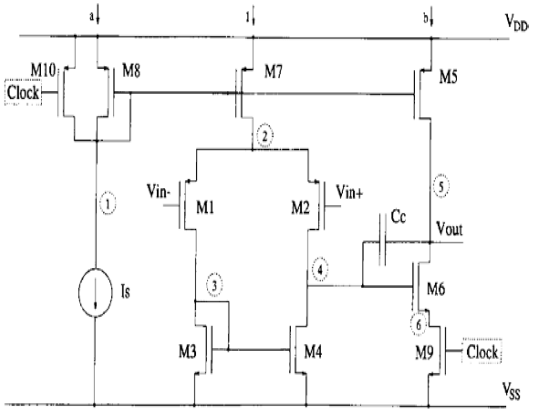

Figure 6-1 First proposed switched-OpAmp circuit.

When the clock is logic high, the OpAmp isin normal operation; M9 is ON and M10 is OFF. When the clock is logic low, the OpAmp is in high impedance state. M9 is OFF and prevents the discharge of the sampling capacitor in the following stage. Also M10 is ON such that the voltage VDDwill be applied to all the current mirrors and shuts them off. As a result, the OpAmp is completely shut off when the integrator is in sampling phase. To illustrate the operation of the SO circuit, the following example shows a problematic switch in a low-Q biquad filter is replaced with the SO circuit.

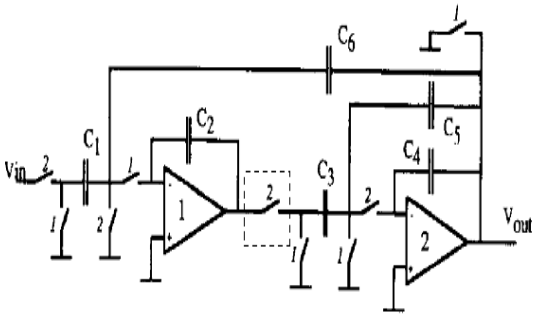

Figure 6-2 A typical low-Q biquad filter realized with SC circuit.

In Figure 6-2, the highlighted switchis replaced by the switched OpAmp integrator in Figure 6-3. An extra switched OpAmp in the SO circuit is needed because the first OpAmp in the SC circuit has to drive capacitor C3 at φ2. By shutting off SO1 (equivalent to first OpAmp in the SC circuit) at φ2in the SO circuit, it can no longer drive C3. Thus, a non-inverting delay (integrator 2) is put in. Although this increased the number of SO, the power dissipation is decreased by 0.75 because all three SO are in operation for half of the clock cycle [3]. Figure 6-4 detailed the operations of all the integrators in the low-Q biquad circuit.

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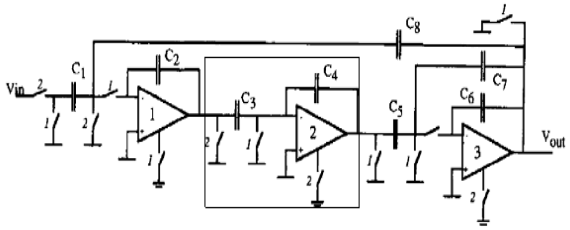

Figure 6-3 The low-Q biquad filter realized with SO circuit.

Time	Integrator 1	Integrator 2	Integrator 3
φ1	Integrate C2	Sample C3	Discharge C5
φ2	Sample C1	Integrate C4	Integrate C6/7

Figure 6-4 Table illustrating switched OpAmp circuit in action.

During the time that the OpAmp is recovering from OFF to ON state, transistor M8 is used to charge the gate capacitance of all the current mirrors, M5, M7 and M8. Thus, M8 should be sized considerably large. For transistor M10, it needs a very low on-resistance to ensure that a voltage close to VDDis applied to the gate of the current mirrors for proper shut off. Finally, for transistor M9, it needs to have a very low on-resistance because it might limits the voltage swing and degrade the voltage gain of the OpAmp. The exact sizing of the transistors is listed in [3].

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