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Design And Analysis Of Multi-Threshold Cmos Full Adder Using 90nm

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Abstract

High rate of power consumption in the digital integrated circuit is the major field of concern in the development of VLSI circuits. Demand of higher speed multiple operations and smaller process geometry contributes in the leakage power. So today leakage power consumption is the most important source of power dissipation rather than run time power consumption. Previously many techniques have been proposed for the leakage reduction. Amongst all MTCMOS technique carries the property of being most efficient in leakage reduction. In this paper we are going tost all MTCMOS technique carries the property of being most efficient in leakage reduction. In this paper we are going to analyze the different types of low power adder circuits with different types of low power design methodologies. The comparison results have also been displayed in this paper. The circuits are simulated in 90nm CMOS technology using tanner EDA simulator.

Key Words: Active mode, Combinational circuits, Leakage current, Multi-threshold voltage CMOS, Standby mode, Threshold Voltage.

1. Introduction

VLSI industry in the recent years suffers from the critical challenge in the management of power consumption. With the scaling down of the CMOS the supply voltage and threshold voltage is scaled down respectively. Leakage current has an inverse relationship with the threshold voltage the more and more threshold voltage is scaled, more is the leakage power dissipation [1].40% of the total power consumed by the device in active mode is dissipated by the leakage current [1]. With the aggressively scaling down of CMOS and need of multiple operations we are putting more and more transistors on a chip. With this increasing transistor density the

leakage current dominates the total power dissipation of the chip. On the other hand leakage current is the only source of power dissipation when device is in standby mode.

In portable device leakage current need to be managed as it directly affects the battery life of the device. Leakage needs to be reduced for the longer battery life. There are several leakage components which overall result in leakage power dissipation. The Leakage components in the deep submicron technology are depicted below in the figure.

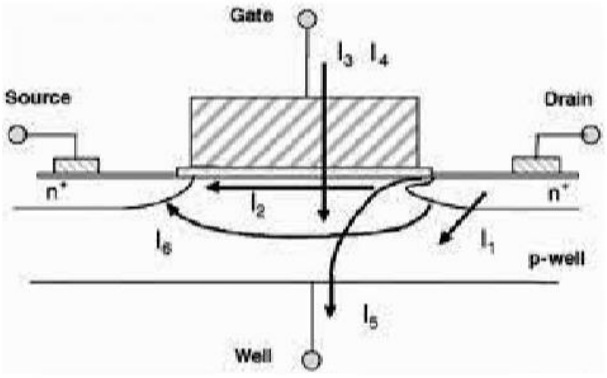

Fig:1.1. Leakage components in the deep submicron transistor

I1= Reverse bias p-n junction diode leakage

I2= Sub threshold leakage current

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I3= Gate oxide tunneling current

I4= Hot-carrier injection current

I5= Gate induced drain leakage current

I6= Channel punch-through

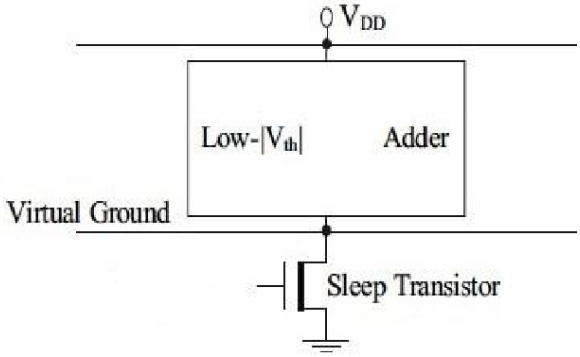

Fig:1.2: MTCMOS Technique (Dark Line shows High Vth)

The extensive development in the field of portable systems and cellular networks has intensified the research efforts in low power microelectronics. The low-power design has become a major design consideration. The design criterion of a full adder cell is usually multi-fold. Transistor count is, of course, a primary concern which largely affects the design complexity of many function units such as multiplier and algorithmic logic unit (ALU). The limited power supply capability of present battery technology has made power consumption an important figure in portable devices [1]. The speed of the design is limited by size of the transistors, parasitic capacitance and delay in the critical path. The driving capability of a full adder is very important, because, full adders are mostly used in cascade configuration, where the output of one provides the input for other. If the full adders lack driving capability then it requires additional buffer, which consequently increases the power dissipation. In the last decade, the full adder has gone through substantial improvement in power consumption, speed and size, but at the cost of weak driving capability and reduced voltage swing. However, reduced voltage swing has the advantage of lower power consumption [2].There is no ideal full adder cell that can be used in all types of applications.

2. IMPLEMENTATION

2.1.TRIMODE MTCMOS TECHNIQUE:

In this section the trimode MTCMOS technique has been reviewed. In this technique one PMOS and one NMOS transistor both of high Vth is connected parallel at the footer of the low Vth logic block. As the name Trimode suggest there are three modes of operation the intermediate mode between the ACTIVE and SLEEP mode known as PARK mode to reduce the ground bounce noise.

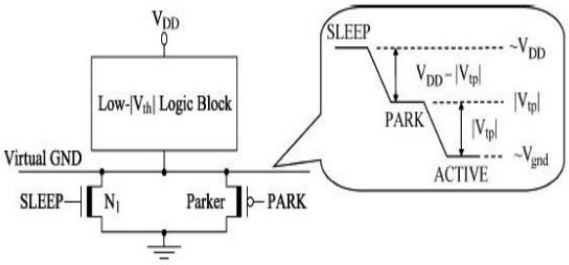

Fig.2.1: Trimode MTCMOS Technique

In the ideal situation both the transistors NMOS and PMOS at the footer is turned off to reduce the leakage power dissipation of the circuit. In ideal situation Voltage at the virtual line is maintained upto ~ Vdd (supply voltage). During the mode transition from SLEEP to ACTIVE mode the PMOS is turned on while NMOS is kept at cut off. In this situation circuit is said to be at PARK mode. The virtual line which was ~Vdd discharges till Vtp, now the reactivation process is completed by subsequently turning on the NMOS at the footer finally virtual line is discharged till ~ Vgnd. Here in this technique no additional circuitry is required for controlling the footer sleep transistors. The trade off in this technique is ground bounce noise, temperature and size of the transistors [4].

Different noise-aware MTCMOS circuit techniques originally intended for combinational circuits

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are presented in this section. The application space of these previously published noise-aware power gating techniques is expanded to the sequential circuits. The effectiveness of the techniques for suppressing the ground bouncing noise as well as the leakage currents while providing a data retention sleep mode in idle flip-flops is evaluated in the following sections.

A trimode power gating structure is proposed in [7] to lower the ground bouncing noise produced during the activation of idle MTCMOS circuits. The trimode circuit technique is a modification of the standard gated-ground MTCMOS circuits for low noise. A high-$|V_{th}|$ pMOS data preserving transistor (Parker) is connected in parallel with the footer (N1) to implement a low leakage data retention PARK mode in idle flip-flops as shown in Figure. During the PARK mode, the Parker is activated while is maintained cutoff. The virtual ground line is maintained at the threshold voltage of the Parker ($|V_{th}|$) . The circuit is capable of lowering the leakage power consumption while retaining the data by maintaining a reduced yet significant voltage difference (V_{dd}-$|V_{th}|$) between the power supply and the virtual ground line in the PARK mode.

2.2. DUAL-SWITCH MTCMOS TECHNIQUE:

In the Dual-Switch technique an intermediate mode is between the SLEEP and ACTIVE mode same as in Trimode technique. It is also an another technique that is adopted to suppress the Ground bounce noise, but comparatively more effective in terms of leakage reduction and ground bounce noise suppression as compared to the Trimode MTCMOS technique. As depicted in Fig. 3. A pair of high Vth NMOS and PMOS transistors is connected between the real and virtual supply line. At the ideal situation all the four sleep transistors are off. When mode transition is done the high Vth PMOS at the header and footer is turned on keeping the NMOS transistors at cut off.

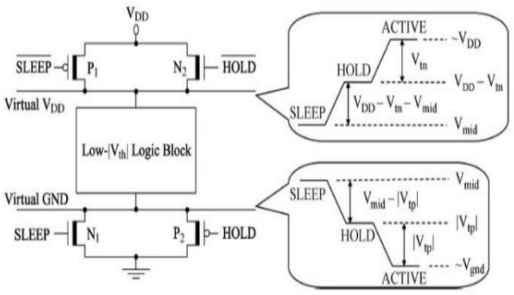

Fig. 2.2. Dual-Switch MTCMOS Technique

2.3. IMPROVED STACKING POWER GATING TECHNIQUE:

In Sleep transistor stacks, stacking power gating technique and a delay is introduced between the activation times of the transistors [6]. This, Keeps the ground isolated for a short time period during the transition of mode. The intermediate voltage at the node is controlled by using an additional capacitor which reduces the ground bounce noise. In this technique the second MOS transistor is used as diode connected MOS, which further reduces the ground bounce noise. The sleep transistors are connected to the low Vth logic block in the form of stack, which reduces the leakage power dissipation by the transistor stacking effect [6]. A capacitor C2 is additional which is inserted at the intermediate node VGND2 which controls the current flowing through drain and the sleep transistor M2 during the transition of mode.

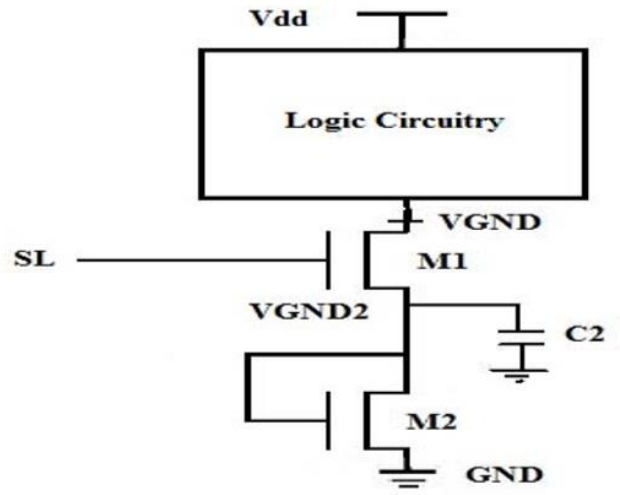

Fig. 2.3. Sleep transistors stacks MTCMOS technique propose

2.4. DIODE BASED STACKING POWER GATING TECHNIQUE:

In this strategy we incorporate the operation of the sleep transistor in the form of diode [7]. This technique is more effective in terms of leakage reduction and ground bounce noise. The sleep transistor is operated as a diode during mode transition for some time period. This limits a large amount of transient current which results in reduced ground bounce noise. Delay circuit used here to isolate the ground for some time during transition of SLEEP to ACTIVE mode. The transistor S2 is made to work in linear region instead of saturation region to decrease the current fluctuation which is achieved by placing a capacitor at the intermediate node [7].

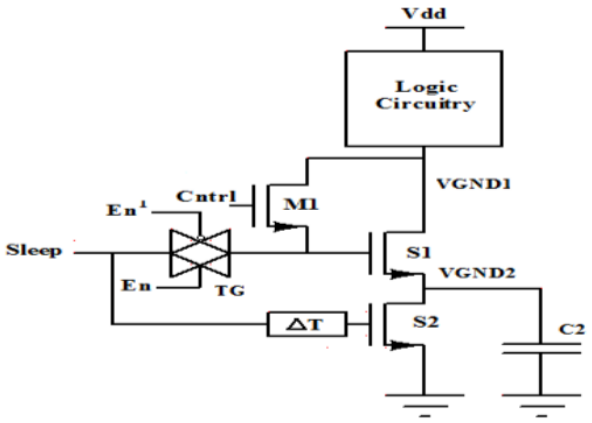

Fig.2.4. Diode based stacking power gating technique

3. TANNER EDA

The tool used for simulation purpose for the entire research work is Tanner EDA tool version 13.0 and micro wind for layout designing the features and functionality of this tool has been described below:

3.1 SIMULATION TOOL:

The design cycle for the development of electronic circuits includes an important pre-fabrication verification phase. Because of the expense and time pressures associated with the fabrication step, accurate verification is crucial to efficient design. The role of EDA tool is to help design and verify a circuit's operation by numerically solving the differential equations describing the circuit. These simulation results allow circuit designers to verify and fine-tune designs before submitting them for fabrication.

Tanner EDA tool is a complete circuit design and analysis system that includes:

Schematic Editor (S-Edit): Schematic editor is a powerful design capture and analysis package that can generate netlist directly usable in T-Spice simulations.

T-Spice Circuit Simulator:T-Spice performs fast and accurate simulation of analog and mixed analog/digital circuits. The simulator includes the latest and best device models available, as well as coupled line models and support for user- defined device models via tables or C functions. T-Spice uses an extended version of the SPICE input language that is compatible with all industry standard SPICE simulation programs. All of SPICE's device models are incorporated, as well as resistors, capacitors, inductors, mutual inductors, single and coupled transmission lines, current sources, voltage sources, controlled sources, and a full complement of the latest advanced semiconductor device models from Berkeley and Philips Labs.

Waveform Editor (W-Edit): W-Edit displays T-Spice simulation output waveforms as they are being generated during simulation. Visualizing the complex numerical data resulting from VLSI circuit simulation is critical to testing understanding, and improving those circuits. W-Edit is a waveform viewer that provides ease of use, power, and speed in a flexible environment designed for graphical data presentation.

Layout Editor (L-Edit): Tanner EDA tool includes L-Edit for layout editing, Interactive DRC for real-time design rule checking during editing, Standard DRC for hierarchical DRC, Standard Extract for netlist extraction, Standard LVS for layout versus schematic, Node Highlighting for highlighting all geometry associated with a node and SPR for standard cell place &route.

3.1.1 T-SPICE:

To transform your ideas into designs, you must be able to simulate large circuits quickly and with a high degree of accuracy. That means you need a simulation tool that offers fast run times, integrates with your other design tools, and is compatible with industry standards. Tanner T-Spice Circuit Simulator puts you in control of simulation jobs with an easy-to-use graphical interface and a faster, more intuitive design environment. With key features such as multi-threading support, device state plotting, real-time waveform viewing and analysis, and a command wizard for simpler SPICE syntax creation, T-Spice saves you time and money during the simulation phase of your design flow.

T-Spice enables more accurate simulations by supporting the latest transistor models—including BSIM4 and the Penn State Philips (PSP) model. Given that T-Spice iscompatible with a wide range of design solutions and runs on Windows and Linux platforms, it fits easily and cost effectively into your current tool flow.

T-Spice incorporates numerous innovations and improvements not found in other SPICE and SPICE-compatible simulators:

- **Speed:** T-Spice provides highly optimized code for evaluating device models, formulating the systems of linear equations, and solving those systems.
- In addition to the standard direct model evaluation, T-Spice also provides the option of table-base transistor model evaluation, in which the results of device model evaluations are stored in tables and reused
- **Convergence**: T-Spice uses advanced mathematical methods to achieve superior numerical stability. Large circuits and feedback circuits, impossible to analyze with other SPICE products, can be simulated in T-Spice.

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- **Accuracy**: T-Spice uses very accurate numerical methods and charge conservation to achieve superior simulation accuracy.
- **Macro modelling:** T-Spice simulates circuits containing “black box” macro devices. A macro device can directly use experimental data as its device model.
- Macro devices can also represent complex devices, such as logic gates, for which only the overall transfer characteristics, are of interest.
- **Input language extensions:** The T-Spice input language is an enriched version of the standard SPICE language. It contains many enhancements, including parameters, algebraic expressions, and a powerful bit and bus input wave specification syntax.
- **External model interface:** You can develop custom device models using C or C++.
- **Runtime waveform viewing:** The W-Edit waveform viewer displays graphical results during simulation. T-Spice analysis results for voltages, currents, charges, and power can be written to single or multiple files. Let’s see how to design for a CMOS inverter using tanner tools

4. SIMULATION AND COMPARISON RESULTS

The above techniques are simulated on Tanner EDA using 90nm process technology which supports the characterization of all the above mentioned techniques. The transistors used in the designing are of following values: High Vth NMOS =320 mV, low Vth NMOS = 72mV, High

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Vth PMOS = −273mV, Low Vth PMOS= −56mV [5].All the simulations are done for adder circuit. Table I shows the comparison of leakage current after applying Trimode, Dual Switch Mode, Improved Stacking and Diode based Stacking in the logic block for the input combination of ABC=000. The simulations are also done at different supply voltages ranging from 0.5V to 1V.From the Table below we can find that power dissipated is minimum in Diode based stacking technique.

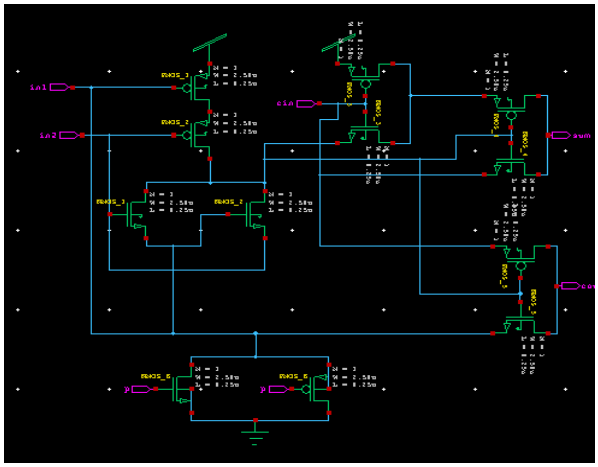

Fig.4.1 (a) . Trimode MTCMOS Technique Schematic diagram

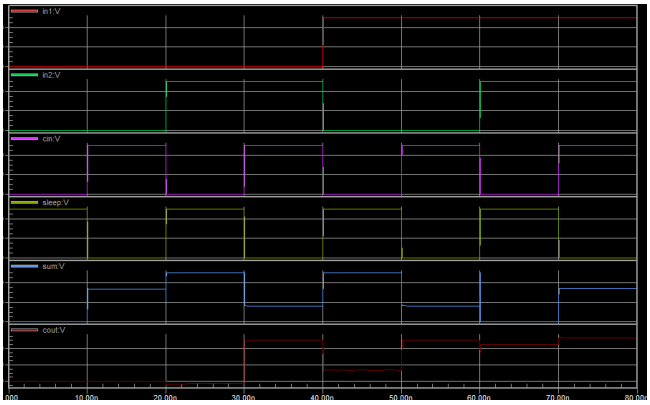

Fig.4.1 (b) . Trimode MTCMOS Technique Output waveform

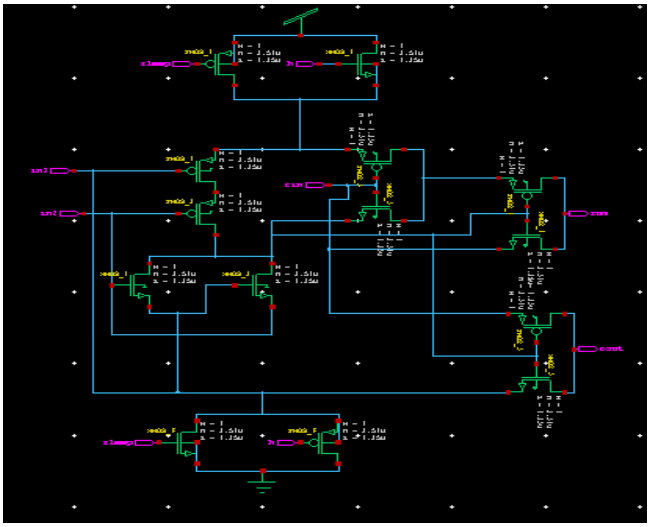

Fig.4.2 (a). Dual-SwitchMTCMOS Technique Schematic diagram

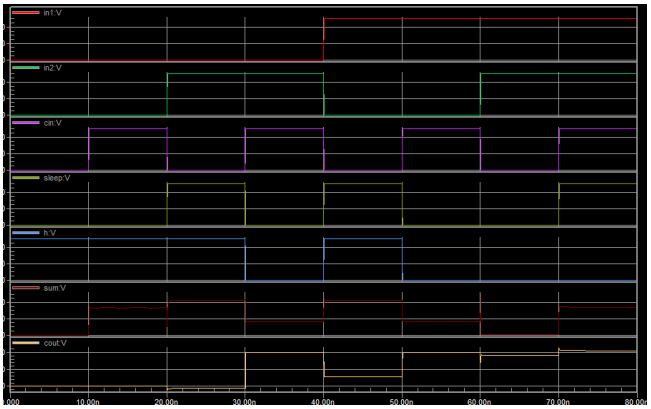

Fig.4.2 (b). Dual-Switch MTCMOS Technique Output waveform

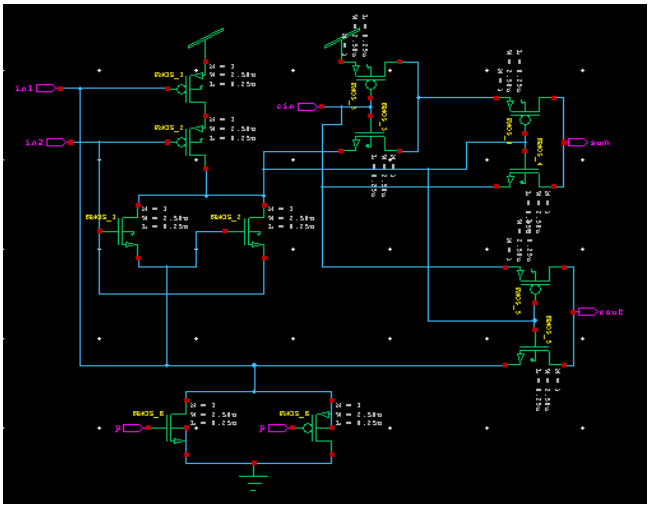

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Fig.4.3 (a). Improved stacking MTCMOS technique Schematic diagram

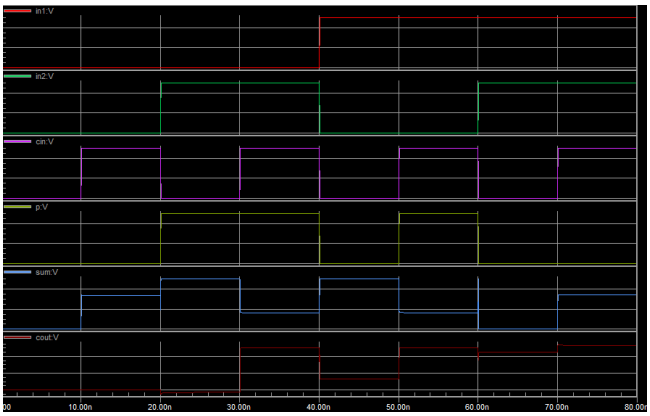

Fig.4.3 (b). Improved stacking MTCMOS technique Output

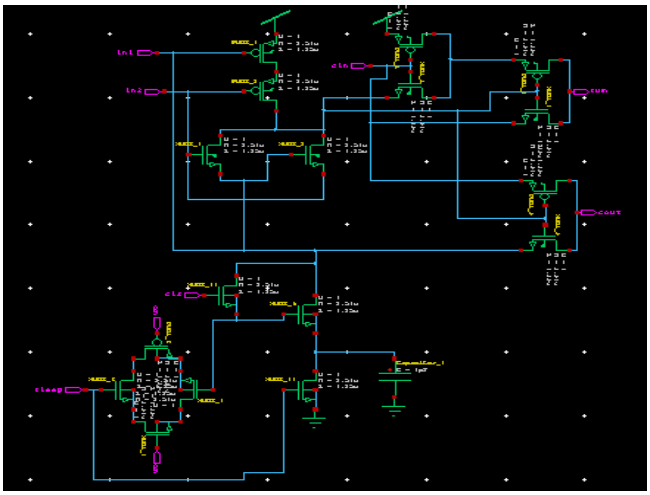

Fig.4.4 (a). Diode based stacking power gating technique Schematic diagram

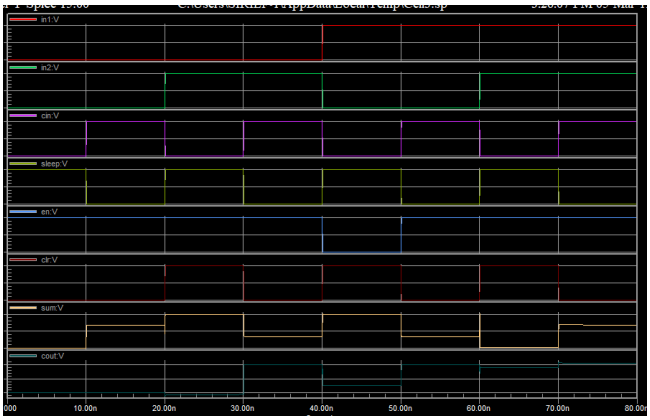

Fig.4.4 (b). Diode based stacking power gating technique Output waveform

SupplyVoltage (Volts)	Leakage Current(nA)			
	Trimode	Dual Switch Mode	Improved Stacking	Diode based Stacking
1	6.6	2.05	1.559	0.933
0.9	6.4	2.01	1.506	0.911
0.7	6.1	1.98	1.407	0.866
0.5	5.8	1.95	1.312	0.823

TABLE 4.1: Leakage current comparison between all techniques at combination of ABC=000

Table II shows the comparison between the highest and lowest value of leakage current calculated by applying Trimode technique and Diode based Stacking technique respectively for the input combination of ABC=000 and at different supply voltages. The leakage is minimized in Diode connected power gating as compared to Trimode technique as the sleep transistor in connected as Diode in Diode connected gating which completely cutoff the ground rail from the real ground.

Supply Voltage (Volts)	Leakage Current(nA)	
	Trimode	Diode based Stacking
1	6.6	0.933
0.9	6.4	0.911
0.7	6.1	0.866
0.5	5.8	0.823

TABLE 4.2: Leakage current at combination of ABC=000

Table III shows the leakage currents which is calculated after applying Trimode , Dual Switch Mode, Improved Stacking and Diode based Stacking for the input combination of ABC=111. The results are also simulated for the different supply voltages ranging from 0.5 V to 1 V. The circuit is simulated for the input combination of ABC=111. The comparison result shows that the diode based technique is the most efficient in terms of leakage current is drastic decrease in leakage current is due to the combined effect of transistor stacking and power gating.

Supply Voltage (Volts)	Leakage Current(nA)			
	Trimode	DualSwitch Mode	Improved Stacking	Diode based Stacking
1	4.01	2.85	1.95	1.32
0.9	4.07	2.63	1.57	1.28
0.7	4.58	2.49	1.45	1.12
0.5	4.56	2.34	1.28	1.04

TABLE 4.3: Leakage current comparison between all techniques at combination of ABC=111

5 CONCLUSION

Leakage current parameter in standard MTCMOS technique has been investigated in this paper. Different stand by leakage reduction techniques to suppress the leakage are presented. All the leakage suppression techniques provide significant leakage reduction compared with that of the classical MTCMOS circuit. Out of all the above mentioned techniques, Diode based stacking provides the most leakage reduction. The leakage reduction is due to the stacking phenomenon. This is best explained by the following given equation.

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