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Analysis and Design of A Low-Voltage Low-Power Double-Tail Comparator

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Abstract:
The need for ultra low-power, area efficient and high speed analog-to-digital converters is pushing toward the use of dynamic regenerative comparators to maximize speed and power efficiency. In this paper, an analysis on the delay of the dynamic comparators will be presented and analytical expressions are derived. From the analytical expressions, designers can obtain an intuition about the main contributors to the comparator delay and fully explore the tradeoffs in dynamic comparator design. Based on the presented analysis, a new dynamic comparator is proposed, where the circuit of a conventional double-tail comparator is modified for low-power and fast operation even in small supply voltages. Without complicating the design and by adding few transistors, the positive feedback during the regeneration is strengthened, which results in remarkably reduced delay time. Post-layout simulation results in a 0.18- µm CMOS technology confirm the analysis results. It is shown that in the proposed dynamic comparator both the power consumption and delay time are significantly reduced. The maximum clock frequency of the proposed comparator can be increased to 2.5 and 1.1 GHz at supply voltages of 1.2 and 0.6 V, while consuming 1.4 mW and 153 µW, respectively. The standard deviation of the input-referred offset is 7.8 mV at 1.2 V supply

INTRODUCTION

High Performance energy efficient logic style is one of the famous research topic in the field of VLSI circuits because of the continuous demands of power, speed and area constraints. As transistor integration increases, new advances are established in the concerned design strategies and related tools are used to design the VLSI circuits, which results cost effective and low power high performance VLSI circuits.

DIGITAL CIRCUITS

A digital circuit is a circuit where the signal must be one of two discrete levels. Each level is interpreted as one of two different states (for example, on/off, 0/1, true/false). Digital circuits use transistors to create logic gates in order to perform Boolean logic. This logic is the foundation of digital electronics and computer processing. Digital circuits are less susceptible to noise or degradation in quality than analog circuits. It is also easier to perform error detection and correction with digital signals. To automate the process of designing digital circuits, engineers use electronic design automation (EDA) tools, a type of software that optimizes the logic in a digital circuit.In this digital circuits, a digital comparator or magnitude comparator is a hardware electronic device that takes two numbers as input in binary form and determines whether one number is greater than, less than or equal to the other number. Comparators are used in central s (CPUs) and microcontrollers (MCUs). Examples of digital comparator include the CMOS 4063 and 4585 and the TTL 7485 and 74682-'89. For example, X NOR gate is a basic comparator, because its output is "1" only if its two input bits are equal. The analog equivalent of digital comparator is the voltage comparator. Many microcontrollers have analog comparators on some of their inputs that can be read or trigger an interrupt.

COMPARATOR

Comparator is one of the fundamental building blocks in most analog-to-digital converters (ADCs).A comparator is a device that compares two voltages or currents and outputs a digital signal indicating which is larger. It has two analog input terminals V_+ and V_- and one binary digital output V_o. The output is ideally

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$$V_o = \begin{cases} 1, & \text{if } V_+ > V_- \\ 0, & \text{if } V_+ < V_- \end{cases}$$

A comparator consists of a specialized high-gain differential amplifier. They are commonly used in devices that measure and digitize analog signals, such as analog-to-digital converters (ADCs), as well as relaxation oscillators.

DIFFERENTIAL VOLTAGE

The differential voltages must stay within the limits specified by the manufacturer. Early integrated comparators, like the LM111 family, and certain high-speed comparators like the LM119 family, require differential voltage ranges substantially lower than the power supply voltages (±15 V vs. 36 V). Rail-to-rail comparators allow any differential voltages within the power supply range. When powered from a bipolar (dual rail) supply,

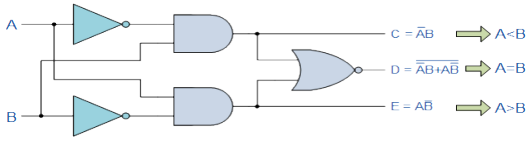
$$V_{S-} \leq V_+, V_- \leq V_{S+}$$

or, when powered from a unipolar TTL/CMOS power supply:

$$0 \leq V_+, V_- \leq V_{cc}$$

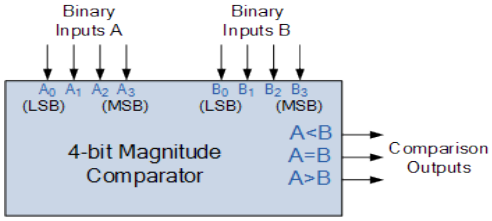
Specific rail-to-rail comparators with p-n-p input transistors, like the LM139 family, allow input potential to drop 0.3 volts below the negative supply rail, but do not allow it to rise above the positive rail.[2] Specific ultra-fast comparators, like the LMH7322, allow input signal to swing below the negative rail and above the positive rail, although by a narrow margin of only 0.2 V.[3] Differential input voltage (the voltage between two inputs) of a modern rail-to-rail comparator is usually limited only by the full swing of power supply

BIT DIGITAL COMPARATOR



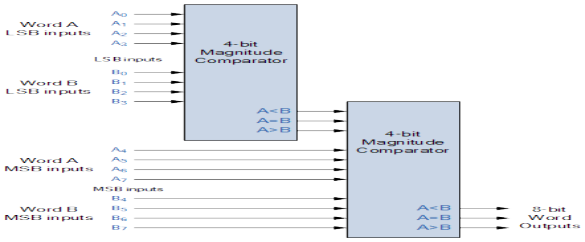
Then the operation of a 1-bit digital comparator is given in the following Truth Table.

BIT MAGNITUDE COMPARATOR



Some commercially available digital comparators such as the TTL 74LS85 or CMOS 4063 4-bit magnitude comparator have additional input terminals that allow more individual comparators to be "cascaded" together to compare words larger than 4-bits with magnitude comparators of "n"-bits being produced. These cascading inputs are connected directly to the corresponding outputs of the previous comparator as shown to compare 8, 16 or even 32-bit words

BIT WORD COMPARATOR



When comparing large binary or BCD numbers like the example above, to save time the comparator starts by comparing the highest-order bit (MSB) first. If equality exists, A = B then it compares the next lowest bit and so on until it reaches the lowest-order bit, (LSB). If equality still exists then the two numbers are defined as being equal. If inequality is found, either A > B or A < B the relationship between the two numbers is determined and the comparison between any additional lower order bits stops. Digital Comparator are used widely in Analogue-to-Digital converters, (ADC) and Arithmetic Logic Units, (ALU) to perform a variety of arithmetic operations

LITERATURE SURVEY

INTRODUCTION

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This section explains the papers which are referred for the entire project to implement the Constant Delay Logic style in Tanner EDA tool.

PAPERS REFERRED

Low-power logic styles: CMOS versus pass-transistor logic

NORA: A race free dynamic CMOS technique for pipelined logic structures

Zipper CMOS

Output prediction logic: A high-performance CMOS design technique

Low power arithmetic circuit in Feed Through dynamic CMOS logic

Analysis of high-performance fast Feed Through logic families in CMOS

Design of a 64-bit low-energy high-performance adder using dynamic Feed Through logic

Design of 64-bit Full Adder by using Dynamic Feed through Logic

LOW-POWER LOGIC STYLES: CMOS VERSUS PASS-TRANSISTOR LOGIC

This paper presents the comparison of Complementary Pass Transistor and Complementary CMOS based on full-adder circuits and proves Complementary Pass Transistor logic (CPL) to be much more power-efficient than complementary CMOS. However, new comparisons performed on more efficient CMOS circuit realizations and a wider range of different logic cells, as well as the use of realistic circuit arrangements demonstrate CMOS is to be superior to CPL in most cases with respect to speed, area, power dissipation, and power-delay products

EXISTING METHODOLOGIES

INTRODUCTION

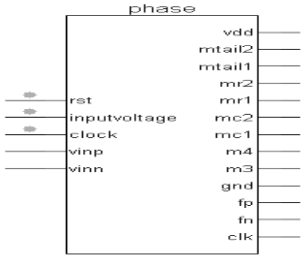
In this section, the basic fundamental building block of ADC i.e COMPARATOR is explained and when we analyzethesehigh speed ADCs, such as flash ADCs which require high-speed, low power comparators with small chiparea. To achieve this, we are going for conventional dynamic comparator and conventional double tail comparator.

CLOCKED REGENERATIVE COMPARATORS

CMOS fully dynamic latched comparators are majorly used in Analog to Digital converters (ADCs), data receivers and Memory Sense Amplifiers (SAs) because they provide high speed, reduced power consumption, full swing output and high input impedance. Dynamic latched comparators employ re-generative stage, which consist of cross coupled inverters, to provide a positive feedback mechanism. This regenerative stage is used to convert a differential voltage, from the input stage, into a full swing digital output state at a very fast rate. Clocked regenerative comparators have found wide applications in many high-speed ADCs since they can make fast decision due to the strong positive feedback in the regenerative latch. Recently many comprehensive analyses have been presented, which investigate the performance of these comparators from different aspects, such as noise, offset, random decision errors and kickback noise

PROPOSED DOUBLE-TAIL DYNAMIC COMPARATOR

demonstrates the schematic diagram of the proposed dynamic double-tail comparator. Due to the better performance of double-tail architecture in low-voltage applications, the proposed comparator is designed based on the double-tail structure. The main idea of the proposed comparator is to increase Vfn/fp in order to increase the latch regeneration speed. For this purpose, two control transistors (Mc1 and Mc2) have been added to the first stage in parallel to M3/M4 transistors but in a cross-coupled manner



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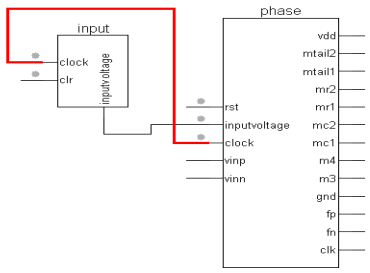
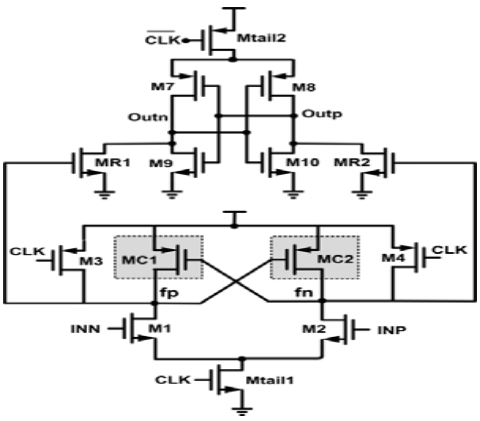
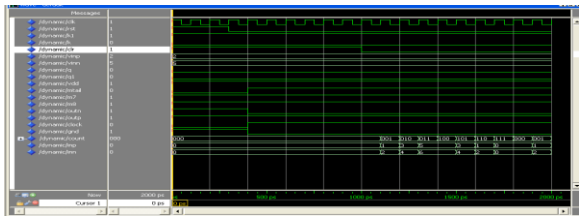
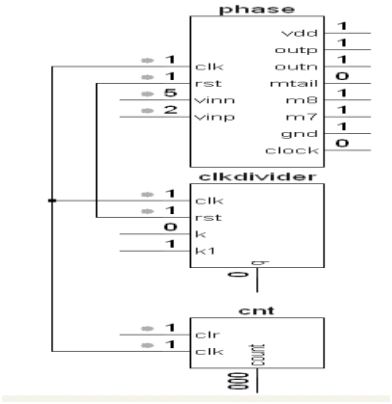




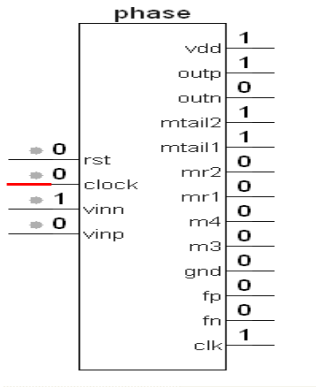
Design of Dynamic Clocked Comparator
Comparator is the basic building block for the ADC applications. This application module developed consists of a single-tail this comes under the clocked regenerative comparator that can make fast decisions with the positive feedback. The main parameters considered here are the clock inputs and with this the double tail comparator is developed.





Design of Double-Tail Comparator

This module is implemented to show the difference between the dynamic clocked regenerative comparator and the double-tail comparator. The conventional double tail comparator is developed and its delay analysis is performed. The analysis results help to find out the disadvantages of the current double-tail comparator design.



Design of Auto Tunable Threshold Comparator

This module is designed with the tuanble threshold.Using the auto-tunable threshold a comparator is capable of generating digital signal from analog input which can achieve good tolerance and efficiency.This module helps to avoid the kick-back noise and Mis-match in the existing double tail comparator design using autotunable threshold.

Design and Analysis of the Integration Module

We integrate all the sub-modules and their analysis and performance are implemented with the Model Sim software simulation results

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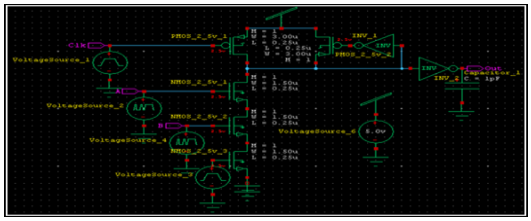
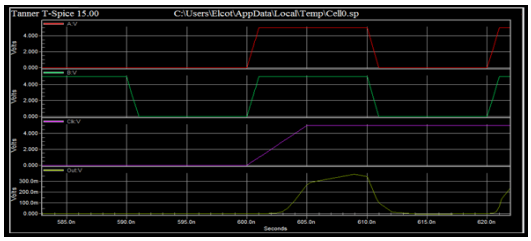
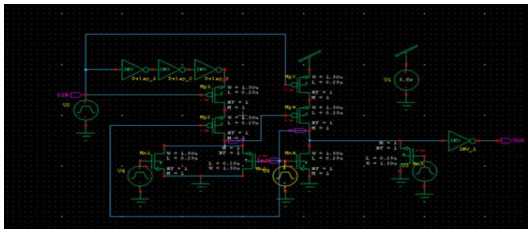
SIMULATION RESULTS

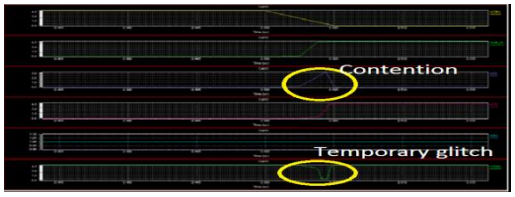
INTRODUCTION

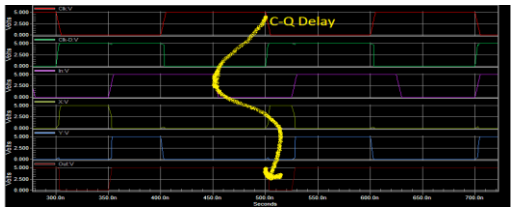
All simulation results are simulated in the schematic level in the Tanner EDA design environment. The conventional dynamic comparator, conventional double tail comparator and proposed comparator are designed, simulated and synthesized. The synthesized results of these comparators are in TABLE I



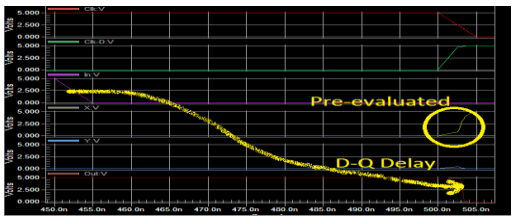






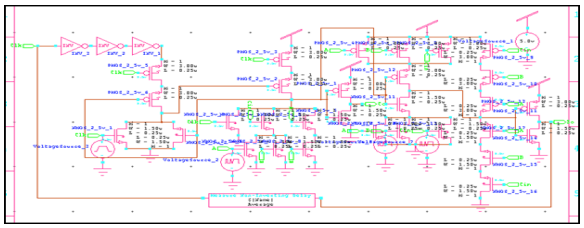


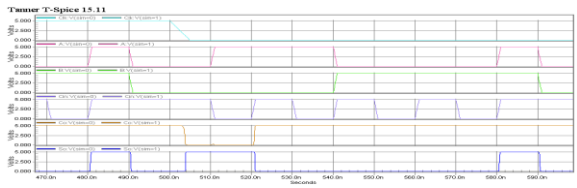
Output waveform of contention and C-Q delay modes of CD logic. In the contention mode, Out has temporary glitch. In the C-Q Delay mode, the delay is measured by the falling edge of both CLK and Out

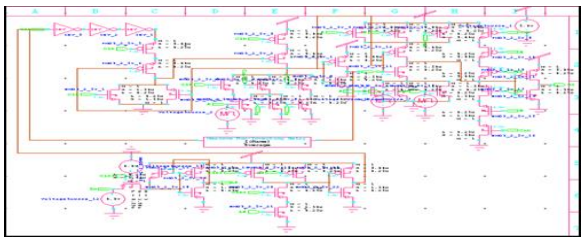


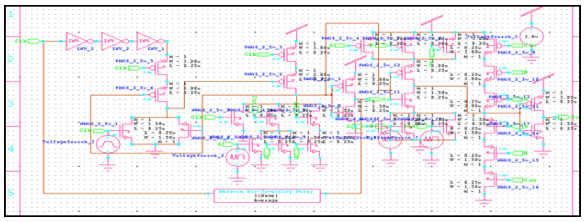
Output waveform of D-Q delay mode of CD logic. Here the output is pre-calculated before getting the inputs from the previous stage. The delay is measured by the falling edge of both Data and Out

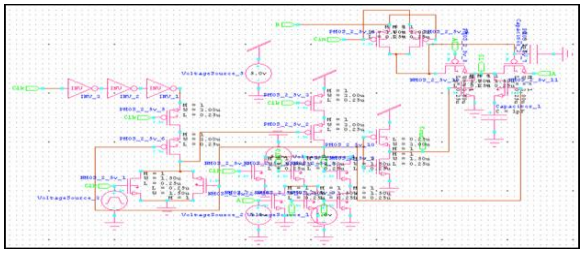
SIMULATIONS AND SYNTHESIS RESULTS

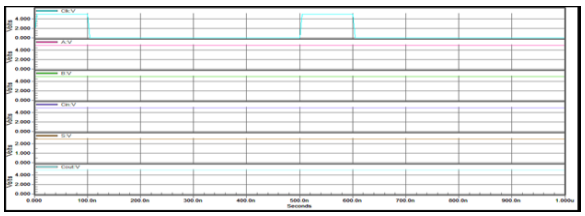












CONCLUSION

In this paper, we presented a comprehensive delay analysis for clocked dynamic comparators and expressions were derived. Two common structures of conventional dynamic comparator and conventional double-tail dynamic comparators were analyzed. Also, based on theoretical analyses, a new dynamic comparator with low-voltage low-power capability was proposed in order to improve the performance of the comparator. Post-layout simulation results in 0.18-μm CMOStechnology confirmed that the delay and energy per conversion Of the proposed comparator is reduced to a great extent in comparison with the conventional dynamic comparator and double-tail comparator.

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