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A Review on Power optimization of BIST circuit using low power LFSR

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Abstract: *In most number of electronic systems that are used in safety critical applications circuit testing has to be performed periodically. For these systems power dissipation due to BIST [built in self test] represents a significant percentage of overall power dissipation. The power dissipation during the test mode is 200% more than in normal mode. So, to reduce the power dissipation during the test mode for BIST circuit, we are using a low power LFSR. The correlation between consecutive patterns are higher in normal mode than during testing so, by using LPLFSR we are reducing the transitions between consecutive patterns generated by the conventional LFSR.*

Keywords- LFSR, Optimization, Low power, Test patterns.

1.INTRODUTION

Now a days many circuits include on chip structures that enable self testing known BIST. The power dissipation during the test mode 200% more than in normal mode. hence it is an important aspect to optimize the power during testing. The main sources of power dissipation in CMOS devices are summarized by the following expression

$$P = 0.5.C.V_{DD}^2.f.N+Q_{SC}.V_{DD}.f.N+I_{leak}.V_{DD}\ldots eqn(1)$$

Where, p denotes the total power, v_{dd} is the supply voltage and f is the frequency of operation.

The first term in equation(1) corresponds to the power involved in charging and discharging circuit nodes. C represents the node capacitance and N is the swiching activity i.e., the number of gate output transitions per clock cycle(also known as transition density)is the energy involved in charging or discharging a circuit with node capacitance C and is the average number of times per second that the node switches.

The second term in (1) represents the power dissipation due to current flowing directly from the supply to ground. During this period that the pull-up and pull-down networks of the CMOS gate are both conducting when the output switches. This

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current is often called short circuit current. The factor represents the quantity of charge carried by the short circuit current per transition.

The third term in (1) is related to the static power dissipation due to leakage current. The transistor source and drain diffusions in a MOS device from parasitic diodes with bulk regions. Reverse bias current in these diodes dissipate power. These 3 factors for power dissipation are often referred to as dynamic power, short-circuit power and leakage current power respectively. It has been shown[2] that during normal operation of well designed CMOS circuits the switching activity power accounts for over 90% of total power dissipation. Thus power optimization techniques at different levels of abstraction targets minimal switching activity power. In equation(1), the power dissipation can be reduced if we reduce the supply voltage or clock frequency. But this will degrade the performance of the system. C is the function of process technology and therefore not under the control of designer. So the power dissipation is directly proportional to the switching activity.

The reasons for increased power in test mode are:

1) To test the large circuit, the circuits are partitioned to save the test time, but the parallel testing results in excessive energy and power dissipation.

2) Due to lack of at speed equipment availability, the delay is introduced in the circuit during testing. This will cause the power dissipation.

Due to lack of correlation between the successive patterns, there exist a large

2.ARCHITECTURE OF BIST CONTROLLER

A typical BIST architecture consists of

- TPG - Test Pattern Generator
- TRA – Test Response Analyzer
- Control Unit
- MISR-Multiple input signature register
- Circuit under test

As shown in figure below.

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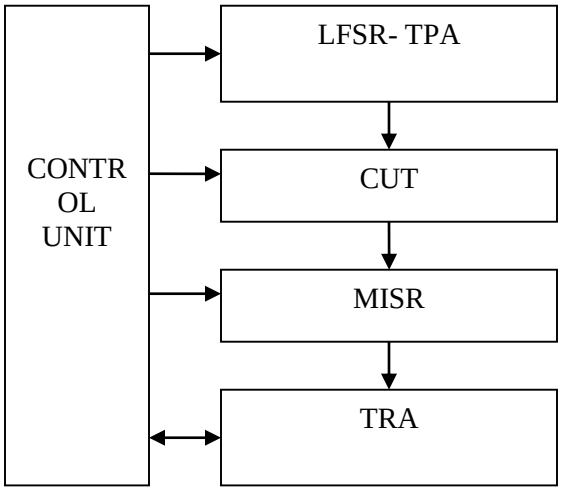

Fig 1: BIST Architecture

A built-in self test (BIST) circuit using a linear feedback shift register (LFSR) and a multiple input signature register (MISR) requiring reduced circuitry exclusive of the number of inputs and outputs of the circuit to be tested. The BIST circuit is built in a prescribed circuit having a memory to test a target circuit in the prescribed circuit. The BIST circuit includes an LFSR, including a first logic section which is composed of a plurality of XOR gates and selection sections, and a first memory which is a part of the memory, for performing a primitive polynomial, an MISR, including a second logic section which is composed of a plurality of XOR gates and selection sections, and a second memory which is a part of the memory, for performing the primitive polynomial, and a BIST control section for controlling data input/output between the first and second memories and the target circuit and providing selection signals for controlling the selection sections in the first and second logic sections, the BIST control section controlling the target circuit and comparing operation results of the target circuit to perform the test of the target circuit.

2.1 Test Pattern Generator

It generates test pattern for CUT. It will be dedicated circuit or a micro processor. Pattern generated may be pseudo random numbers or deterministic sequence. Here we are using a Linear Feed back Shift Register for generating random number. The Architecture for LFSR is as shown below.

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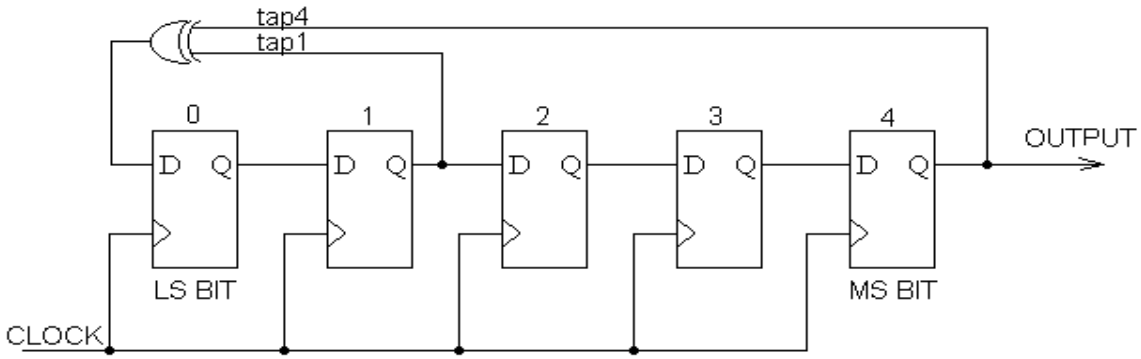

Fig 2: LFSR architecture

Tapping can be taken as we wish but as per taping change the LFSR output generate will change & as we change in no of flip-flop the probability of repetition of random number will reduce. The initial value loading to the LFSR is known as seed value.

2.2 Multiple Input Signature Resisters (MISR)

Architecture of MISR is as shown below. The blue boxes are indicating D-Flip Flop.

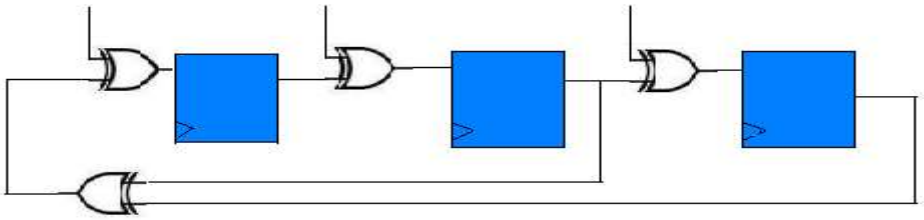

Fig 3: Architecture of MISR

In order to reduce the amount of hardware required to compress a multiple bit stream, a multiple input signature analysis register can be used. The theory presented in the literature shows that the functionality in terms of aliasing probability is unchanged for this implementation. A multiple input signature register (MISR) adapted to test a target circuit, said target circuit having a data bus coupled to a plurality of memory cells, the MISR comprising:

A plurality of storage elements, each of said elements being adapted to store a respective one coefficient of a primitive polynomial resulting from a pseudo-random signal. A plurality of exclusive-OR gates (XORs), each of said gates being adapted to generate XOR-gated values responsive to an output read out from a respective one of the plurality of storage elements, primitive polynomial data read out

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from the memory cells of the target circuit, and data supplied to the plurality of gates in parallel.

3.RESULTS AND DISCUSSIONS

3.1 Top module

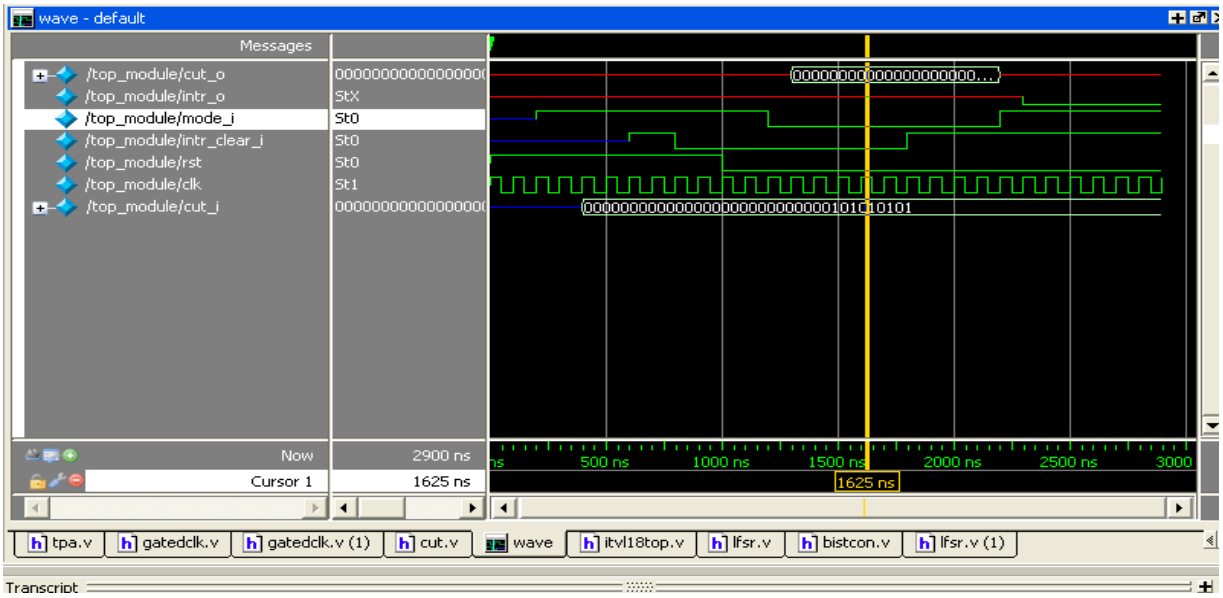

Fig 4: Simulation results of top module

3.2 XOR-LFSR

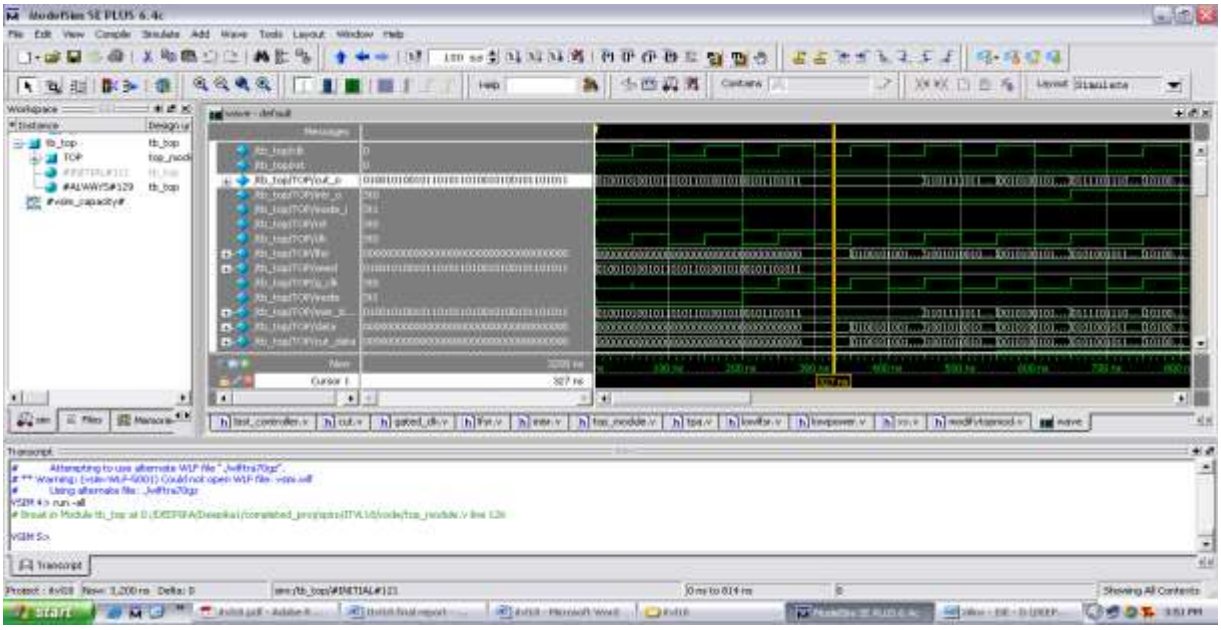

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Fig 5: Simulation results of XOR-LFSR

3.3 Low Power -LFSR

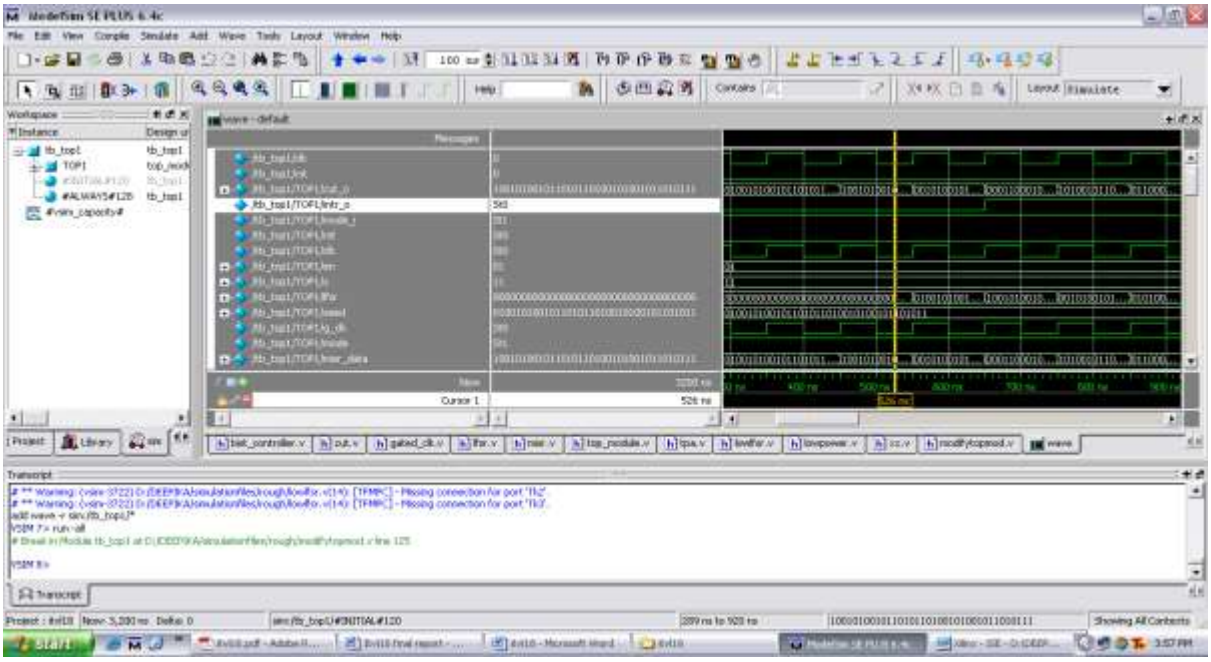

Fig 6: simulation results of low power LFSR

3.4 MISR

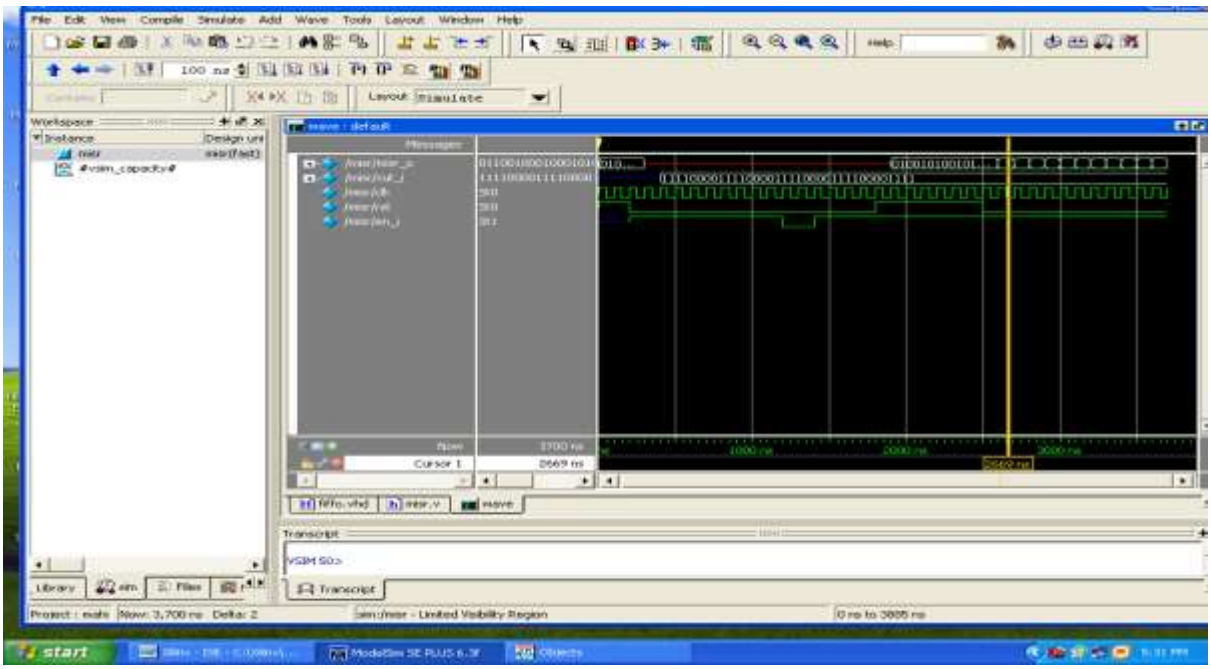

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Fig 7: Simulation results of MISR

3.5 Test Pattern Analyzer

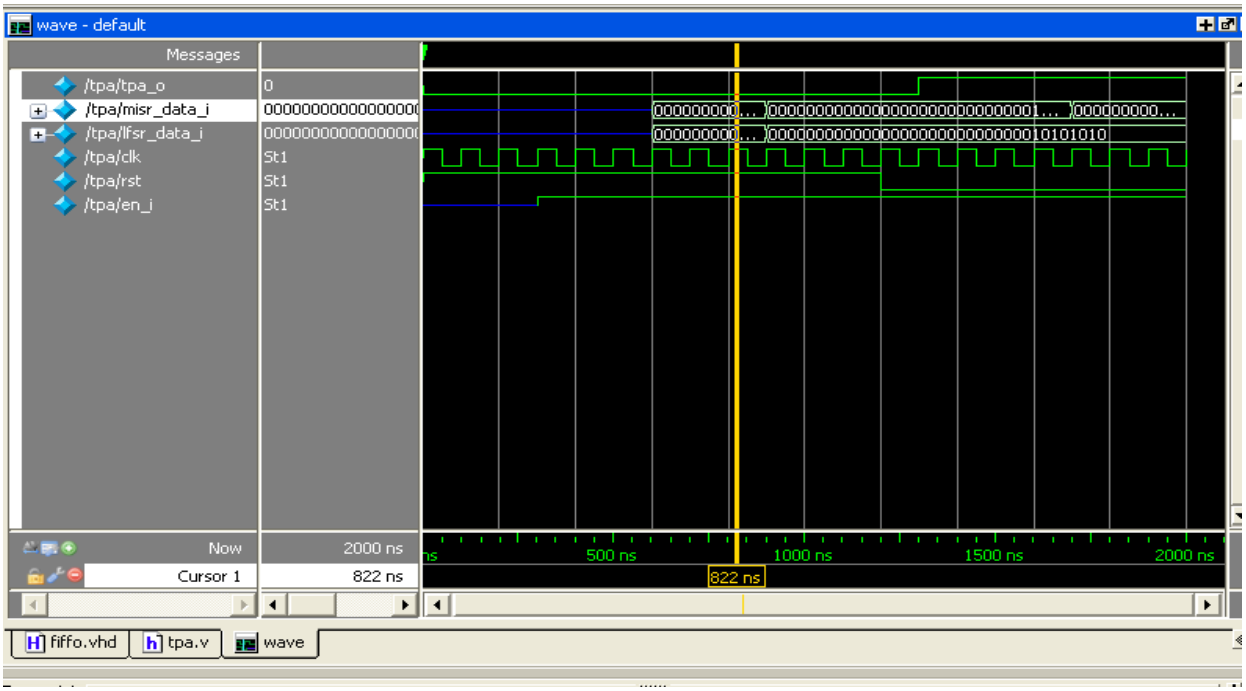

Fig 8: Simulation results of TPA

3.6 Gated Clock

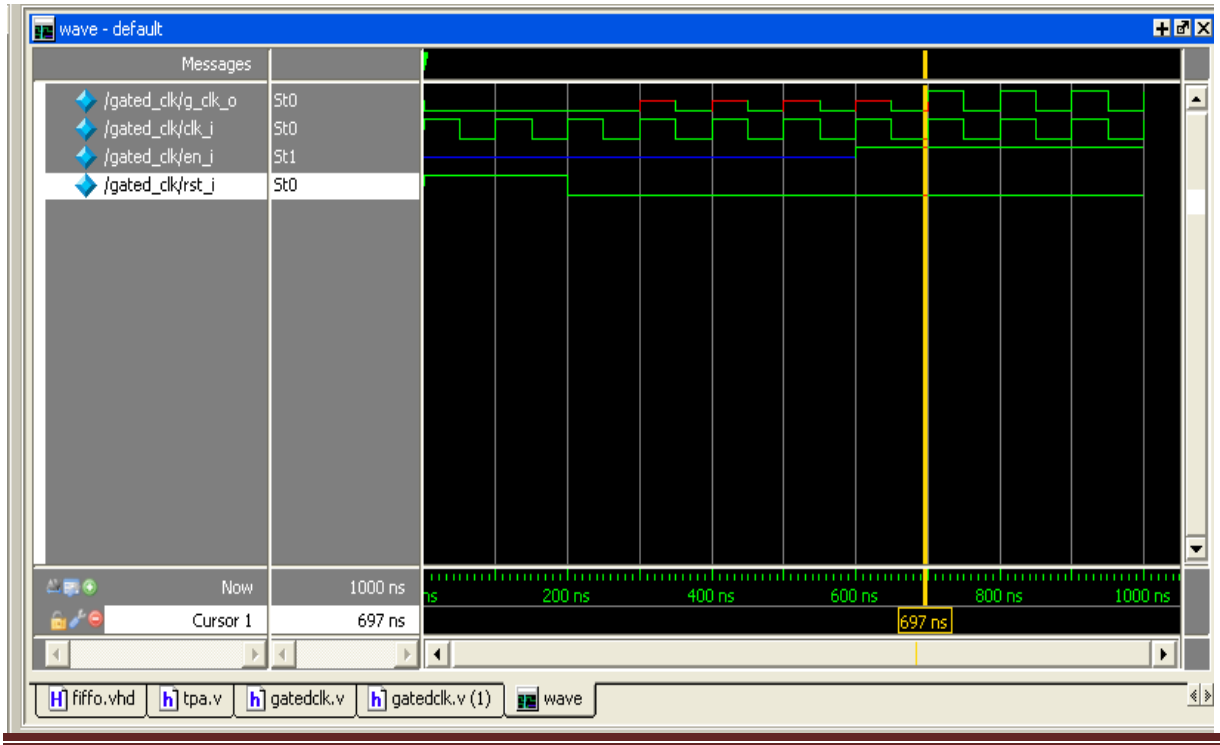

Fig 9: Simulation results of Gated Clock

4.CONCLUSION

The results obtained from the Xilinx 9.1 implementation with the device xc3s200-4pq208 in which, we have generated VCD file after the post simulation. X power is used to calculate the with the simulation files. Results are obtained for each case and comparison of power dissipation is made on the basis of reports. It is observed that the that the total power consumed in modified LFSR is 46% less than the power consumed with normal LFSR and output dynamic power is decreased by 44.6 %. It is concluded that low power LFSR is very useful for BIST implementation in which the CUT may be Combinational, sequential and memory circuits.

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