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An High Efficient Transformer less MOSFET Inverter for a Grid-Tied Photovoltaic System

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ABSTRACT

The unipolar sinusoidal heartbeat width adjustment full-connect transformer less photovoltaic (PV) inverter can accomplish high productivity by utilizing most recent super intersection metal–oxide–semiconductor field-impact transistor (MOSFET) together with silicon carbide (Sic) diodes. In any case, the MOSFETs are restricted to use in transformer less PV inverter because of the low turn around recuperation attributes of the body diode. In this task, a group of new transformers less PV inverter topology for a solitary stage network tied activity is proposed utilizing super intersection MOSFETs and Sic diodes as no turn around recuperation issues are required for the fundamental power switches for solidarity control activity. The additional clipping branch braces the freewheeling voltage at the half of dc input voltage during the freewheeling time frame. Thus, the regular mode voltage kept consistent during the entire matrix time frame that diminishes the spillage current essentially. What's more, dead time isn't essential for fundamental power switches at both the high-recurrence substitution and the framework zero intersection moment, results low-current bending at yield.

1. INTRODUCTION

The interest in renewable-energy sources is successively increasing because of rising demand of the world's energy and increasing price of the other energy sources, together with considering the environmental pollution. Many renewable energy sources are now available; among them, PV is the most up-to-date technique to address the energy problems. Due to the large-scale manufacturing capability of the PV module, it is becoming increasingly cheaper during these last years. So, the attempt to decrease the total grid-tied PV system cost is mostly depend on the price of grid-tied inverter [1-3]. Grid-tied PV inverters which consists a line frequency transformer are large in size, make the entire system extensive and difficult to install. It is also a challenging task to increase the efficiency and reduce the cost by using high frequency transformer which requires several power stages [4, 5]. On the other hand, transformer-less grid-tied inverters have the benefits of lower cost, higher efficiency, smaller size, and weight [6-12]. However, there exist a galvanic connection between the power grid and the PV module due to the exclusion of transformer which form a CM leakage current. This CM leakage current increases the grid current harmonics and system losses and also creates strong conducted and radiated electromagnetic interference [13-15].

In order to minimize the CM leakage current of the transformer-less grid-tied PV inverters, depth research have been pursued by many researchers of different countries [6-11, 13, 16-19]. Most of the inverters described in literature and commercially available show the European Union (EU) efficiency in the range of 96%-98% [16]. Hence, to improve the efficiency of the transformer-less inverters, several topologies by using MOSFETs as main switches have been proposed in [16, 20]. Super-junction MOSFETs can escape the fixed voltage drop and turn-off losses caused by tail current. Yu et al. proposed a H6_type MOSFET inverter by removing the use of low proficient IGBTs as shown in Fig. 1(a) [20]. The indicated peak and EU efficiencies of H6_type inverter on 300W prototype circuit with 180V DC bus voltage and 30 kHz operating frequency were 98.3% and 98.1%, respectively. In active mode of H6_type MOSFET inverter, the grid current flows through three switches, as a result, higher conduction losses still remain. Another difficulty is that the anti-parallel diodes of MOSFETs will be activated if a phase shift is occurred in the inverter output voltage and current. Accordingly, the dependability of the system is reduced because of MOSFET anti-parallel diode reverse recovery issues. GU et al. proposed high reliability and

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efficiency (HRE) MOSFET inverter shown in Fig. 1(b) [16]. HRE topology splits the ac sides into two independent parts in the positive and negative half cycle of grid current if compared with HERIC topology. The reported maximum and California energy commission (CEC) efficiencies of the HRE inverter on a 5kw prototype circuit with 20 kHz switching.

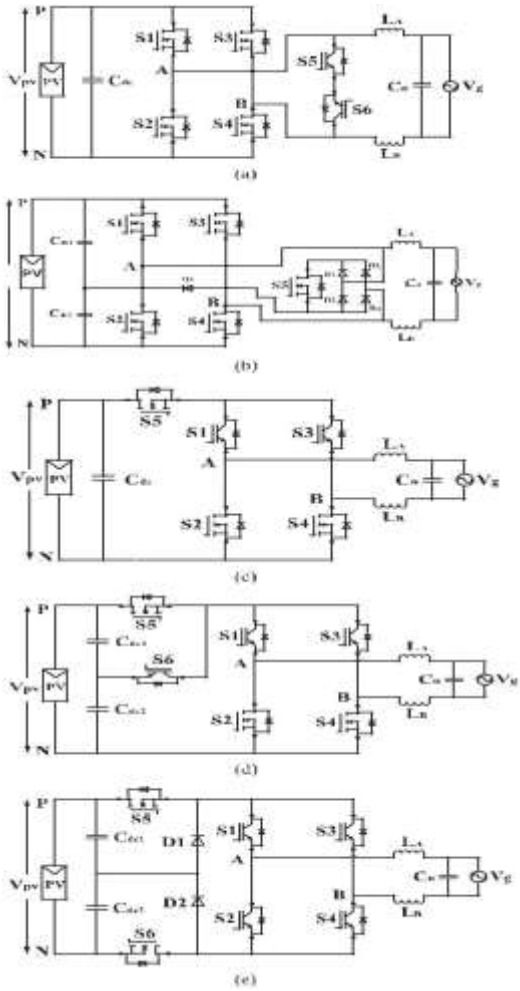

Fig. 1. Some existing MOSFET-based transformer less topologies for grid-tied PV application: (a) HERIC topology proposed in [26]. (b) HB-ZVR topology proposed in [10]. (c) H5 topology proposed in [27]. (d) oH5 topology proposed in [9]. (e) H6 topology proposed in [16].

grid current flows through two switches during the whole grid period; as a result, conduction loss is low.

Fig. 1(c) shows another explicit transformer less topology pro-posed in [27] called H5 topology, made up by adding an extra switch in the dc side of an FB inverter. In this topology, the freewheeling current flows through S_1 and body diode of S_3

during positive half cycle, and S_3 and body diode of S_1 during negative half cycle. As a result, the switches S_1 and S_3 could not be implemented with MOSFETs due to the low reverse re-covary of the MOSFET body diode. Another disadvantage is that the output current flows through three switches in the ac-time mode for the complete grid cycle, thus higher conduction losses are present. A fluctuating CM voltage could also be ob.-served because the freewheeling path potential is not clamped at the midpoint of dc link. An extension of H5 topology is pre-sented in [9] called optimized H5 (oH5) topology, where an extra switch (S_6) has been added with the H5 topology to clamp the CM voltage at the half of input voltage as demonstrated in Fig. 1(d). Unfortunately, a dead time must have to be added between the gate signals of the switches S_5 and S_6 to avoid the short-circuit of the input split capacitor $C_{d\,c1}$. As a result, CM voltage fluctuates in dead time [9]. Another disadvantage of this topology is that higher conduction losses still remain due to the grid current flows through three switches in the active mode. Gonzalez *et al.* proposed another topology in [16] called full-bridge with dc bypass which is also named as H6 topology. It employs two switches and two diodes in the dc side of FB inverter. The CM characteristics of this topology are better than other topologies because of the bidirectional clamping branch. During freewheeling mode, either diode D_1 or D_2 can be conducted based on whether the freewheeling path potential ($V_{A\,N} \approx V_{B\,N}$) is higher or lower than half of the dc-link volt-age. In this topology, leakage current removal effect depends only on the turn-on speed of the clamping diodes. However, this topology can be implemented with two MOSFET switches (S_5 and S_6) only. In addition, the grid current flows through four switches, thus higher conduction losses are also present. Considering the advantages and the drawbacks of the trans-former less inverter mentioned earlier, a family of new trans-former less topologies for a single-phase grid-tied PV system is proposed based on two asymmetric phase legs in this paper. The key

features of the proposed inverter are: 1) no dead time is required because the switches in the same phase leg are never all turned-on during the same SPWM cycle; as a result, current distortion at output is lower, 2) the CM voltage is kept constant at half of the dc input voltage because of the added clamping branch, and 3) during the positive and negative half cycle, the inductor current flows through two and three switches, respectively, thus the conduction loss is lower. The detailed operation principles and the control scheme to reduce the dc current in-ejection are described in this paper. An investigation has been conducted to calculate the device power losses and to make a detail comparison with the topologies presented in Fig. 1. Fi-Nally, the experimental results validate the proposed topology. At last, a comparison table has been summarized based on the experimental data to show the effectiveness of the proposed topology.

2. PROPOSED SYSTEM AND CONTROL DESIGN

A. Derivation Method of the Proposed Topology

The traditional MOSFET-based phase legs of transformer less inverter is shown in Fig. 2.2(a) and (b). In order to ensure high efficiency, a modification is made in Fig. 2.2(a) and (b) by replacing IGBTs with MOSFETs and diodes which is shown in Fig. 2.2(c) and (d). By combining these two-phase legs, a family of new transformer less topologies are derived based on the ac decoupling and asymmetric phase legs. The followings are the derivation steps of the proposed new topologies: 1) first, IGBT switches of the HERIC and H5 methods are replaced with MOSFETs and diodes to boost the efficiency; 2) next, combine these two- phase legs to derive new topology. By changing the position of the freewheeling switches (S3 and D1), the family of the new topologies is derived; 3) finally, to clamp the CM voltage at the half of the dc input voltage, a clamping branch consisting of a switch and a diode with a capacitor divider is introduced.

B. Circuit Configuration The family of the proposed transformer less PV inverter topology is depicted in Fig. 2.2 which is derived according to the derivation method described in the prior section, where S1, S2, S4, and S5 are high-frequency switches, and S3 and S6 are low frequency freewheeling switches. The unidirectional clamping branch is constructed using switch S7 and diode D3 with a capacitor divider (Cdc1 and Cdc2) which clamps the CM voltage at the midpoint of dc link. LA, LB, and Co make up the LC-type filter connected to the grid and Vpv represent the input dc voltage. The unipolar SPWM can be employed to the proposed topology with three-level output voltage. The MOSFET power switches are utilized as no reverse-recovery issues are required for the proposed configuration of the inverter for unity power factor operation. Consequently, the efficiency of the entire PV system is increased.

C. Operating Principle In order to analysis and verify, the circuit structure A is taken as an example. Fig. 2.1 shows the switching pattern for unity power factor operation, where the G1, G2, G3, G4, G5, G6, and G7 are the gate signals of the switches S1, S2, S3, S4, S5, S6, and S7. As can be seen S1, S4 and S2, S5 commutate at the switching frequency with the identical commutation order in the positive and negative half cycle of the grid current, respectively. In Fig. 2.2, the operating principles of the proposed topology are shown. Four operation modes are proposed to generate the output voltage state of +VPV,0, and −VPV, which can be explained as follows. 1) Mode 1 is the active mode in the positive half cycle of the grid current. When S1 and S4 are turned-on, the inductor current iL increases linearly through grid. In this mode, VAN = VPV and VBN = 0, thus VAB = VPV and the inductor current iL (t) = VPV − vg L (t). (1) 2) Mode 2 is the freewheeling mode in the positive half cycle of the grid current, as indicated in Fig. 5(b). The inductor current iL flows through S6 and D2, and reduces linearly under the effect of grid voltage. In this state, VAN falls and VBN rises until their values are equal. If the voltages (VAN ≈ VBN) are higher than half of the dc-link voltage, freewheeling current flows through S7 and D3 to the midpoint of the dc link, results VAN and VBN are clamped at VPV /2. Therefore, at mode 2, VAN = VPV /2, VBN = VPV /2, the inverter output voltage VAB = 0 and the inductor current iL (t) =

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−vg L (t). (2) 3) Mode 3 is the active mode in the negative half cycle of grid current. Similar to mode 1, when S2, S3, and S5 are turned on, the inductor current increases in the opposite direction. In this mode, the voltage VAN = 0 and VBN = VPV, thus VAB = −VPV and the inductor current iL (t) = VPV − vg L (t). (3) 4) Mode 4 is the freewheeling mode in the negative half cycle of grid current. When S5 and S2 are turned-off, the inductor current flows through S3 and D1. Similar to mode 2, if the voltages (VAN ≈ VBN) are higher than half of the dc-link voltage, freewheeling current flows through S7 and D3 to the midpoint of the dc link, results the voltages VAN and VBN are clamped at VPV /2. Therefore, in this mode, VAN = VBN = VPV /2, VAB = 0, and the inductor current iL (t) = −vg L (t). (4) As described above, the freewheeling path potential is clamped at the midpoint of the dc link during freewheeling period of positive and negative half cycle. As a result, the inverter hardly generates any leakage current. It can also be seen that the antiparallel diodes of the MOSFETs remained inactive during the whole

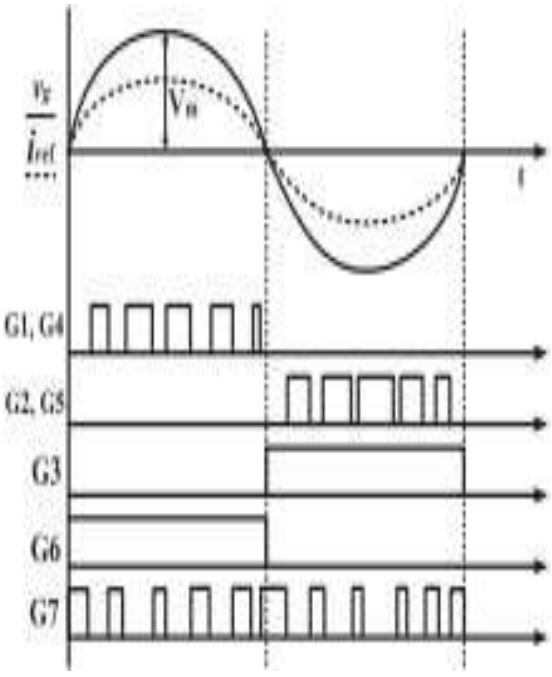
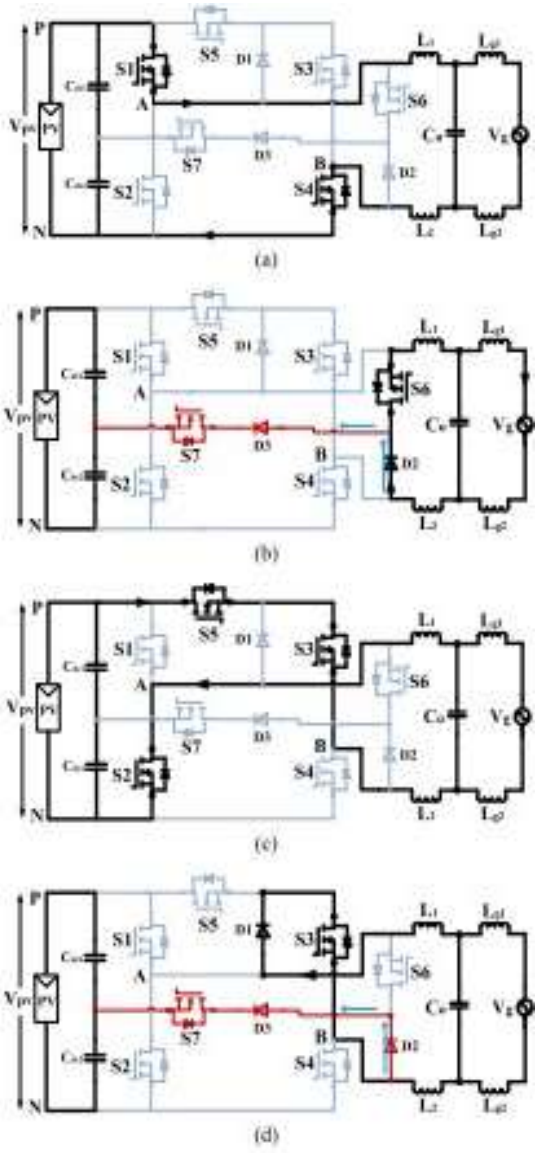


Fig 2.1: Gate drive signals of the proposed topology for the circuit structure A.



operation period. Therefore, the proposed topology could be implemented utilizing MOSFET switches. However, the body diode will be activated if a phase shift is occurred in the inverter output voltage and current. Accordingly, the dependability of the system will be reduced because of the MOSFET antiparallel diode low reverse-recovery issues.

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Fig 2.2: Operating principle of the proposed topology: (a) Active and (b) Freewheeling modes in the positive half cycle of the grid current. (c) Active and (d) freewheeling modes in the negative half cycle of the grid current.

3.SIMULATION MODE AND RESULTS

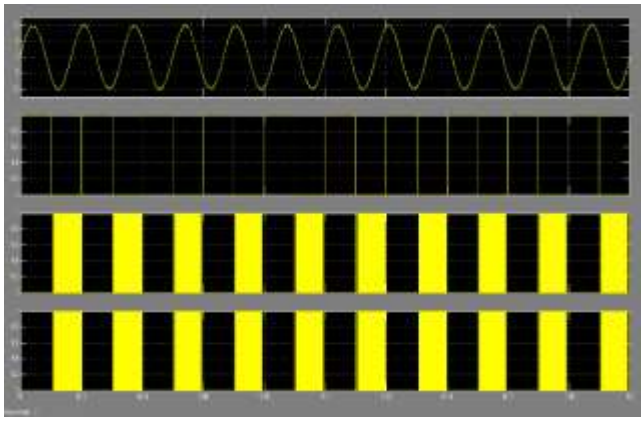

Fig 3.1 shows the simulation model of proposed circuit for the MOSFET Inverter system for a grid tied PV system to verify the proposed system by using MATLAB SIMULINK has been carried out, it has input, CM voltage, converter, control blocks low pass filter and output.

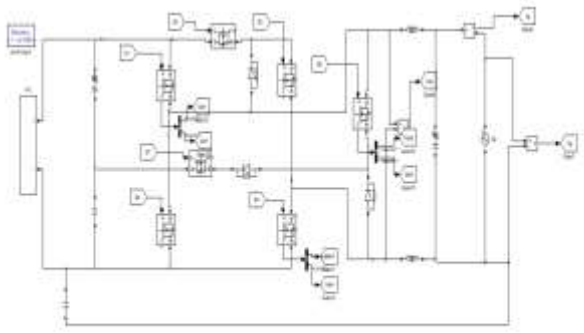

Fig 3.1 Proposed circuit for the MOSFET inverter system for a grid tied PV system with S_1, S_4 are ON.

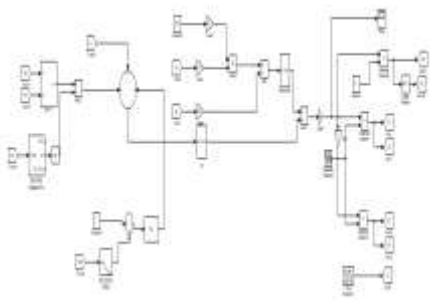

Fig 3.1.1 Control diagram for proposed system.

As shows above Fig 3.1.1 the control block and it has dc suppression loop, a grid current controller and a phase locked loop to synchronize with the grid current. The dc suppression loop is composed of a differential amplifier.

Fig 3.1.a Drain source voltage waveform of the switches S_1, S_4 and S_6.

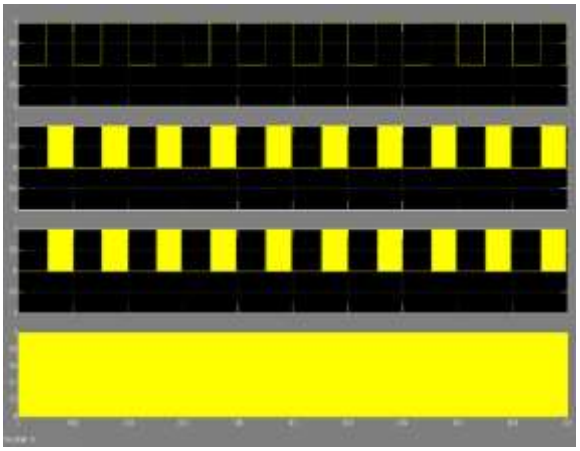

Fig 3.1.b Gate pulses for switching S_1, S_4, S_6 and S_7 switches.

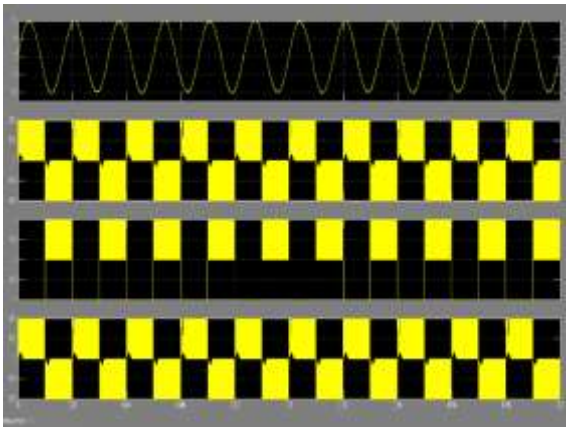

Fig 3.1.c Drain source S_1, S_4 and S_6 switches.

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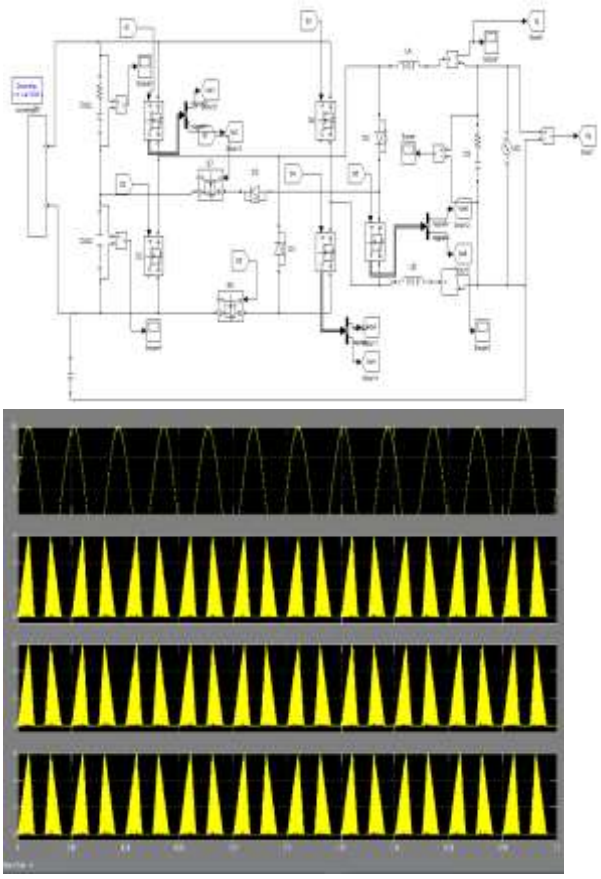


Fig 3.1.d current switches S_1, S_4 and S_6 switches.

As shows Fig 3.2 the simulation model of proposed circuit for the MOSFET Inverter system for a grid tied PV system to verify the proposed system by using MATLAB SIMULINK has been carried out, it has input, CM voltage, converter, control blocks low pass filter and output.

Fig 3.2 Proposed circuit for a grid tied PV system with S_6, S_7 are ON.

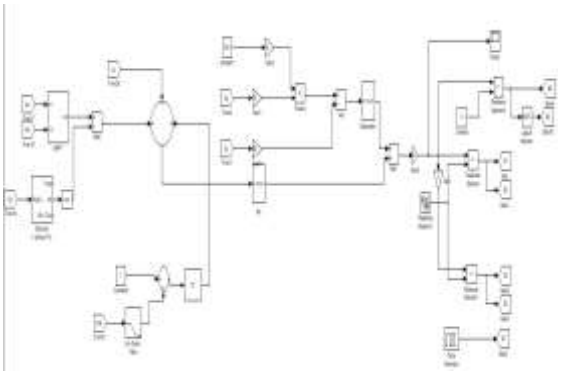
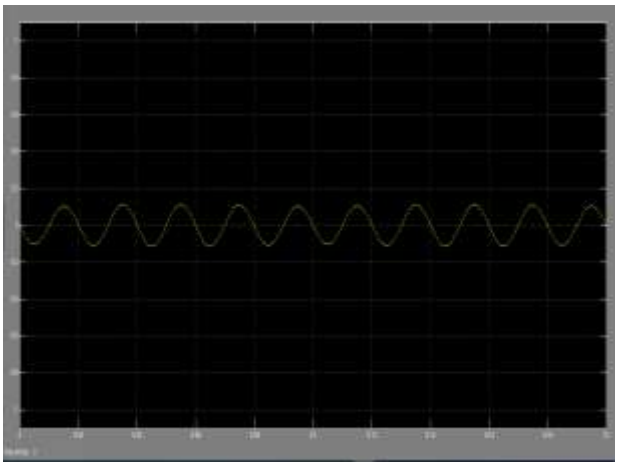


Fig 3.2.1 Control diagram for proposed system.

As shows above Fig 3.2.1 the control



block and it has dc suppression loop, a grid current controller and a phase locked loop to synchronize with the grid current. The dc suppression loop is composed of a differential amplifier.

Fig 3.2.a Current stress on the switches S_2, S_3 and S_5.

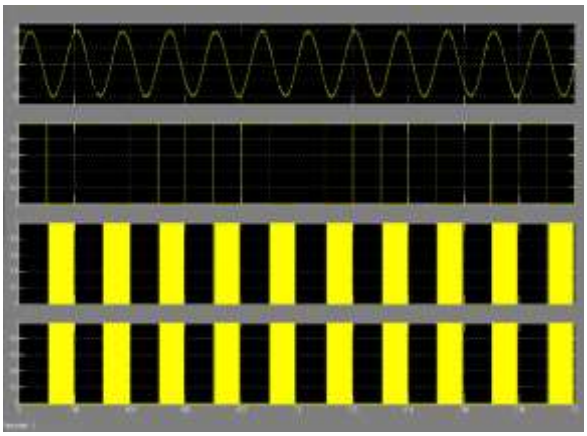


Fig 3.2.b Drain source voltage waveform of the switches S_1, S_4 and S_6.

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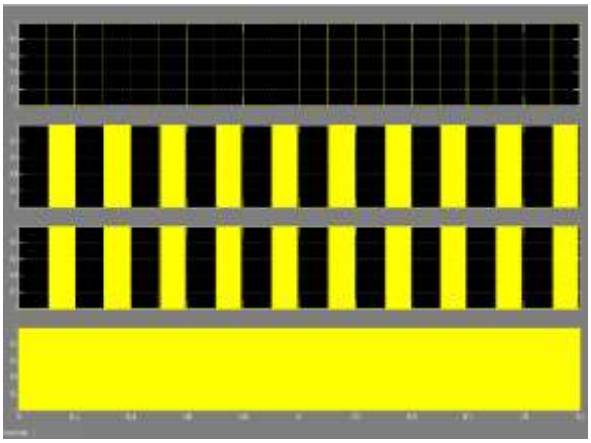


Fig 3.2.c Gate pulses for switching S_1, S_4, S_6 and S_7 switches.

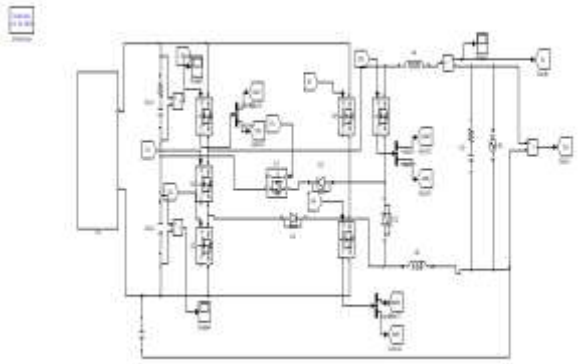
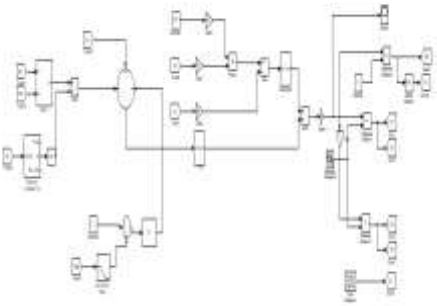


Fig 3.2.d Drain source S_1, S_4 and S_6 switches.



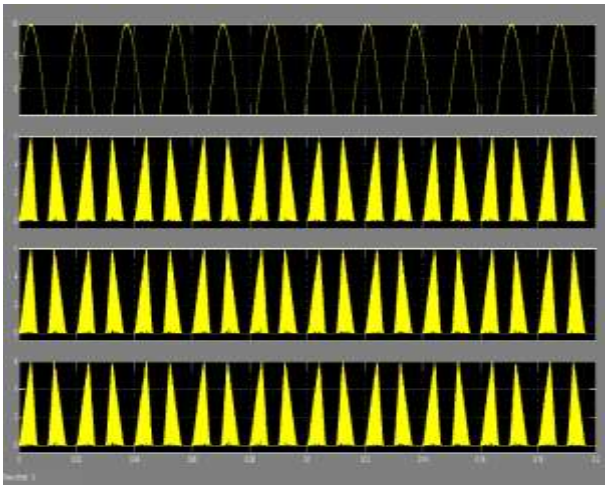
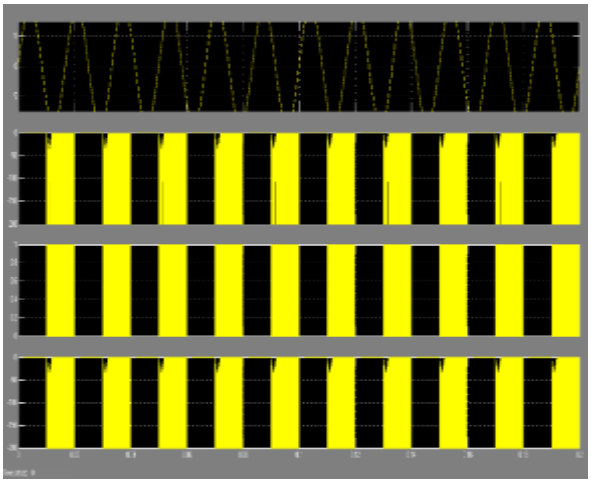


Fig 3.2.e current switches S_1, S_4 and S_6 switches.



As shows Fig 3.3 the simulation model of proposed circuit for the MOSFET Inverter system for a grid tied PV system to verify the proposed system by using MATLAB SIMULINK has been carried out, it has input, CM voltage, converter, control blocks low pass filter and output.

Fig 3.3 Proposed circuit for a grid tied PV system with S_2, S_3, S_5 are ON.

Fig 3.3.1 Control diagram for proposed system.

As shows above Fig 3.3.1 the control block and it has dc suppression loop, a grid current

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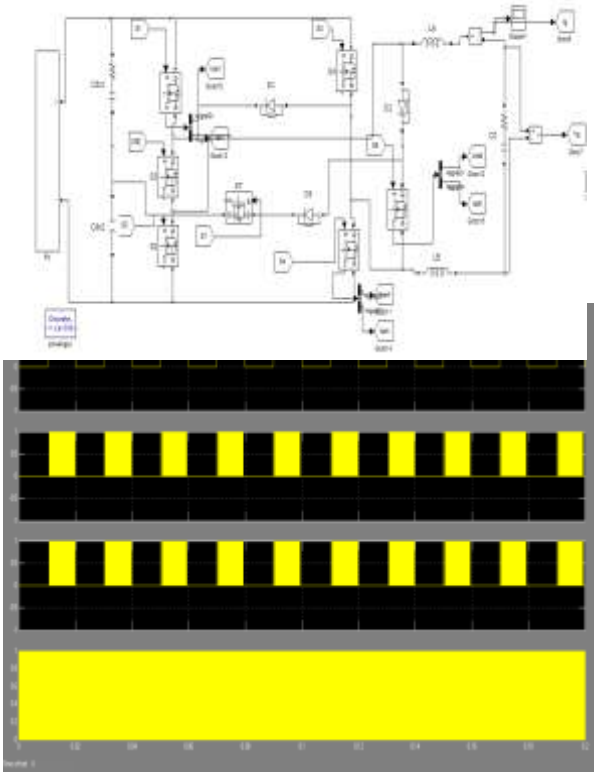
controller and a phase locked loop to synchronize with the grid current. The dc suppression loop is composed of a differential amplifier.



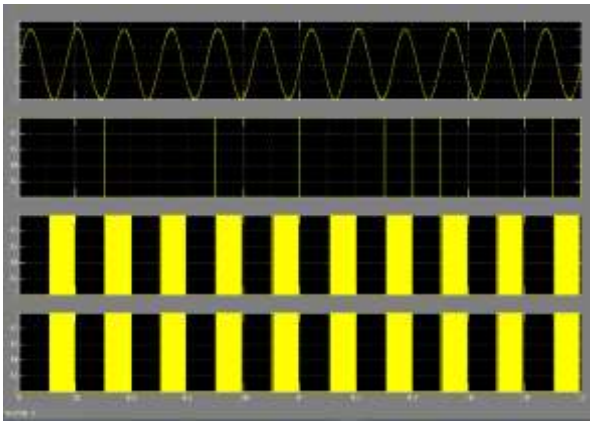


Fig 3.3.a Drain source voltage waveform of the and S_6 switches S_1, S_4.

Fig 3.3.b Gate pulses for switching S_1, S_4, S_6 and S_7 switches.

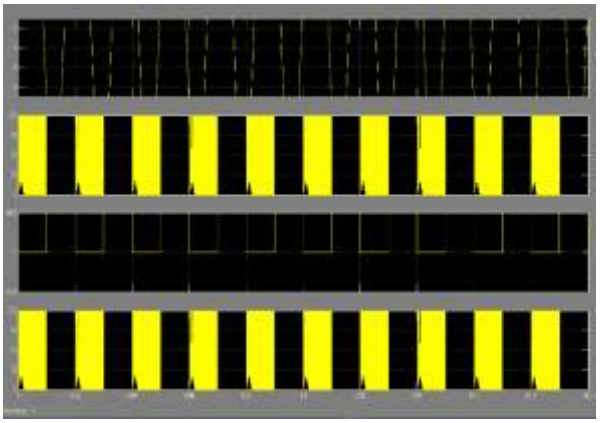


Fig 3.3.c Drain source S_1, S_4 and S_6 switches.

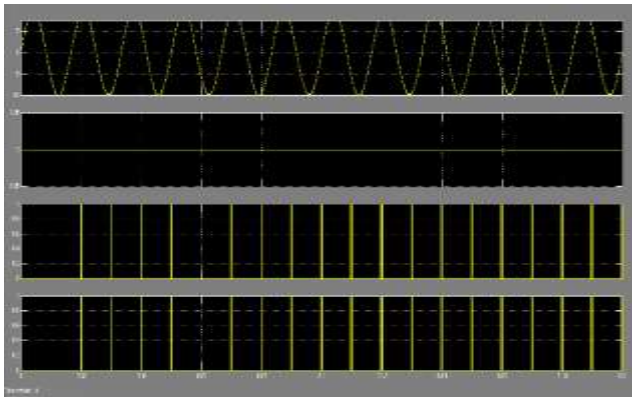


Fig 3.3.d current switches S_1, S_4 and S_6 switches.

As shows Fig 3.4 the simulation model of proposed circuit for the MOSFET Inverter system for a grid tied PV system to verify the proposed system by using MATLAB SIMULINK has been carried out, it has input, CM voltage, converter, control blocks low pass filter and output.

Fig 3.4 Proposed circuit for a grid tied PV system with S_3, S_7 are ON.

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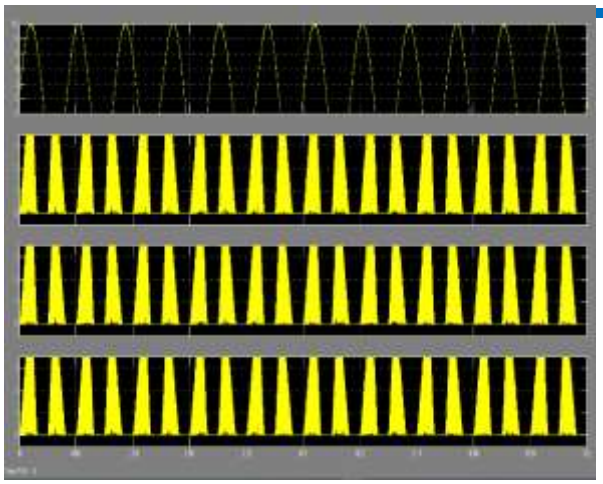

Fig 3.4.a Drain source voltage waveform of the switches S_1, S_4 and S_6.

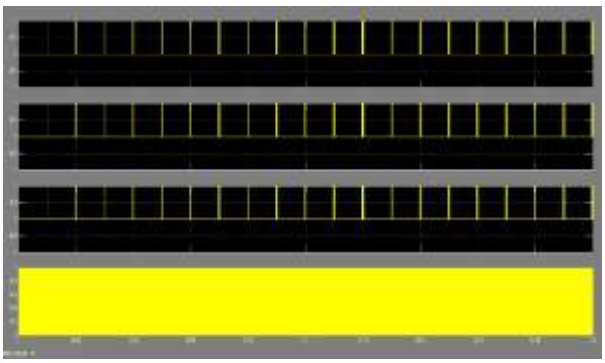

Fig 3.4.b Gate pulses for switching S_1, S_4, S_6 and S_7 switches.

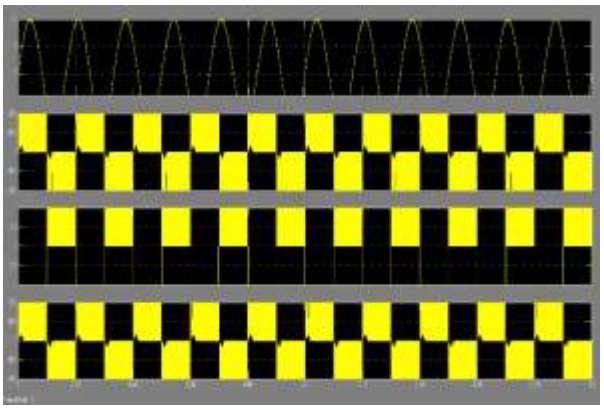

Fig 3.4.c Drain source S_1, S_4 and S_6 switches.

Fig 3.4.d current switches S_1, S_4 and S_6 switches.

4.CONCLUSION

This proposed efficient transformer less inverter for a grid tied PV Power generation system has the ability to achieve high efficiency by using super junction MOSFETs and Sic diodes .it can also reduce the leakage current.it also can reduce conduction and switching losses by using superfunction MOSFETs.the main advantages of proposed system are CM voltage remains constant during all operating modes, it has having excellent DM characteristics and PWM deadtime is not required for main switches, results low distortion at output. By using proposed system, we can achieve 240V/50Hz,1KW, then the efficiency is more than 98.32%. therefore, the proposed system is very suitable for a single-phase grid connected PV system.

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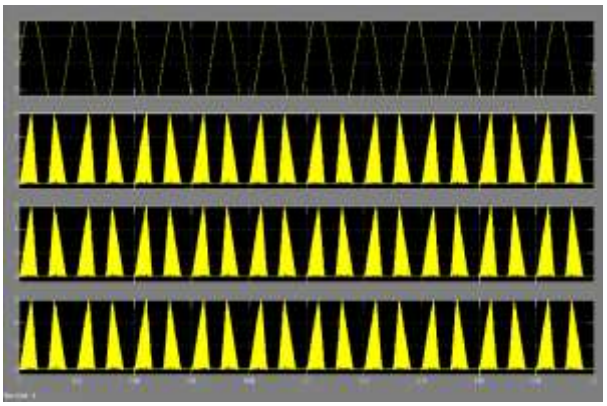

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