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# Power Factor Correction in Modified SEPIC Converter fed Switched Reluctance Motor Drive

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**ABSTRACT**
This paper presents a dual output PFC (Power Factor Correction) converter for switched reluctance motor (SRM) drive. Here, a modified SEPIC (Single Ended Primary Inductance Converter) converter is proposed for wide range of speed control and to achieve power factor correction at AC mains. The switching frequency of the converter is considered at 20 kHz. The converter is designed to operate in DCM (Discontinuous Conduction Mode) of operation, which reduces the size of the output inductor. The DCM mode to obtain PFC, also reduces the sensor requirement as compared to CCM where two voltage sensors and one current sensor, add to the drive cost. The drive is proposed for universal AC mains (90V-270V AC). Simulated and experimental results are demonstrated to validate the performance of the drive during different operating conditions. The input current total harmonic distortion (THD) is reduced to comply an IEC 61000-3-2 standard.

**Keywords:- Reluctance motors, Inductors, Capacitors, Switches, Voltage control, Semiconductor diodes**

## INTRODUCTION

Switched reluctance motor (SRM) drives are becoming popular due to their simple structure and low cost. High efficiency over wide speed range, absence of any sort of magnet, winding free rotor and no brushes, make SRM superior to permanent magnet brushless DC motor and induction motor drives. However, a SRM drive requires a power converter, controller for generating switching pulses and position sensor to sense exact rotor position, which is used to excite sequentially the phases of SRM [1-7]. Usually physical position sensor on the shaft, senses the rotor position, which adds to cost and size to the SRM drive. Thus to reduce cost and size of the motor, various sensorless position estimation methods have also been investigated and reported in the literature. These are active phase current detection method, EMF method, impedance sensing method, inductance slope based, Kalman filter based and pulse signal injection based methods [8-11].

Exciting one phase at any instant, is conventionally used to control the SRM. However, SRM with simultaneous conducting two phases at any given time, has also been explored in the literature to reduce the losses and torque ripple in SRM. Here a 8/6 pole, four phase SRM is considered, such that all the poles are always in torque producing region, therefore, to produce continuous torque, two phase windings allow to conduct at any instant [12]. Conventionally SRM drives are powered by AC mains using a diode bridge rectifier, which draws harmonics rich current. Therefore, poor power factor and high losses in SRM drive, are the challenging and concerned areas for research. Thus to improve power factor and to reduce input current THD (Total harmonic distortion) of the SRM drive, front

end PFC converters are recommended. Hence, a modified SEPIC (Single Ended Primary Inductance Converter) fed SRM drive with PFC, is proposed in this work. A mid-point converter, which utilizes a single switch and a single diode to excite individual phases, is selected here to build the proposed drive as a low cost system. This converter is well suited for inexpensive application due to reduced count of switches and drivers requirement. Moreover, switch voltage rating requirement is half because of its split DC configuration. The only drawback associated with this so far unpopular converter topology, is the required voltage symmetry. This encourages the design of a PFC converter, which can take care of power quality issues at AC mains and generates two symmetrical voltages across the capacitors. The converter with two output voltages and neutral points, is directly connected to the mid-point converter with neutral point N.

The PFC converters exhibit unity power factor operation, low input current THD and well regulated output voltages, which are further categorised as buck, boost and buck-boost converters on the basis of the output voltage requirement. Buck type PFC converters are required, where preferred output voltage is low [13], [14]. However, the discontinuous input current in buck converter results in requirement of a robust input passive filter. To resolve this problem, PFC boost converters are widely used with an advantage of reduced input current ripple but output voltage always higher than peak input voltage [15]. In these boost PFC converter circuits, input-output isolation cannot be implemented. Therefore, PFC buck-boost converters are preferred over buck and boost converters to resolve these problems, which can provide high power factor over a complete output voltage range. SEPIC and Cuk converters are widely used for PFC applications [16].

On the basis of the current nature through the inductor, three operating modes, are reported in the literature to obtain PFC, i.e., CCM (Continuous Conduction Mode), CRM (Critical Conduction Mode) and DCM (Discontinuous Conduction Mode) [17-19]. Low rms currents through the device and an inductor, add merit to CCM based control with reduced EMI (Electromagnetic Interference) issues. However, the switch always operates at hard switching and the diode suffers from reverse recovery. Two voltage sensors and one current sensor, are required in this PFC approach.

The advantages of CRM over CCM, includes zero current turn on of switch and no reverse recovery of the diode. The demerits associated with CRM, are the operation at variable switching frequency at different input voltages and load conditions, thus noise spectrum is continuous and varies in a complicated manner. Therefore, the design of EMI filter is an issue as per the given electromagnetic compatibility (EMC) standard limits. However, same number of voltage and current sensors, are required in CRM as compared to CCM.

Whereas, DCM provides soft switching with no diode reverse recovery current same as CRM based scheme. To ensure discontinuous current through the inductor during different loading conditions and supply voltage variation, the inductor is selected of much lower value as compared to the calculated value. The control for the DCM of operation, requires just a voltage sensor to regulate the DC link voltage as per the output voltage requirement. However, the PFC is obtained due to discontinuous inductor current mode during each switching period. During this period, the circuit behaves as a emulated resistance, and thus inherent wave-shaping is provided to the circuit. Therefore, DCM of operation is selected here for proposed low cost and low power rating SRM drive for house hold

applications. Accomplishing the system requirement, the conventional SEPIC converter is modified while adding one extra diode and capacitor to the circuit. The key features associated with proposed converter topology, are as follows.

- Generating two symmetrical output voltages using only one voltage sensor.
- Eliminating additional voltage balancing loop.
- Unity or near to unity power factor.
- Low input AC mains current THD.
- High voltage gain.
- Reducing stress across semiconductor device due to presence of neutral point N.

## SEPIC CONVERTER

### Basic of Sepic Converter

The basic converter we see in our day to-day life is buck converter. It is so called, because it only step down the input voltage .the output is given by

$$V_o = DV_s \qquad (2.1)$$

Where $V_o$=output voltage

$V_{IN}$=input voltage

D=duty cycle

By interchanging input and output we get boost converter .which only step up voltage, hence its name boost. The output is always greater than input, but main problem is to get step up and step down voltage from a single device depending on output. We can use two cascaded converters (a buck and a boost).but for this two separate controller and separate switch are required. So it is not the good solution .Buck-boost converter can give required output but here output is inverting .These converters have more component stresses, component sizes and lesser efficiency. To reduce the losses caused by high voltages, a circuit with buck-boost conversion characteristics, small energy storage element required and smaller inductor size is desired .but inductor should not be so less ,such that ripple current is high.

Thus, the optimum converter however should have low component stresses, low energy storage requirements and size and efficiency performance comparable to the boost or the buck converter One converter that provided required output is the SEPIC (single ended primary inductor converter) converter. by varying duty cycle of gate signal of MOSFET we can vary the output. If duty cycle is greater than 50%, it will step up. so it is called as boost converter. if duty cycle is below 50% it will step down the voltage and it operate as buck converter. Another advantage of this converter is it provides a positive regulated output voltage from an input voltage that varies from above to below the output voltage. It function as both like a buck and boost converter, the SEPIC also has minimal active components, a simple controller that provide low noise operation.

## OPERATION OF MODIFIED SEPIC CONVERTER

The SRM drive with single switch SW1 is shown in Fig. 1. The converter comprises of two SEPIC converters operating for two half cycle of supply voltages, separately. This topology provides one common input and output inductor for two SEPIC converters [20]. However, input inductor ($L_i$) operates in CCM, whereas output inductor ($L_o$) is designed for DCM of operation. The converter operation can be explained under two half cycles of source voltages, separately. Two intermediate capacitors $C_1$ and $C_2$ operate in CCM such that $C_1$ conducts for one half while $C_2$ conducts for other half. Six operating modes of modified SEPIC converter are given as follows.

Mode I: This mode begins with every switch on period. However, the energy flow

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takes place from supply side to an input inductor ($L_i$) through diodes $D_1$, and $D_4$. The output inductor ($L_o$) starts storing energy through diode $D_6$. The intermediate capacitor $C_1$ is discharged whereas output capacitor $C_{dc2}$ is charged during this operating mode, which is shown in Fig. 2(a).

Mode II: The switch $S_{W1}$ is turned off as this mode begins, the circuit under this mode is given in Fig. 2 (b). The transfer of energy takes place from input side indutor $L_i$ to intermediate capacitor $C_1$ and DC link capacitor $C_{dc1}$ through diode $D_1$ and $D_5$ while the output side inductor $L_o$ energy transfers to DC link capacitor $C_{dc1}$ and $C_{dc2}$ through diodes $D_5$ and $D_6$.

Mode III: The current through output inductor ($L_o$) decreases to zero in this operating mode. The current flow during this operating mode, is given in Fig. 2(c). The capacitor $C_{dc2}$ is discharged across the load during this operating mode.

Mode IV: This mode starts with negative half cycle of the source voltage as shown in Fig. 2(d). During this mode, the source current finds its path through diode $D_2$, switch $S_{W1}$ and diode $D_3$. The intermediate capacitor $C_2$ is discharged across output inductor $L_o$. The DC link capacitor $C_{dc1}$ is charged during this mode while the other capacitor $C_{dc2}$ keeps on discharging across the load.

Mode V: This mode begins with switch off state of switch $S_{w1}$. The intermediate capacitor $C_2$ and DC link capacitor $C_{dc2}$ are charged during this mode of operation. The energy stored in output side inductor $L_o$ during previous mode, is transferred to DC link capacitors $C_{dc1}$ and $C_{dc2}$ through diodes $D_5$ and $D_6$, which is demonstrated in Fig. 2(e).

Mode VI: This mode begins as the output side inductor current $i_{Lo}$ becomes discontinuous. This mode is demonstrated in Fig. 2(f) and the related current through and voltage across waveforms across circuit components during each switching period are given in Figs. 2(g) and (h).

## DESIGN OF MODIFIED SEPIC CONVERTER

To investigate the performance of modified SEPIC converter fed SRM drive, a prototype is developed for a rated power of 400W. A DSP (DS1104), a real time controller with real time interface (RTI), is used to generate pulses for power converter to drive SRM and to switch the proposed modified SEPIC converter. The motor phases are provided with additional fuses for protection against high current.

The proposed drive is fed with an input voltage $v_s$, which is given as,

$$v_s = V_m \sin(2\pi f_L t) = 220\sqrt{2}\sin(314t)$$

However, $f_L$ denotes the line frequency and peak input voltage is given by $V_m$. The rectified output voltage $V_{in}$ is given as,

$$V_{in} = |V_m \sin(\omega t)| = |220\sqrt{2}\sin(314t)|$$

The voltage $V_{dc}$ of the SEPIC, is calculated as [21],

$$V_{dc} = \frac{D}{1-D} V_{in}$$

The maximum and minimum duty cycles when DC link voltage is varied from maximum to minimum values, can be obtained as,

$$D_{\max} = \frac{V_{dc\max}}{V_{dc\max} + V_{in}}, D_{\min} = \frac{V_{dc\min}}{V_{dc\min} + V_{in}}$$

An instantaneous power associated with the proposed drive at different DC link voltages, is considered as the linear function, which can be given as,

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$$P_i = (\frac{P_{max}}{V_{dc}})V_{dc}$$

Where $V_{dc}$ gives rated DC link voltage.

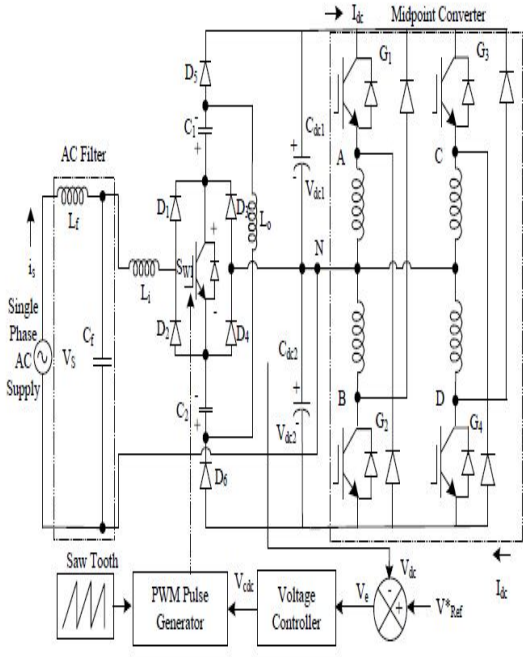


Fig. 1 Modified SEPIC converter fed SRM drive

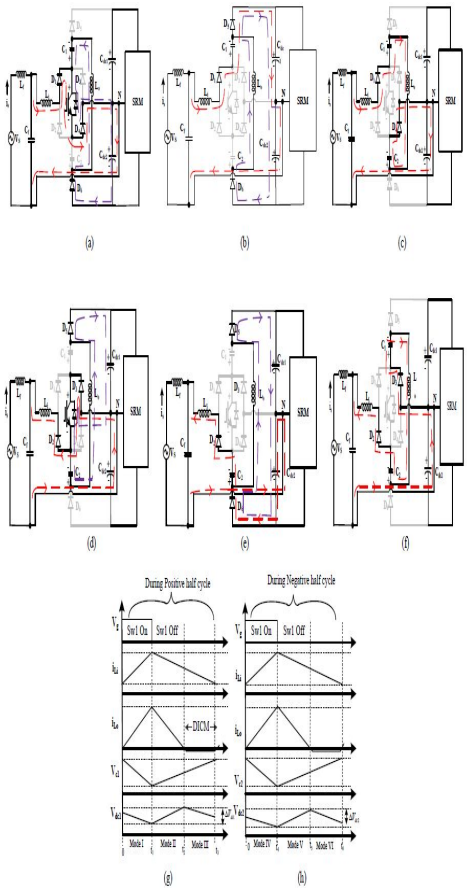

Fig. 2. DCM operation during (a, b, c) for positive half cycle, during (d, e, f) for negative half cycle and related waveforms (g) and (h) for each switching period during Modes I, II, III, IV, V and VI.

### A. Estimation of Input Inductor ($L_i$) for CCM

The design for Li is selected to operate in CCM mode, with permissible current ripple about 50%. Therefore, an expression for input inductor calculation is given as [22-23],

$$L_i = \frac{V_{in}D}{\eta I_{in} f_s} = \frac{R_{in}D}{\eta f_s} = \left(\frac{V_s^2}{P_i}\right)\frac{D}{\eta f_s}$$

$$= \frac{1}{\eta f_s}\left(\frac{V_s^2}{P_{max}}\right)\left(\frac{V_{dc\,max}}{V_{dc\,max}+V_{in}}\right)$$

In this expression, $I_{in}$ denotes input current, the equivalent input resistance is given by $R_{in}$ and converter switching frequency is given by $f_s$. However at rated condition $V_{dc}$=300V with input voltage as $V_{in} = \sqrt{2}V_s$, the value of input inductor is given as,

$$L_i = \frac{1}{0.5\times 20000}\left(\frac{220^2}{400}\right)\left(\frac{300}{300+220\sqrt{2}}\right) = 5.929mH$$

Hence, on the basis of above calculation for input inductor it is considered as 5.5mH

### B. Design of Output Inductor (Lo) for DCM

To obtain inherent PFC, the circuit is designed to operate in DCM during each switching period so that this circuit behaves as a resistor. Therefore, the design of the output inductor is selected to allow the inductor current to decrease below zero, which is given as [22-23],

$$L_o = \frac{V_{dc}(1-D)}{2I_{Lo}f_s} = \frac{V_{dc}D}{2I_{in}f_s} = \frac{R_{in}V_{dc}D}{2V_{in}f_s}$$

$$= \left(\frac{v_s^2}{P_i}\right)\frac{V_{dc}}{2V_{in}f_s}\left(\frac{V_{dc}}{v_{in}+V_{dc}}\right)$$

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$$L_o = \left(\frac{v_s^2}{P_{\max}}\right)\frac{V_{dc\max}}{2\sqrt{2}V_{s\min}f_s}\left(\frac{V_{dc\max}}{V_{dc\max}+\sqrt{2}v_s}\right)$$

$$L_0 = \left(\frac{220^2}{400}\right)\frac{300}{2\sqrt{2}\times220\times20000}\left(\frac{300}{300+220\sqrt{2}}\right) = 1429.23\mu H$$

To assure DCM of operation, an order of 1 / 10th of the inductor i.e. $200\mu H$ is considered as an output inductor [16].

### C. Intermediate Capacitors Design ($C_1$ and $C_2$)

The energy transfer from converter input to converter output, is supported by two intermediate capacitors $C_1$ and $C_2$, which are designed to operate in continuous voltage mode. Therefore, the design of capacitors is given as [24-27],

$$C_{1,2} = \frac{V_{dc}D}{\Delta V_{c1}f_sR_L} = \frac{V_{dc}D}{\Delta V_{c1}f_sR_L}$$

The voltage across both the capacitors, is given as, $V_{C(1,2)}(t)= \{V_{dc} + V_{in}\}$ and $R_L=V_{dc}^2/P_i$ . After substituting the value in (9) and rearranging, final expression for $C_{1,2}$ is written as,

$$C_{1,2} = \frac{V_{dc}}{\kappa\{V_{dc}+V_{in}\}f_s(V_{dc}^2/P_i)}\left(\frac{V_{dc}}{V_{in}+V_{dc}}\right) = \frac{P_{\max}}{\kappa(V_{dc\max}+\sqrt{2}v_s)^2f_s}$$

Therefore at $V_{dc}$ = 300 V the calculation for $C_1$ and $C_2$, is made for ripple voltage (κ) as 10%,

$$= \frac{400}{0.1\times20000\times\left(220\sqrt{2}+300\right)^2} = 535.52\text{nF}$$

Therefore $C_1$ and $C_2$, are considered as 690 nF.

### D. Output Capacitor Design

The value of converter output capacitor, is calculated while considering complete output voltage range as 100 V-300 V DC. For calculation the voltage ripple $(\delta)$ across output capacitor is considered as 3%. Therefore converter output capacitors are calculated as [24-28],

$$C_{DC} = \frac{I_{dc}}{2\omega\Delta V_{dc}} = \frac{P_i/V_{dc}}{2\omega\delta V_{dc}}$$

$$C_{100} = \frac{P_{\min}}{2\omega\delta V_{dc\min}^2} = \frac{155}{2\times314\times.03\times100^2} = 822.71\mu F$$

$$C_{300} = \frac{P_{\max}}{2\omega\delta V_{dc\max}^2} = \frac{400}{2\times314\times.03\times300^2} = 235.90\mu F$$

Therefore two series connected output capacitors, are selected as $C_{dc1}=C_{dc2}=1000\mu F$.

### E. Design of DC Filter ($L_f$ and $C_f$)

The input passive filter is designed to eliminate higher order switching harmonics generated by the converter switch operating at 20 kHz switching frequency. The calculation for filter capacitor $C_f$ is given as [24-28],

$$C_{f\max} = \frac{I_m}{\omega_L V_m}\tan(\theta) = \frac{\left(P_o\sqrt{2}/V_S\right)}{\omega_L V_m}\tan(\theta)$$

$$= \frac{400\sqrt{2}/220}{314\times220\sqrt{2}}\tan(0.5) = 229nF$$

Therefore, on the basis of the above calculation, the filter capacitor is selected of 330nF. Where $V_m$ and $I_m$ denote the supply voltage and current and $\omega_L$ denotes the line frequency. However, $\theta$ represents displacement between fundamental voltage and current. To calculate the value of $L_f$, the source inductance ($L_s$) is selected as 0.03 times the base impedance. Therefore, its calculation is given as,

$$L_f = L_{req} + L_s$$

$$\frac{1}{4\pi^2f_c^2C_f} = L_{req} + 0.03\left(\frac{1}{\omega_L}\right)\left(\frac{V_s^2}{P_i}\right)$$

$$L_{freq} = \frac{1}{4\pi^2\times2000^2\times470\times10^{-9}} - 0.03\left(\frac{1}{314}\right)\left(\frac{220^2}{400}\right) = 1.84\text{mH}$$

Where, $L_{req}$ is the additional value of inductance required. Hence, the selected value of filter inductor is used as 2mH.

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## CONTROL ALGORITHM

The DC link voltage is regulated by implementing variable duty cycle control to obtain speed control of SRM drive. The controlled duty cycle is obtained by comparing the sensed voltage signal with reference signal. The proposed buck-boost converter provides step up and down function thus, output voltage control over a wide range is obtained easily. The PFC operation is achieved by allowing converter to operate in DCM during each switching period. During DCM period, the circuit appears as emulated resistance thus improves the power quality of the system. The control method for the proposed drive, is explained as follows.

### A. Converter Control

To obtain well regulated output voltage under supply voltage variation and different loading conditions, a simple voltage mode control scheme is selected here. The controlled duty cycle provides the fully regulated DC voltage to feed power converter of SRM. The PI (Proportional Integral) controller is designed to track reference voltage ($v^*_{ref}$). However, voltage across the output capacitor ($V_{dc}$) is sensed using Hall-Effect based voltage sensor. If "p" is considered as sampling instant, therefore, comparator error output voltage ($v_e$), is as,

$$v_e(p) = v_{ref}^*(p) - v_{dc}(p)$$

Similarly, controlled output $v_{cdc}$, is as,

$$v_{cdc}(p) = v_{cdc}(p-1) + p_{pv}\{v_e(p) - v_e(p-1)\} + p_{iv}v_e(p)$$

This controlled signal is then compared with the carrier signal at 20 kHz i.e., converter switching frequency to generate controlled duty signal for the converter switch. However, gains of the PI controller, are denoted as $p_{pv}$ and $p_{iv}$.

### B. Control of SRM

Here, the SR motor utilizes an optical encoder to estimate the position. A mid-point converter with two split capacitors, excites the motor phases. SRM based drives are often operated in hysteresis current control mode or voltage control mode. This work utilizes a single pulse voltage control mode, such that each phase is switched on and off at least once in every 60° when considering the motor with 8 stator poles and 6 rotor poles. This is called the fundamental switching of the SR motor. The fundamental frequency of SRM at rated speed of 1500rpm is as 150 Hz with 24 strokes per revolution and stroke angle as 15°. However, in case of hysteresis current control, SR motor operates at high average switching frequency, which results in high switching loss and acoustic noise as compared to PWM based control [3]. In SRM, a discontinuous nature of the motor torque, results in high torque ripples when one motor phase is excited at a time. Therefore, in the proposed SRM drive, the motor control is based upon multiphase excitation to reduce torque ripples and vibrations [3], [12]. Table-I shows the four different states with respect to two encoders output $P_1$ and $P_2$. Switches $G_1$ and $G_2$ turn on for state-I, which excite phases A and B. However, state-II turns on $G_2$ and $G_3$ to excite phase B and C. Similarly for state III and state IV, switches $G_3$, $G_4$ and switches $G_4$, $G_1$ turn on such that two phases are excited all the time.

**TABLE-I**
**SWITCHING STATES BASED UPON ENCODER OUTPUT**

| State | Encoder Output | | SRM converter Pulses | | | |
|---|---|---|---|---|---|---|
| | $P_1$ | $P_2$ | $G_1$ | $G_2$ | $G_3$ | $G_4$ |
| State I | 0 | 0 | 1 | 1 | 0 | 0 |
| State II | 0 | 1 | 0 | 1 | 1 | 0 |
| State III | 1 | 0 | 0 | 0 | 1 | 1 |
| State IV | 1 | 1 | 1 | 0 | 0 | 1 |

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## SIMULATED PERFORMANCE

The proposed modified SEPIC fed SRM drive, is considered to evaluate the performance, which are discussed here.

### A. Starting Dynamics

The motor dynamics performance during starting, is shown in Fig. 3. The currents through motor phases, are well shown in this figure. However, $i_A$, $i_B$, $i_C$ and $i_D$ represent currents through phase A, B, C and D, respectively. An increase in motor speed from 0 to 500 rpm, is demonstrated in this figure. During

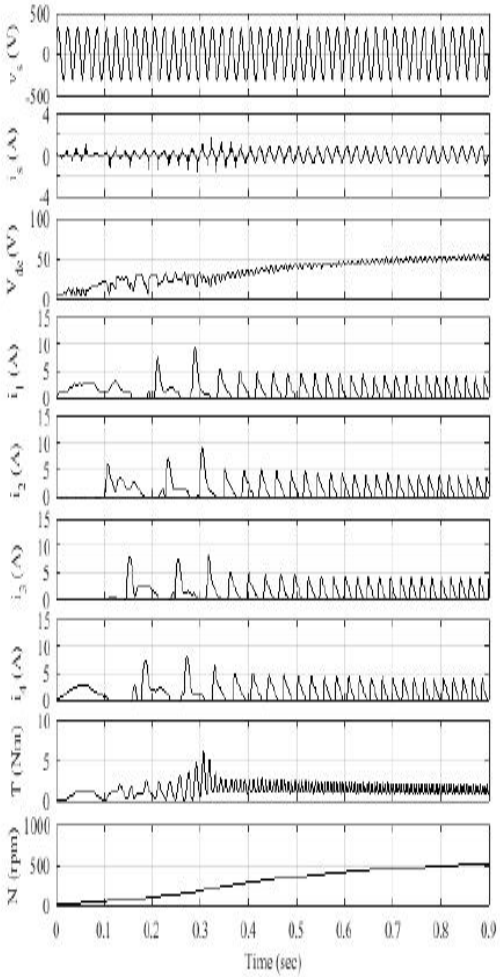
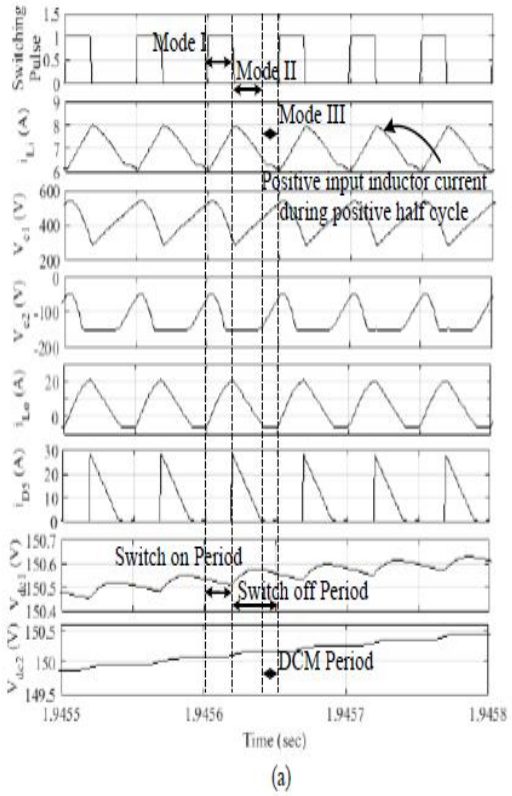



Fig.3 Starting dynamics at $V_{dc}$=50V and $V_s$= 220V

starting reference DC link voltage is set as 50V, which is well tracked by the controller. At reduced speed, an improved power quality operation is achieved as shown in the figure.

### B. Performance During Steady State

The voltage across and current through waveforms in circuit components during different operating modes are demonstrated in Fig. 4. Figs. 5-6 show the steady state performance of the drive for each fundamental frequency period. The converter side performance is shown in Fig. 5. The continuous inductor current $i_{Li}$, the continuous capacitor voltages $V_{c1}$ and $V_{c2}$ and the discontinuous output side inductor current $i_{Lo}$ are well-marked in the figure. The diodes $D_1$ and $D_4$ conduct for one half cycle while other two diodes $D_2$ and $D_3$ conduct other half cycle and the respective diode current is shown in the figure. During steady state condition, the motor side performance is shown in Fig. 6. The motor speed, torque and currents through all the four phases, are shown well in this figure. The stress across switch $S_{w1}$ is shown in Fig. 7(a). The source current THD is obtained as 4.45%, which is demonstrated in Fig.7 (b).




(a)

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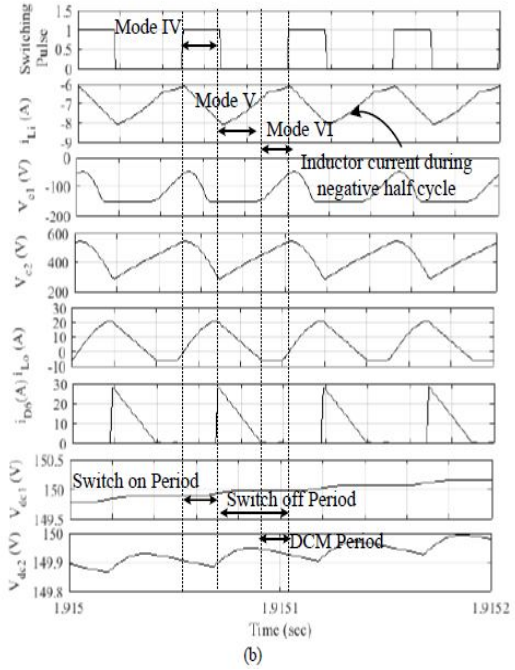



Fig. 4 Simulation results showing waveforms during (a) Mode I, Mode II and Mode III for positive half cycle and (b) Mode IV, Mode V and Mode VI for negative half cycle.

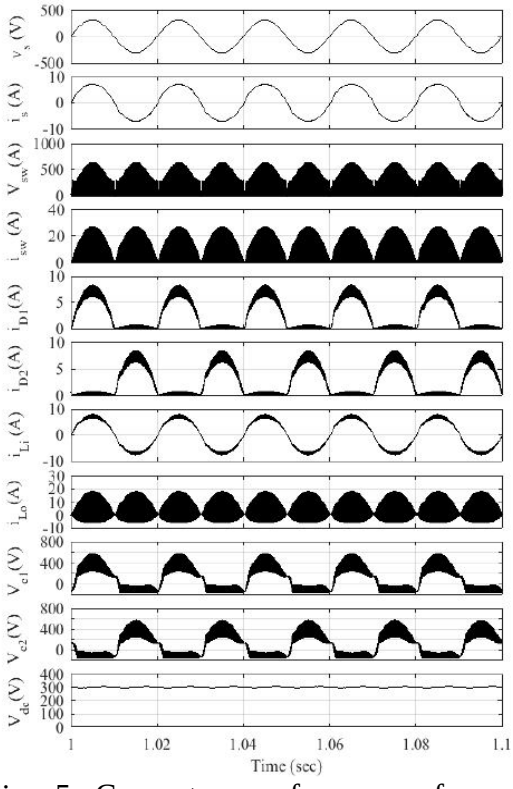



Fig. 5 Converter performance for each fundamental period at 1500 rpm with $V_{dc}$=300V and $V_s$= 220V

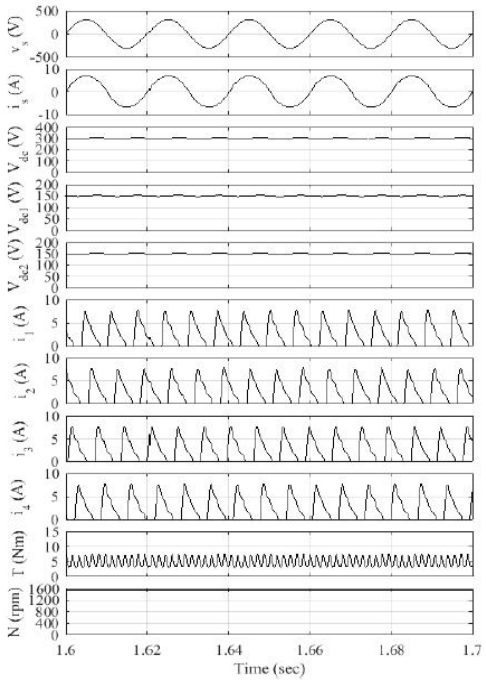
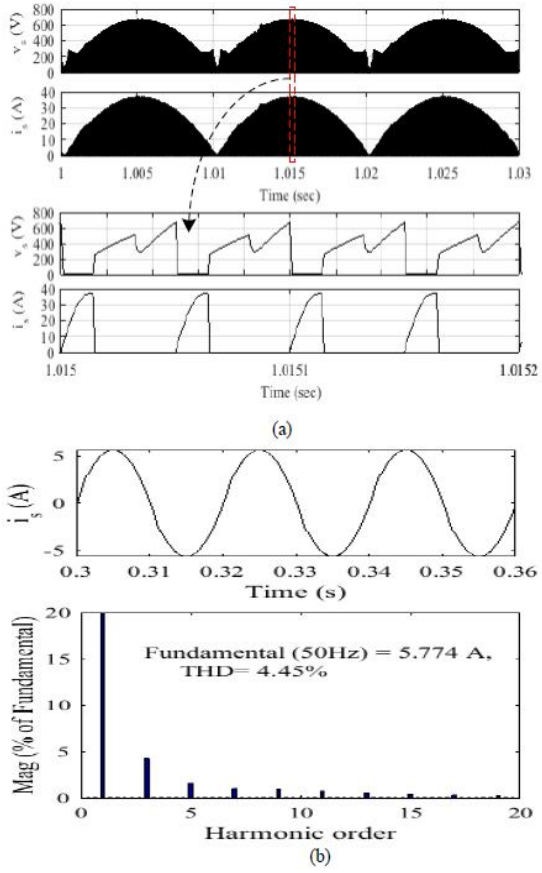



Fig. 6 Motor performance for each fundamental period at 1500 rpm with $V_{dc}$=300V and $V_s$= 220 V



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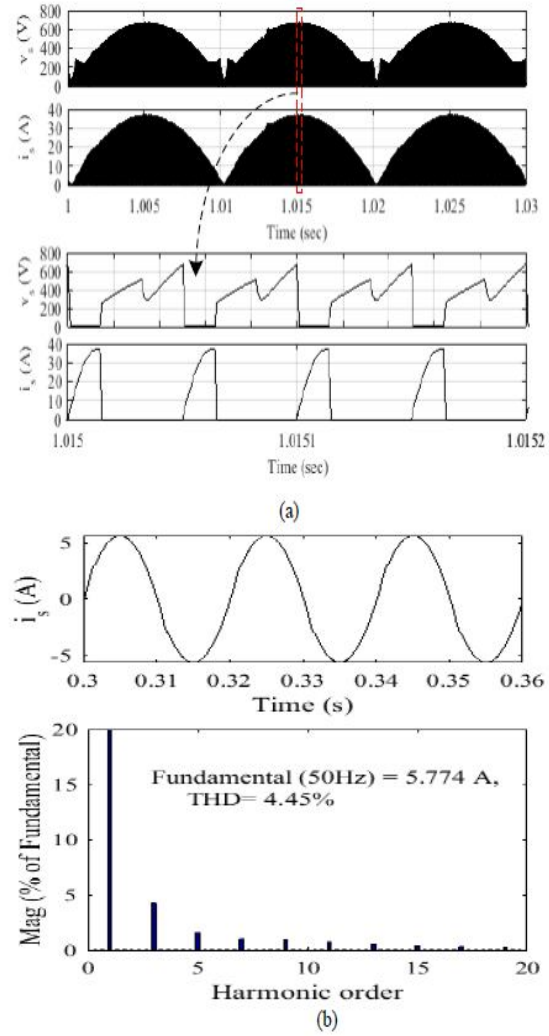


Fig.7 (a) Switching stress with zoomed view given at the bottom, (b) Input current at rated $V_{dc}$=300V and $V_s$=220V.

### *C. Input Voltage Variation*

The proposed PFC SRM drive is designed for practical supply voltage conditions. Therefore, the drive performance is observed with sudden variation in $V_s$ from 220V AC to 170V AC, which is well shown in Fig. 8. As a result of the supply voltage dip, a small inrush source current is observed. The momentarily dip in DC link voltage with a dip in speed from 1 s to 1.15 s, is observed, which is recovered within four to five cycles due to action of PI controller.

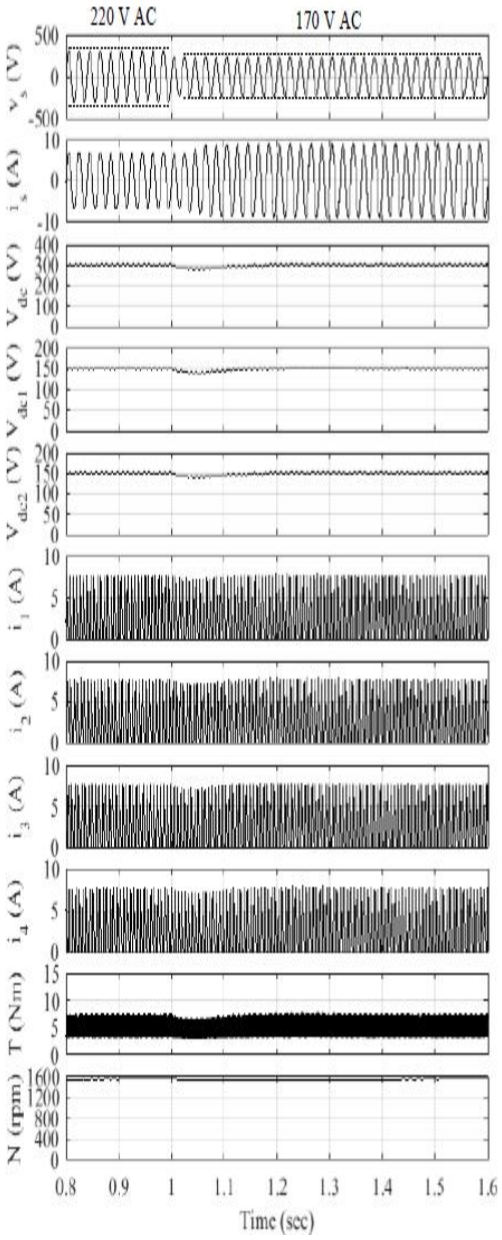


Fig. 8 Dynamics during supply voltage change.

### *D. DC link Voltage Control*

The speed control is considered as a function of DC link voltage, such that with an increase or a decrease in DC link voltage, the speed of proposed drive varies accordingly. Thus, to show the controlled speed operation of the SRM drive, $V_{dc}$ is controlled from 150V to 300V. The obtained results demonstrate the increase in motor current with an increase in supply

current. The change is motor torque and speed, is also observed, which is shown in Fig. 9. The $V_{dc}$ obtained is the summation of two generated output voltages $V_{dc1}$ and $V_{dc2}$ as shown in Figs. 6, 8 and 9. However, $V_{dc1}$ and $V_{dc2}$ are always equal in magnitude for any change in DC link voltage. The performance of the drive is recorded at different DC link voltages, to show the improved power quality operation of the drive for complete speed range. At rated condition, the minimum current THD is obtained as 4.45% with PF as 0.998 when $V_{dc}$ is maintained as 300V. Whereas maximum current THD is obtained as 8% with PF as 0.989 at $V_{dc}$=100V. Table II shows the wide range of speed control with change in $V_{dc}$.

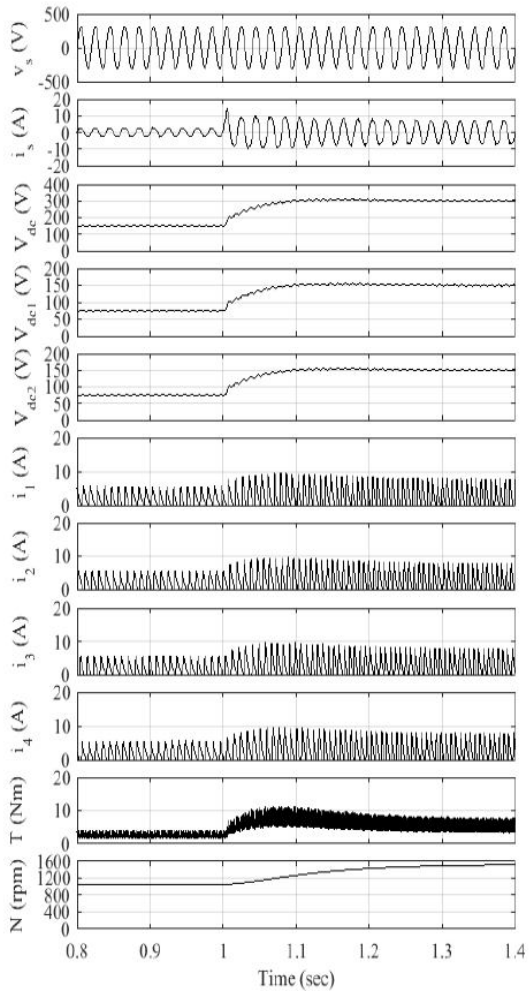


Fig. 9 Dynamics during change in $V_{dc}$ from 150-300 V DC

**TABLE.II**
**SPEED CONTROL OF PROPOSED DRIVE**

| $V_{dc}$ (V) | Speed (rpm) | THD of $I_s$ (%) | Input Current (A) (Peak) | Distortion Factor | Power Factor |
|---|---|---|---|---|---|
| 300 | 1410 | 4.45 | 5.774 | 0.999 | 0.997 |
| 280 | 1370 | 4.65 | 5.191 | 0.998 | 0.997 |
| 260 | 1310 | 5.22 | 4.644 | 0.997 | 0.997 |
| 240 | 1240 | 5.42 | 4.102 | 0.996 | 0.996 |
| 220 | 1170 | 5.78 | 3.615 | 0.996 | 0.996 |
| 200 | 1120 | 5.91 | 3.152 | 0.996 | 0.996 |
| 180 | 1080 | 6.12 | 2.724 | 0.995 | 0.995 |
| 160 | 1000 | 6.63 | 2.290 | 0.995 | 0.993 |
| 140 | 930 | 7.14 | 1.933 | 0.993 | 0.988 |
| 120 | 870 | 7.86 | 1.554 | 0.992 | 0.985 |
| 100 | 790 | 8.02 | 1.222 | 0.992 | 0.989 |

SIMULATION RESULTS

## CONCLUSION

The modified SEPIC converter has the dual output configuration, which is required to feed a mid-point power converter of SR motor. The obtained output voltages, are balanced without any voltage balancing loop. The selected operating mode to obtain PFC, has reduced the inductor size and cost. The SRM drive is controlled by regulating converter output DC voltage and obtained results clearly support the speed control over wide range. Equal or near to unity power factor operation with reduced supply current THD, is demonstrated through simulation and experimental results, which comply with given IEC standard [29]. The overall performance of the drive is validated through obtained results. Thus, proposed SRM drive is expected to find wide applications in household appliances.

## APPENDIX

SRM specifications: 400 W, 8/6 pole, 1500rpm, $L_u$ (unaligned inductance) = 12mH, $L_a$ (aligned inductance) = 110mH, R (winding resistance) = 0.7Ω, $J$ = 0.016kg $m^2$, B = 0.0065Nms: $C_{dc1}$ =$C_{dc2}$ = 1000 μF.

AC mains: 1-ϕ, 220V, 50 Hz, $K_p$ = 0.01; $K_i$ = 0.0008.

## REFERENCES

[1] T. J. E. Miller (Ed.), Electronics Control of Switch Reluctance Machines, Newnes, 2001.

[2] B. K Bose, *Modern power electronics and AC drives*. Englewood Cliffs, NJ:Prentice-Hall, 2002.

[3] R. Krishnan, Switch Reluctance motor Drives: *Modelling, simulation, analysis, design and applications*. New York: CRC Press, 2001.

[4] K. Lu, P. O. Rasmussen, S. J. Watkins and F. Blaabjerg, "A New Low-Cost Hybrid Switched Reluctance Motor for Adjustable-Speed Pump Applications," *IEEE Transactions on Industry Applications*, vol. 47, no. 1, pp. 314-321, Jan.-Feb. 2011.

[5] F. R. Salmasi, B. Fahimi, H. Gao and M. Ehsani, "Sensorless control of switched reluctance motor drive based on BEMF calculation," *APEC. Seventeenth Annual IEEE Applied Power Electronics Conference and Exposition (Cat. No.02CH37335)*, Dallas, TX, 2002, pp. 293-298 vol.1.

[6] S. S. Ahmad and G. Narayanan, "Linearized Modeling of Switched Reluctance Motor for Closed-Loop Current Control," *IEEE Transactions on Industry Applications*, vol. 52, no. 4, pp. 3146-3158, July-Aug. 2016.

[7] G. Gallegos-Lopez, P. C. Kjaer and T. J. E. Miller, "High-grade position estimation for SRM drives using flux linkage/current correction model," *IEEE Transactions on Industry Applications*, vol. 35, no. 4, pp. 859-869, Jul/Aug 1999.

[8] P. P. Acarnley, R. J. Hill and C. W. Hooper, "Detection of Rotor Position in Stepping and Switched Motors by Monitoring of Current Waveforms," *IEEE Transactions on Industrial Electronics*, vol. IE-32, no. 3, pp. 215-222, Aug. 1985.

[9] M. Ehsani and K. R. Ramani, "Direct control strategies based on sensing inductance in switched reluctance motors," *IEEE Transactions on Power Electronics*, vol. 11, no. 1, pp. 74-82, Jan 1996.

[10] E. Ofori, T. Husain, Y. Sozer and I. Husain, "A Pulse-Injection-Based Sensorless Position Estimation Method for a Switched Reluctance Machine Over a Wide Speed Range," *IEEE Transactions on Industry Applications*, vol. 51, no. 5, pp. 3867-3876, Sept.-Oct. 2015.

[11] P. P. Acarnley, R. J. Hill and C. W. Hooper, "Detection of Rotor Position in Stepping and Switched Motors by Monitoring of Current Waveforms," in *IEEE Transactions on Industrial Electronics*, vol. IE-32, no. 3, pp. 215-222, Aug. 1985.

[12] A. M. Jain and N. Mohan, "Dynamic modelling, experimental characterization, and verification for SRM operation with simultaneous two-phase excitation," *IEEE Trans. Ind. Electron.*, vol. 53, no. 4, pp.1238-1249, August. 2006.

[13] L. Huber, L. Gang and M. M. Jovanovic, "Design-Oriented Analysis and Performance Evaluation of Buck PFC Front End," in *IEEE Transactions on Power Electronics*, vol. 25, no. 1, pp. 85-94, Jan. 2010.

[14] A. A. Fardoun, E. H. Ismail, N. M. Khraim, A. J. Sabzali and M. A. Al-Saffar, "Bridgeless High-Power-Factor Buck-Converter Operating in Discontinuous Capacitor Voltage Mode," in *IEEE Transactions on Industry Applications*, vol. 50, no. 5, pp. 3457-3467, Sept.-Oct. 2014.

[15] W. Y. Choi, J. M. Kwon, E. H. Kim, J. J. Lee and B. H. Kwon, "Bridgeless Boost Rectifier With Low Conduction

Losses and Reduced Diode Reverse-Recovery Problems," in *IEEE Transactions on Industrial Electronics*, vol. 54, no. 2, pp. 769-780, April 2007.

[16] D. S. L. Simonetti, J. Sebastian and J. Uceda, "The discontinuous conduction mode Sepic and Cuk power factor preregulators: analysis and design," in *IEEE Transactions on Industrial Electronics*, vol. 44, no. 5, pp. 630-637, Oct 1997.

[17] A. Anand and B. Singh, "Power Factor Correction in Cuk–SEPIC-Based Dual-Output-Converter-Fed SRM Drive," *IEEE Transactions on Industrial Electronics*, vol. 65, no. 2, pp. 1117-1127, Feb. 2018.

[18] T. J. Liang, K. H. Chen and J. F. Chen, "Primary Side Control for Flyback Converter Operating in DCM and CCM," *IEEE Transactions on Power Electronics*, Early Access.

[19] S. F. Lim and A. M. Khambadkone, "A Simple Digital DCM Control Scheme for Boost PFC Operating in Both CCM and DCM," *IEEE Transactions on Industry Applications*, vol. 47, no. 4, pp. 1802-1812, July-Aug. 2011.

[20] W. Kolar, H. Sree, U. Drofenik, N. Mohan and F. C. Zach, "A novel three-phase three-switch three-level high power factor SEPIC-type AC-to-DC converter," *Proc.of 12th Annual Applied Power Electr. Conference and Expo., APEC*, Atlanta, GA, 1997, pp. 657-665 vol.2.

[21] A. Anand, B. Singh, A. Chandra and K. Al-Haddad, "Power factor correction in modified bridgeless buck boost converter fed SRM drive," *IECON 2016 - 42nd Annual Conference of the IEEE Industrial Electronics Society*, Florence, 2016, pp. 3756-3761.

[22] B. Singh and A. Anand, "Power factor correction in modified sepic converter fed switched reluctance motor drive," *2016 7th India International Conference on Power Electronics (IICPE)*, Patiala, 2016.

[23] B. Singh, V. Bist, A. Chandra and K. Al-Haddad, "Power Factor Correction in Bridgeless-Luo Converter-Fed BLDC Motor Drive," *IEEE Transactions on Industry Applications*, vol. 51, no. 2, pp. 1179-1188, March-April 2015.

[24] S. Singh, B. Singh, G. Bhuvaneswari and V. Bist, "A Power Quality Improved Bridgeless Converter-Based Computer Power Supply," *IEEE Transactions on Industry Applications*, vol. 52, no. 5, pp. 4385-4394, Sept.-Oct. 2016.

[25] A. Anand and B. Singh, "Design and implementation of PFC Cuk converter fed SRM drive," *IET Power Electronics*, vol. 10, no. 12, pp. 1539-1549, 10 6 2017.

[26] A. Anand and B. Singh, "Power Factor Correction in single-ended primary inductance converter fed switched reluctance motor drive," *IEEE 1st International Conference on Power Electronics, Intelligent Control and Energy Systems (ICPEICES)*, Delhi, 2016.

[27] B. Singh and A. Anand, "Power quality improvement in bridgeless zeta converter fed switch reluctance motor drive," *39th National Systems Conference (NSC)*, Noida, 2015.

[28] A. Anand and B. Singh, "PFC-based half-bridge dual-output converter-fed four-phase SRM drive," *IET Electric Power Applications*, vol. 12, no. 2, pp. 281-291, 2018.

[29] Limits for Harmonic Current Emissions (Equipment input current ≤16 A per phase), International Standard IEC61000-3-2, 2000.