International Journal of Research
Available at https://edupediapublications.org/journals
p-ISSN: 2348-6848
e-ISSN: 2348-795X
Volume 06 Issue 13
December 2019

DC-Link Capacitor Current Ripple Reduction in DPWM based Back-to-back Converters

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ABSTRACT
This paper proposes an improved offset selection method for discontinuous pulse-width modulation (DPWM)- based back-to-back converters to reduce DC-Link current ripple. DPWM is introduced to power converters to diminish the stress on power transistors and prolong their lifespan. However, when using the DPWM method, the DC-Link current ripple is increased in non-switching regions of the power transistors. Moreover, in DPWM-based back-to-back converters, the DC-Link current ripple reaches its maximum when the two transistors of both inverters are clamped in opposite directions. Therefore, the DC-Link capacitors endure more stress, resulting in decreased life-duration. To overcome this issue, the switching method should consider the clamping periods, when the current ripple increases. This can be achieved by modifying the DPWM offset, so that the clamping states of both converters are matched. The effectiveness of the proposed method is confirmed by both simulation and experimental results.

Keywords: Power conversion, Capacitors, Switches, Rails, Power transistors, Transistors

INTRODUCTION

Voltage source converters (VSCs) are widely used in power generation and conversion systems and proved to be a reliable, low-cost and a highly efficient solution with many advantages such as power factor control and improved harmonic distortion levels [1]. VSC can be controlled to operate either in a rectifier mode or in an inverter mode. With these advantages, the VSC can be found in many applications such as motor drive systems, uninterruptible power supplies (UPS), frequency converters or wind turbine generation systems [2]–[5]. It is also possible to connect several VSCs in parallel to increase the overall power rating [6] and reliability [7]. Connecting two VSCs in series yields a so-called back-to-back converter topology, when one of the VSCs is operated as a rectifier and the other one as an inverter. This topology is very

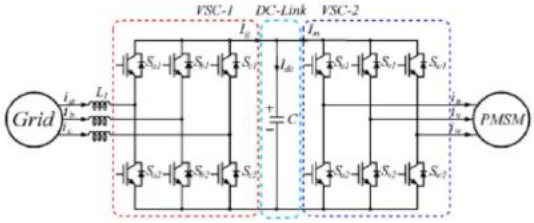


Fig. 1. Circuit configuration of a back-to-back converter.

effective in wind energy conversion systems and traction power systems mostly owing to the capability of the bidirectional power flow [8]–[10]. A DC-Link capacitor is used to maintain the voltage level around an established value in VSCs. This improves the power conversion quality and efficiency. However, the DC-Link capacitor is the weakest part of the system, because it is the subject of a constant stress caused by the high-frequency current. For that reason, a

large value is always chosen for the capacitor, which increases the size of the whole system. Many researches have attempted to find new methods to minimize the DC-Link capacitor size by reducing the current ripple. So far, the most commonly used DC-Link capacitor current ripple reduction technique is a phase-shift of two PWM carriers by 0º or 90º, depending on modulation methods. This method reduces the DC-Link current ripple value up to 50%. However, it can be applied only to a parallel connected VSC system [11]–[15].

Discontinuous pulse-width modulation (DPWM) is used in power conversion systems to improve the efficiency with no change in the hardware or the topology. The DPWM minimizes the switching loss of the power transistors by up to 30%, and provides better harmonic characteristics at high modulation indexes (MI) [16]–[18]. For these reasons, the DPWM is used in active power filters, traction inverters, and UPS (Uninterruptible power supply) [19]–[20]. When the DPWM is used, each power transistor is being fully turned off or turned on for a certain period, usually 60 electrical degrees. The linked reference voltage is clamped to either the positive or negative DC-Link rail. At these moments, the output signal of the clamped phase is being modulated by switching the other 2 phases over the course of the period [5].

Although reducing the switching loss improves the efficiency, the DPWM method, applied to a back-to-back conversion system increases the DC-Link current ripple, and therefore causes more stress on the DC-Link capacitor. Moreover, when both converters are clamped to opposite DC-Link rails, prominent current peaks appear in the DC-Link. As a result, the lifespan of the DC-Link component and the whole system is shortened. On the contrary, when both VSCs are clamped to the same DC-Link rail, the current ripple is reduced. This paper proposes an improved DPWM offset selection method to reduce the DC-Link current ripple in back-to-back converters. The reduction method is accomplished by matching the clamping states of both VSCs and eliminating the regions when the converters are clamped in opposite directions. Therefore, the DC-Link current ripple is reduced along with minimized switching loss of the power transistors. This improves the system reliability and power handling capability with the mitigated DC-Link capacitor and power transistors stresses. The proposed method efficiency is verified by means of simulation and experimental results.

Pulse Width Modulation

Pulse width modulation (PWM) has been actively used in circuits and systems for many years. Its unique features help it participate in various applications, including motor control, telecommunications, switch-mode power supplies (SMPS), and class D power amplifiers (PA). The PWM is an inevitable part of the SMPSs and the class D PAs among the other major applications. Being a part of these circuits and systems makes the PWM be a part of a huge family of products addressing various markets such as consumer electronics, wearable electronics, automotive, healthcare, industrial, military/defense, and aerospace.

The evolution of a simple PWM chip was first started by Silicon General's cofounder and power electronics engineer, Bob Mammano, in 1975 [1]. Constant advances in the electronics technology have triggered the evolution of the first PWM integrated circuit (IC) so that the transition from a simple chip to a complete power management IC (PMIC) was achieved.

The significant role of the PWM in wide range of circuits and systems has been motivating many researchers and engineers to develop its theoretical and practical background for many years. Today, the PWM can be implemented in various platforms with
different methods. The PWM can be implemented by an analog or a digital application specific integrated circuit (ASIC) or general purpose digital ICs such as a field-programmable gate array (FPGA) or a digital signal processor (DSP). Besides, the PWM can be implemented in discrete circuit level with active and passive electronic components.

Brief Description of Pulse Width Modulation

The Pulse Width Modulation (PWM) is a technique in which a reference signal is coded into a pulse train whose widths correspond to the interpretation of the signal itself [6],[10]. The PWM requires two signals; the original signal, also called the "modulating signal", which will be coded into a pulse train, and the "carrier signal", which can be either a triangle wave or a saw-tooth wave. The resulted pulse train is called "modulated signal" which is the PWM signal itself. The PWM signal is generated by comparing the modulating signal with the high frequency carrier signal as depicted in Figure 1.

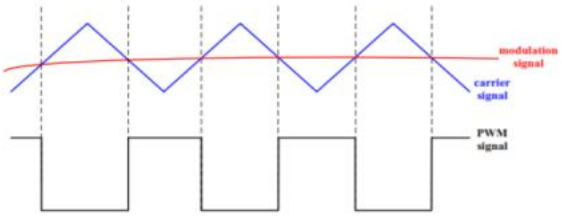
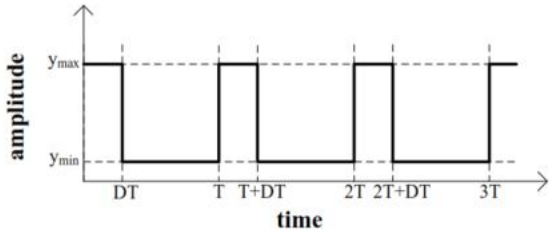


Figure 1 Pulse Width Modulation

As can be seen in Figure 1, the PWM signal is made of rectangular pulses, which switch between high and low levels. Figure 2 shows a close-up view of a sample PWM signal with a defining function y(t), period T, low level value ymin, high level value ymax, and a duty cycle D.



The average value of the PWM signal shown in Figure 2 can be expressed as

$$\bar{y} = D \times y_{max} + (1 - D) \times y_{min}. \quad (1)$$

This relation reveals the direct dependence between the average value of the PWM signal and its duty cycle. The ability of controlling the average value of the PWM signal with its duty cycle creates many application areas for the PWM. The following sub-section summarizes some of the major application areas of the PWM.

Major Applications of Pulse Width Modulation

The pulse width modulation has been playing a critical role in many circuits and systems for a long time. Its unique structure makes the PWM participate in various applications. The major applications of the PWM can be listed as follows:
Motor Control
Motor control is one of the major applications of the PWM for many years [11], [12], [5]. Controlling the speed of an electric motor is achieved by controlling the power delivered to it, which is directly proportional to the voltage applied. This control mechanism is perfectly matched with the idea of the PWM in such a way that the duty cycle of the PWM signal should be decreased to slow down the motor or increased to speed it up. By changing the duty cycle of the PWM signal, its average

value is adjusted to control the power delivered to a motor as it is expressed in (1). In PWM- controlled servomotors on the other hand, the servo position is determined by the width of the pulse instead of the duty cycle of the pulse. Controlling a servomotor with respect to the widths of the PWM signal is shown in Figure 3 with an example, where the servomotor used is HS-322HD of Hitec RCD, USA [13]. As can be seen in Figure 3, the specific values of the pulse widths of the PWM signal correspond to the specific rotation angles.

Switch-Mode Power Supplies

All electronic circuits and systems need power supplies to function. Power supplies can be categorized into two; linear power supplies and switch-mode power supplies (SMPS). Linear power supplies contain transistors working in the active operation region, causing high voltage drops at high currents. Thus, these types of supplies have large power dissipation resulting in low efficiency [10], [14].

SMPSs use transistors as switches in such a way that they allow current passing through them when they are "ON" and they do not conduct any current when they are "OFF". For both cases, the power dissipation over the transistors are ideally zero. Therefore, the switch-type operation of the transistors dramatically reduces the power dissipation of the system resulting in a large improvement in the efficiency. High efficiency, small size and light-weight are the dominant characteristics of SMPSs over linear power supplies helping SMPSs employed in a variety of electronic systems such as personal computers, laptops, and televisions [15].

The PWM is an essential part of most of the SMPS circuits. Kazimierczuk in [10] defines a family of PWM-based circuits consisting of the buck, boost, buck-boost, fly- back, forward, SEPIC (single-ended primary input converter), and dual SEPIC, which are all singleended types. Moreover, there are three multiple-switch PWM-based SMPS circuits such as the half-bridge, full-bridge, and push-pull converters. All of these circuits utilize the PWM in their control loop to adjust the output voltage. The detailed analysis of all PWM-based SMPS circuits are beyond the scope of this work, however for the sake of completeness, the PWM operation will briefly be covered for the buck and boost converter circuits. The circuit topology for the buck converter is shown in Figure 4.

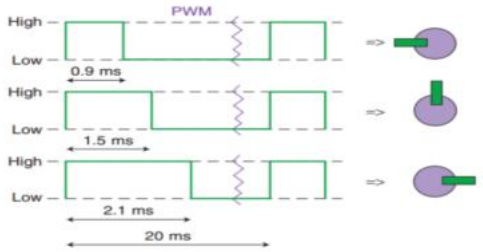


Figure 3 Controlling HS-322HD servomotor with PWM

The circuit operates under the control of the pulse width modulation as follows: when the PWM signal is high, the transistor M will be "ON" making the diode D reverse-biased. Thus, there will be a current flowing through the inductor L charging the capacitor C. When the PWM signal is low, the transistor will be "OFF" and the diode will be forward-biased. Also, the input voltage will be separated from the output since the transistor is "OFF". Within this time interval, the inductor will behave like a voltage source. In other words, the input voltage will supply the current when the PWM signal is high and the inductor will supply the current when the PWM signal is low. If the value of the current never falls to zero, the operation is called continuous mode and the voltage/current waveforms for this operation is shown in Figure 5.

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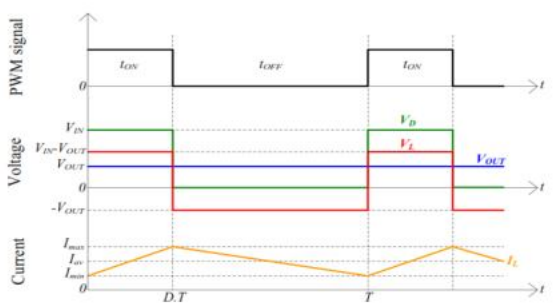

Figure 5 Voltage/current waveforms for the continuous mode buck converter

PROPOSED DPWM METHOD FOR BACK-TO-BACK CONVERTERS

A. Conventional PWM Methods

Fig. 1 shows a typical circuit configuration of a back-to-back converter. The converter is composed of an input stage 3-phase AC power source, grid-side converter (VSC-1), motor-side converter (VSC-2), and a DC-Link capacitor, that is connected between them and an output stage 3-phase AC motor. Each VSC is formed by six power transistors and driven using pulse width modulation (PWM). Sine pulse width modulation (SPWM) and space vector pulse width modulation (SVPWM) are the most commonly used modulation techniques due to their advantages such as implementation simplicity for the former and improved performance for the latter. The drawbacks of the SPWM are high level of total harmonic distortion (THD), poor performance and over-modulation inability. All of them are overcome with the SVPWM method, by using modified sine-wave references. The reference voltage is obtained by adding a modified zero sequence component, usually referred to as an offset voltage into the phase voltage:

$$\begin{cases} V_{an} = V_{as} + V_{sn} \\ V_{bn} = V_{bs} + V_{sn} \\ V_{cn} = V_{cs} + V_{sn} \end{cases}$$

where V_{as}, V_{bs}, and V_{cs} are the phase voltages, V_{sn} is the offset voltage, and Van, V_{bn}, and V_{cn} are the reference voltages. The offset voltage is obtained using the maximum (V_{max}) and the minimum(V_{min}) values of the phase voltage references:

$$V_{sn} = \frac{V_{max} + V_{min}}{2}.$$

However, both SPWM and SVPWM methods applied to high-power VSCs, require the use of transistors with higher

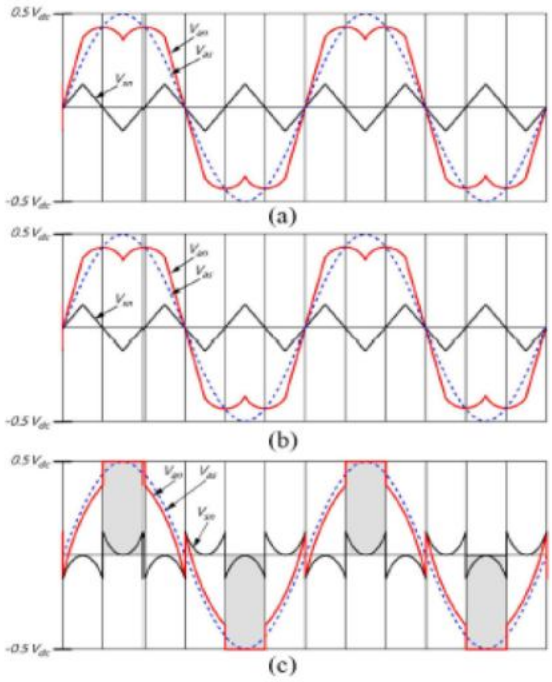

Fig. 2. Reference voltage (Van), phase voltage (V_{as}), and offset voltage (V_{sn}) of Phase A for different modulation schemes: (a) SPWM, (b) SVPWM, and (c) DPWM.

power ratings, due to the stress caused by switching over the periods with the highest current magnitude. To overcome this problem, a DPWM is used. The DPWM minimizes switching loss of each transistor, increasing the lifespan and the reliability with reduced cost [21]. In the DPWM each phase leg output is clamped to the negative or positive DC bus voltage for total of 120º of the fundamental period. Thus, one power transistor is completely off for 60º period, when the phase current magnitude is the

highest, resulting in reduced switching loss for the designated interval, called a non-switching region. For three-phase PWM, the offset voltage should be selected that the reference voltages do not exceed the following limitations:

$$\begin{cases} -0.5V_{dc} \le V_{an} < 0.5V_{dc} \\ -0.5V_{dc} \le V_{bn} < 0.5V_{dc} \\ -0.5V_{dc} \le V_{cn} < 0.5V_{dc} \end{cases}$$

where V_{dc} is a DC-Link voltage.
Therefore, the offset voltage for the DPWM is obtained:

$$-0.5V_{dc} - V_{\min} \le V_{zn} \le 0.5V_{dc} - V_{\max}.$$

There is a variation of DPWM schemes, which can be applied by selecting corresponding offset voltages. The most commonly used one is a 60º DPWM, with the offset calculated as:

$$\begin{cases} V_{zn} = \dfrac{V_{dc}}{2} - V_{\max}, & (V_{\max} + V_{\min} \ge 0) \\ V_{zn} = -\dfrac{V_{dc}}{2} - V_{\min}, & (V_{\max} + V_{\min} < 0). \end{cases}$$

Fig. 2 provides phase voltage references and offset voltages of the aforementioned methods. Fig. 2(a) shows the SPWM waveform. As can be seen, there is no offset added to the reference voltage, so the reference voltage has a sine shape. The SVPWM reference voltage waveform is given in sine-shaped phase voltage. Finally, the waveform of the 60º DPWM method is shown in Fig. 2(c). As is evident, the reference voltage has regions, when the signal is clamped to either 0.5Vdc or –0.5Vdc. During these moments, the corresponding transistors are not operated, and the switching loss are minimized.

B. Proposed DPWM Method

Although the conventional DPWM (CDPWM) method has advantages in terms of cost and transistor loss reduction, there are other issues, which occur due to the reference signal being clamped either to positive or to negative DC-Link rail. In back-to-back topology, using DPWM methods causes the increase of the DC-Link current ripple. Fig. 3 shows the DC-Link current when the system is under the DPWM. The waveform, given in Fig. 3(a), describes the DC-Link current ripple of a bipolar clamping state (BCS), when two VSCs are clamped to opposite rails of the DC-Link. On the contrary, the waveform, shown in Fig. 3(b) depicts the capacitor current ripple in the case of a unipolar clamping state (UCS), in which both converters are clamped to the same rail of the DC-Link. Fig. 4 provides a circuit representation of these states. The BCS is shown in Fig. 4(a). The switches Sa1S and Su1 are clamped to the positive and the negative rails of the DC-Link, respectively. The UCS is given in Fig.4(b), where both switches Sa1 and Su1 are clamped to the same DC-Link rail.

Fig. 5 shows detailed waveforms of the DC-Link current ripple over one switching period. It is assumed, that the switching frequency of both converters is the same and there is no phase shift between two VSCs. The switching frequency is high enough to assume the reference signal values during one switching period constant. Sa1, Sb1, and Sc1 refer to the upper switches of the VSC-1, while Su1, Sv1, and Sw1 represent the upper switches of the VSC-2. Obviously, when an upper switch of a VSC is turned on, the corresponding lower switch is turned off and vice versa. From Fig. 5, the current, flowing through the DC-Link capacitor over the interval t0-t5 is determined by the switching pattern of both VSCs. Therefore, the instantaneous value of the DC-Link

International Journal of Research
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p-ISSN: 2348-6848
e-ISSN: 2348-795X
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current can be determined as a superposition of phase currents of the VSC-1 (ia , ib , ic) and the VSC-2 (iu , iv , iw). It is known, that the sum of all three phase currents is 0, when their switching functions are at the same state:

$$S_a \cdot i_a + S_b \cdot i_b + S_c \cdot i_c = 0$$

$$S_u \cdot i_u + S_v \cdot i_v + S_w \cdot i_w = 0$$

where Sa, Sb, Sc, Su, Sv, and Sw are switching functions of the corresponding phases.

Fig. 5(a) shows the switching pattern and the DC-Link capacitor current ripple for the BCS. The transistors Sa1 and Su1 are clamped to the negative and to the positive DC-Link rails, respectively. Then, during the interval t0-t5, the transistors Sc1,Sb1, Sw1, and Sv1 are turned off sequentially.

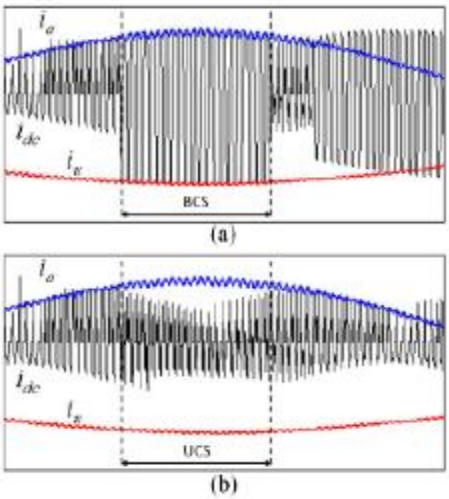

Fig. 3. DC-Link current ripple of the DPWM: (a) BCS and (b) UCS.

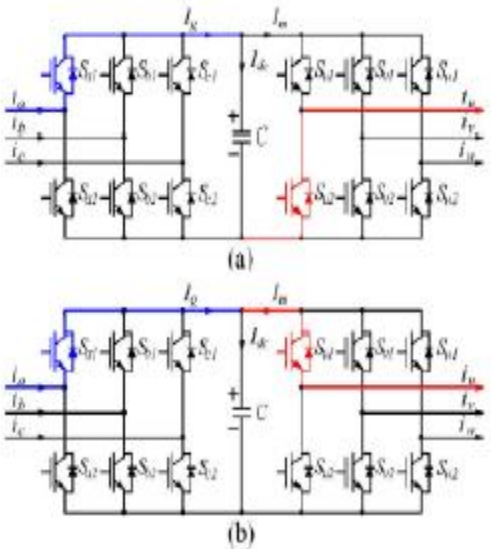

Fig. 4. VSC DPWM clamping states: (a) BCS and (b) UCS.

By considering the currents and the switching states over each period of the intervals t_0-t_5 of Fig. 5(a), the instantaneous value of the DC-Link current under the BCS for each period can be estimated as:

$$I_{dc} = \begin{cases} i_u, & (t_0 < t < t_1) \\ i_u - i_b, & (t_1 < t < t_2) \\ -i_b - i_v, & (t_2 < t < t_3) \\ i_a - i_v, & (t_3 < t < t_4) \\ i_a, & (t_4 < t < t_5). \end{cases}$$

In the case of the UCS, shown in Fig. 3(b), Fig.4(b), and Fig. 5(b), the instantaneous value of the DCLink current is:

$$I_{dc} = \begin{cases} i_u - i_a, & (t_0 < t < t_1) \\ i_u + i_c, & (t_1 < t < t_2) \\ i_c - i_v, & (t_2 < t < t_3) \\ -i_v, & (t_3 < t < t_4) \\ 0 & (t_4 < t < t_5). \end{cases}$$

From Fig. 5, the ratio of the intervals T_0, T_1, T_2, T_3, and T_4 to the carrier period Ts for both the BCS andthe UCS can be expressed as:

$$\frac{T_0}{T_s} = \frac{1}{5} \cdot \left(1 - \frac{v_b}{V_{dc}/2}\right)$$

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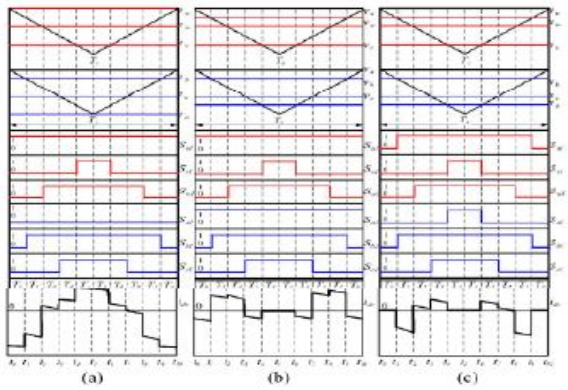

Fig. 5. PWM waveforms through one carrier period: (a) BCS, (b) UCS, and (c) SVPWM.

$$\frac{T_1}{T_s}=\frac{1}{5}\cdot\left(\frac{v_b-v_w}{V_{dc}/2}\right)$$
$$\frac{T_2}{T_s}=\frac{1}{5}\cdot\left(\frac{v_w-v_c}{V_{dc}/2}\right)$$
$$\frac{T_3}{T_s}=\frac{1}{5}\cdot\left(\frac{v_c-v_v}{V_{dc}/2}\right)$$
$$\frac{T_4}{T_s}=\frac{1}{5}\cdot\left(1+\frac{v_v}{V_{dc}/2}\right)$$

where v_a, v_b, v_c, v_u , v_v, and v_w are the reference voltage signals of phases a, b, c, u, v, and w, correspondingly, and V_{dc} is a DC-Link voltage. In this paper, the reference voltage signals are represented as

$$\frac{v_a}{V_{dc}/2}=M_1\cdot\sin(\omega_1 t)+V_{sn1}$$
$$\frac{v_b}{V_{dc}/2}=M_1\cdot\sin\left(\omega_1 t-\frac{2\pi}{3}\right)+V_{sn1}$$
$$\frac{v_c}{V_{dc}/2}=M_1\cdot\sin\left(\omega_1 t+\frac{2\pi}{3}\right)+V_{sn1}$$
$$\frac{v_u}{V_{dc}/2}=M_2\cdot\sin(\omega_2 t)+V_{sn2}$$
$$\frac{v_v}{V_{dc}/2}=M_2\cdot\sin\left(\omega_2 t-\frac{2\pi}{3}\right)+V_{sn2}$$
$$\frac{v_w}{V_{dc}/2}=M_2\cdot\sin\left(\omega_2 t+\frac{2\pi}{3}\right)+V_{sn2}$$

where M_1, ω_1, V_{sn1}, M_2, ω_2, and V_{sn2} are the MI, fundamental angular frequency of the output voltages, and the offset voltages of the VSC-1 and the VSC-2, respectively. The mean square value of the DC-Link current ripple over one carrier period can be calculated as:

$$I_{dc}^2=\frac{1}{T_s}\int_{t_0}^{T_s} i_{dc}^2\cdot dt.$$

Then for the BCS and the UCS the rms value of the DC-Link current ripple can be represented as:

$$I_{dc,BCS}^2=2\cdot\left[\begin{aligned}&\frac{T_0}{T_s}\cdot i_a^2+\frac{T_1}{T_s}\cdot(i_u-i_b)^2+\frac{T_2}{T_s}\cdot(i_b+i_v)^2\\&+\frac{T_3}{T_s}\cdot(i_a-i_v)^2+\frac{T_4}{T_s}\cdot i_a^2\end{aligned}\right]$$

$$I_{dc,UCS}^2=2\cdot\left[\begin{aligned}&\frac{T_0}{T_s}\cdot(i_u-i_a)^2+\frac{T_1}{T_s}\cdot(i_u+i_c)^2\\&+\frac{T_2}{T_s}\cdot(i_c-i_v)^2+\frac{T_3}{T_s}\cdot i_v^2\end{aligned}\right].$$

$$I_{dc,BCS}=\sqrt{\frac{2}{5}\left[\begin{aligned}&(i_a^2+i_b^2)+\left(M_1\cdot\sin\left(\omega_1 t-\frac{2\pi}{3}\right)+V_{sn1}\right)\cdot(i_b^2-2i_a i_b)\\&+\left(M_2\cdot\sin\left(\omega_2 t+\frac{2\pi}{3}\right)+V_{sn2}\right)\cdot(i_a^2-2i_b i_a-i_a^2)+\left(M_2\cdot\sin\left(\omega_2 t-\frac{2\pi}{3}\right)+V_{sn2}\right)\cdot(2i_b i_a-i_a^2)\end{aligned}\right]}$$

$$I_{dc,UCS}=\sqrt{\frac{2}{5}\left[\begin{aligned}&(i_u-i_a)^2+\left(M_1\cdot\sin\left(\omega_1 t-\frac{2\pi}{3}\right)+V_{sn1}\right)\cdot(i_c^2-i_a^2+2i_a(i_a+i_c))\\&+\left(M_2\cdot\sin\left(\omega_2 t+\frac{2\pi}{3}\right)+V_{sn2}\right)\cdot(i_c^2-i_a^2-2i_c(i_a+i_c))\\&+\left(M_1\cdot\sin\left(\omega_1 t+\frac{2\pi}{3}\right)+V_{sn1}\right)\cdot(2i_c(i_a-i_c^2)-\left(M_2\cdot\sin\left(\omega_2 t-\frac{2\pi}{3}\right)+V_{sn2}\right)\cdot i_c^2\end{aligned}\right]}$$

$$I_{dc,SVM}=\sqrt{\frac{2}{5}\left[\begin{aligned}&\left(M_1\cdot\sin\left(\omega_1 t-\frac{2\pi}{3}\right)+V_{sn1}\right)\cdot(i_a-i_b)^2+\left(M_1\cdot\sin\left(\omega_1 t+\frac{2\pi}{3}\right)+V_{sn1}\right)\cdot(i_a^2-i_b^2-2i_c(i_a+i_b))\\&+\left(M_2\cdot\sin\left(\omega_2 t+\frac{2\pi}{3}\right)+V_{sn2}\right)\cdot(i_c^2-i_b^2+2i_b(i_a+i_b))-\left(M_1\cdot\sin(\omega_1 t)+V_{sn1}\right)\cdot(i_a-i_b)^2\end{aligned}\right]}.$$

By substituting (9)–(19) into (21) and (22) the rms of the DC-Link capacitor current can be represented as shown in (23) and (24) at the bottom of the previous page. From the equations (7) and (23), it can be seen, that for the BCS, the instantaneous values of the currents ia and iu result in the capacitor current. Moreover, because the voltage references of these phases are being clamped to the DC-Link rail, the currents ia and iu are close to their maximum values. As can be observed from Fig. 3(a) and Fig. 5(a), the maximum current of the DC-Link capacitor equals to the maximum current of the clamped phases. In addition, the grid-side ac-current influences the positive ripple component of the DCLink capacitor,

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whereas the motor-side ac-current impacts on the negative ripple component. Thus, in the BCS, the DC-Link capacitor current rapidly changes from the maximum negative value to the maximum positive value, resulting in increased rms. On the other hand, as can be seen from (8) and (24), the DCLink capacitor current in the UCS is a superposition of the input and the output ac currents, where the currents of the clamped phases with the maximum values are subtracted from each other. Therefore, the maximum currents of the clamped phases do not result in the ripple component and the capacitor current is reduced for the UCS compared to that of the BCS. The rms value of the DC-Link capacitor in the case of the SVPWM is derived using the same principle as that of the BCS and the UCS.

The time interval ratios and the instantaneous current values can be find from Fig. 5(c). The final equation is given in (25). It can be seen, that similarly to the UCS, the instantaneous current values are subtracted from each other, therefore, the rms value of the current ripple is less than that of the DPWM under the BCS. In a DPWM-based back-to-back system, both the BCS and the UCS occur, causing the prominent current peaks of the DC-Link capacitor. Nevertheless, it is possible to curtail these current peaks by forcing the system to use only the UCS. It can be done by adjusting the offset voltage of both inverters and synchronizing the clamping regions and polarities. In this case, the offset voltage of the second VSC should be calculated considering the clamping periods of the first converter, which yields:

$$\begin{cases} V_{zs} = \dfrac{V_{dc}}{2} - V_{\max.vsc2}, & \left(V_{\max.vsc1} + V_{\min.vsc1} \geq 0\right) \\ V_{zs} = -\dfrac{V_{dc}}{2} - V_{\min.vsc2}, & \left(V_{\max.vsc1} + V_{\min.vsc1} < 0\right) \end{cases}$$

where Vmax.vsc1, Vmin.vsc1, Vmax.vsc2, and Vmin.vsc2 are the maximum and the minimum values of phase voltage references of the VSC-1 and the VSC-2 respectively. Since the proposed DPWM (PDPWM) method is derived the same way as the CDPWM, the maximum modulation index is the same for the CDPWM and the PDPWM and equals 1.15 for both methods. Fig. 6 provides the waveforms of phase voltage references, offset voltages, and reference voltages of the back-to-back

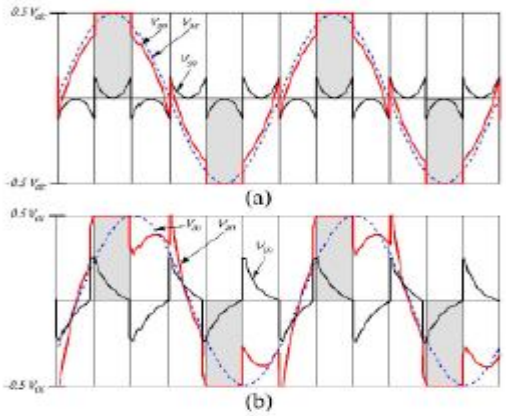

Fig. 6. The proposed DPWM method waveforms: (a) VSC-1 and (b) VSC-2.

TABLE I
SIMULATION AND EXPERIMENT PARAMETERS

Motor		Grid	
Parameter	Value	Parameter	Value
Rated power	11 kw	Line-to-line voltage	110 V_{rms}
Rated speed	1750 r/min	Grid frequency	60 Hz
Rated torque	60.4 N·m	Line resistance	100 mΩ
Number of poles	6	Line inductance	0.930 H
Stator Resistance	349 mΩ	DC-Link voltage	400 V
q-Inductance	15.60 mH	DC-Link capacitor	2.2 mF
d-Inductance	13.17 mH	Switching frequency	10 kHz
Switching frequency	10 kHz		

converter for the PDPWM. It is evident from Fig. 6(a) that the reference voltage of the VSC-1 is the same as with the CDPWM method. However, the reference voltage of the VSC-2 is modified, as shown in Fig. 6(b), so the clamping states of both VSCs are intimately matched. Because the offset voltage of the VSC-2 is obtained, considering the clamping periods of the

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VSC-1, the reference voltage will differ for different speed of the motor.

The simulation of the back-to-back converter was implemented by means of PSIM software to verify the efficiency of the proposed method. The circuit used for the simulation is the same with the one given in Fig 1. The simulation parameters are stated in Table I.

The motor is operated with 20 Nm load. The grid voltage is established at 110 Vrms with the frequency of 60 Hz. The DC-Link voltage is chosen to be 400 V. The DC-Link Capacitance is 2.2 mF. In a typical wind-turbine system, the frequency of the generator-side converter is usually set low to reduce the switching loss, while the grid-side converter frequency is chosen high for improving the current quality and reducing the grid filter size. However, for the proposed method, the switching frequency should be synchronized for both

III. SIMULATION RESULT

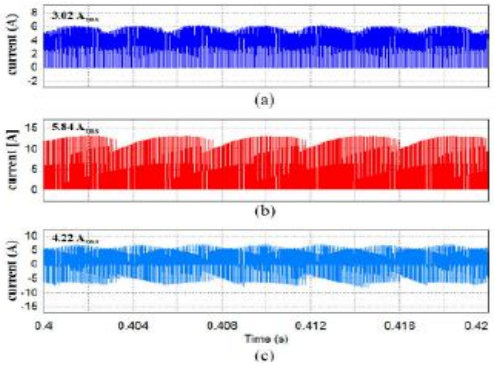

Fig. 7. DC-Link current waveforms for the SVPWM method: (a) VSC-1 DC current, (b) VSC-2 DC current, and (c) DC-Link capacitor current.

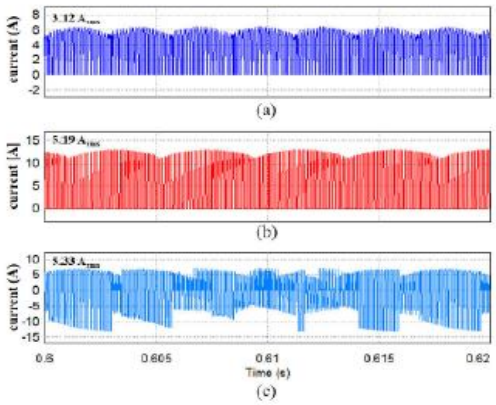

Fig. 8. DC-Link current waveforms for the CDPWM method: (a) VSC-1 DC current, (b) VSC-2 DC current, and (c) DC-Link capacitor current.

converters. For the simulation, the switching frequency is set to 10 kHz for both VSCs.

Fig. 7 shows the DC-Link current ripple waveforms in the case when the VSC-1 and the VSC-2 are controlled using the SVPWM. The rms value of the DC-Link capacitor current is 4.22 A. The simulation results of the CDPWM are shown in Fig. 8. It can be easily observed that the DC-Link capacitor current is increased up to 5.33 Arms, although there is almost no change in the DC-Link current of the VSC-1 and the VSC-2.

Moreover, the DC-Link capacitor undergoes a maximum current with prominent peaks with the amplitude of 10 A when the system is under the BCS and the clamping periods of both converters are not matched. Therefore, when the DPWM is used in a system to reduce the total loss of switching devices, it causes more stress to the DC-Link capacitor resulting in increased capacitance, size and the lifespan. Finally, Fig. 9 shows the simulation results for the PDPWM. It is evident, that the DC-Link capacitor current ripple is reduced for the proposed method by approximately 33 % as compared to the

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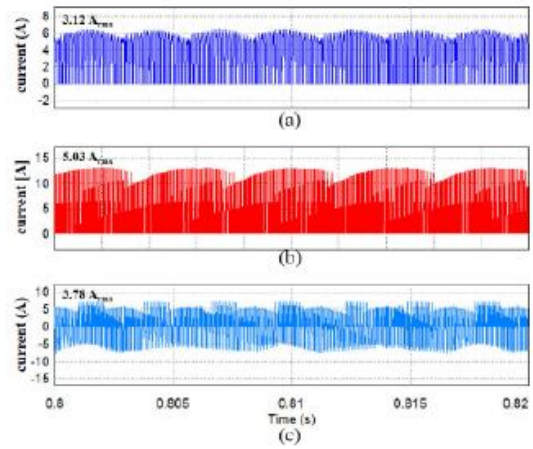

Fig. 9. DC-Link current waveforms for the PDPWM method: (a) VSC-1 DC current, (b) VSC-2 DC current, and (c) DC-Link capacitor current.

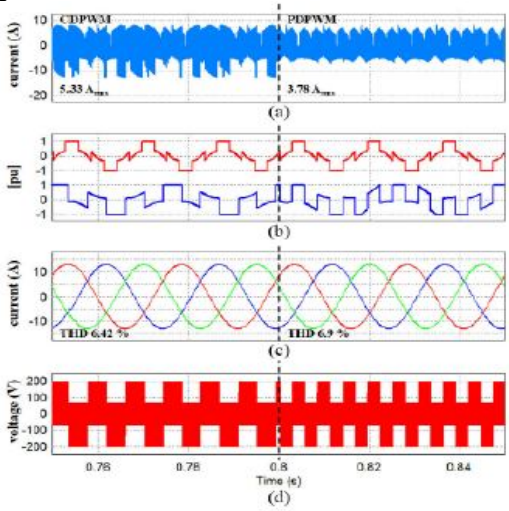

Fig. 10. Simulation waveforms of the CDPWM and the PDPWM: (a) DC-Link current ripple, (b) reference voltages of the VSC-1 and the VSC-2, (c) 3-phase output current, and (d) Common-mode voltage of the motor-side VSC.

CDPWM without a notable effect on the VSC-1 and VSC-2 DC currents. The DC-Link capacitor current ripple is reduced due to the elimination of the BCS, when the maximum current peak occurs. Instead, by matching the clamping states, it is possible to create conditions when the system has only the UCS. In this case, the DC-Link capacitor current ripple is even less as compared to the SVPWM.

Simulation waveforms of the CDPWM and the PDPWM methods are shown in Fig. 10. The prominent DC-Link current peaks, inherent to the CDPWM, are reduced with the proposed PDPWM method, as shown in Fig. 10(a). The reference voltages of both converters are given in Fig. 10(b). Obviously, after the proposed method is applied at 0.8 sec, the DC-Link

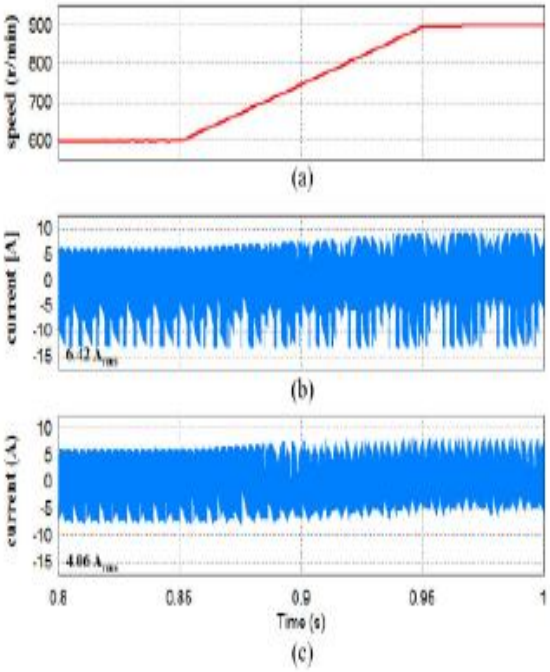

Fig. 11. The DC-Link capacitor current corresponding to the motor speed variation: (a) Motor speed, (b) CDPWM, and (c) PDPWM.

capacitor current ripple is reduced from 5.33 A to 3.78 A. In addition, as can be seen from Fig. 10(c), the proposed method slightly affects the THD level. The amplitude of the common-mode voltage, shown in Fig. 10(d) is not affected, when using the proposed method.

The performance of the proposed method with the motor speed variation is given in Fig. 11. The motor speed is changed from 600 r/min to 900 r/min, as shown in Fig. 11(a). From Fig. 11(b), the prominent current peaks occur when using the

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CDPWM and the DC-Link current ripple increases as the motor speed rises. On the other hand, using the PDPWM reduces the DC-Link current ripple and curtails the current peaks, as can be seen in Fig. 11(c). Fig. 12 shows the frequency spectrum of the DC-Link capacitor current for the SVPWM, the CDPWM, and the PDPWM. Obviously, the first order harmonic is the largest, when using the CDPWM and it is significantly decreased for the PDPWM method. The fourth order harmonic is similarly reduced, when using the CDPWM and the PDPWM compared to that of the SVPWM. The other harmonic components are similar for the three methods.

To estimate the efficiency improvement of the proposed method, the switching loss (PQ.sw) and the conduction loss (PQ.cond) of a transistor are calculated as:

$$P_{Q.sw} = f_{sw} \cdot (E_{ON} + E_{OFF})$$

$$P_{Q.cond} = V_{CE} \cdot I_C \cdot D_{sw}$$

where f_{sw} is a switching frequency, EON is a turn-on energy loss, EOFF is a turn-off energy loss, VCE is a collector-emitter voltage, IC is a collector current and Dsw is a duty ratio. The conduction ($PD_{.cond}$) and the switching loss ($PD_{.sw}$) of a diode are computed as:

$$P_{D.sw} = f_{sw} \cdot E_{rr}$$

$$P_{D.cond} = V_d \cdot I_F \cdot D_D$$

where E_{rr} is a reverse recovery energy loss of a diode, V_d is a diode voltage drop, I_F is a diode forward current, and D_D is a

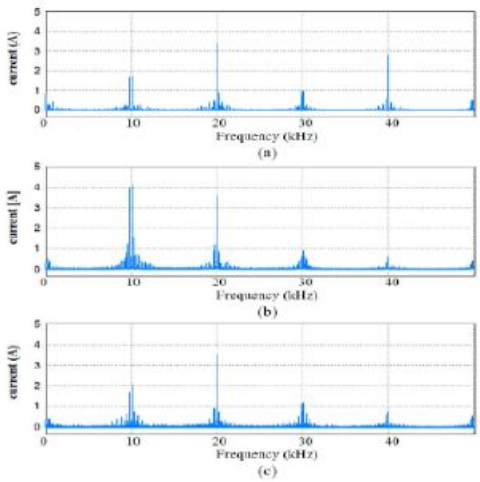

Fig. 12. Frequency spectrum of the DC-Link current: (a) SVPWM, (b) CDPWM, and (c) PDPWM.

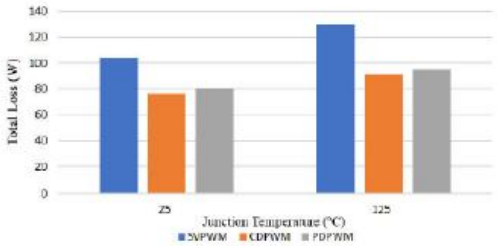

Fig. 13. The total loss comparison between the SVPWM, the CDPWM, and the PDPWM methods at junction temperature 25˚C and 125˚C.

TABLE II
PARAMETERS OF DIODE AND SWITCH

Diode	V_d	0.9 V
	E_{rr}	1.1 mJ/pulse
Switch	V_{CE}	1.65 V
	E_{ON}	1.7 mJ/pulse
	E_{OFF}	2.8 mJ/pulse

diode duty ratio. Fig. 13 provides the loss comparison between SVPWM, CDPWM and the PDPWM methods for two different MI of the VSC-1 at two different junction temperatures, 25˚C and 125˚C respectively. The loss analysis is carried out by PSIM simulation tool. The IGBT module, used for the experiment in this paper is modeled according to the Semikron SK75MLI066T parameters, given in Table II. As can be seen, the total loss is similarly reduced for

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both DPWM methods compared to the SVPWM method

To further confirm the usefulness of the proposed method under different conditions, numerous simulations were implemented for various modulation indexes (MI) of the

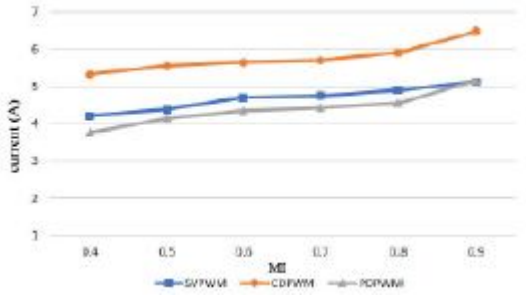

Fig. 14. The DC-Link capacitor current comparison between SVPWM, CDPWM, and PDPWM for different MI.

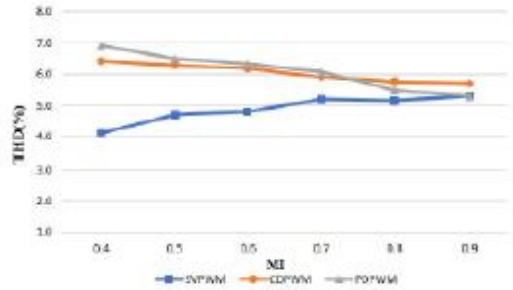

Fig. 15. The THD comparison between SVPWM, CDPWM, and PDPWM for different MI.

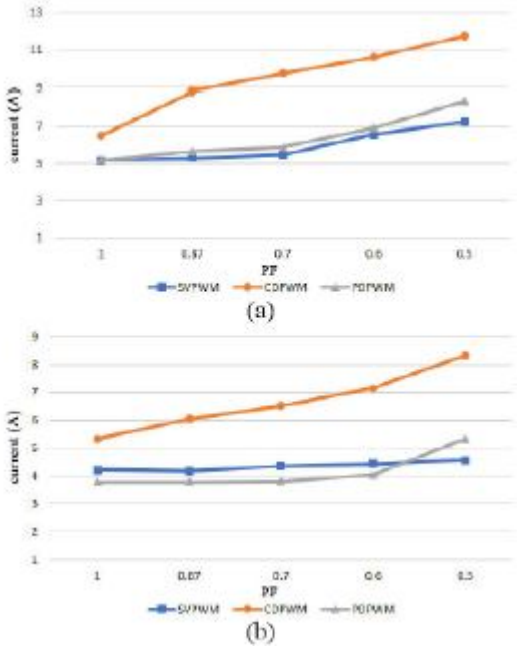

Fig. 16. The DC-Link capacitor current comparison between SVPWM, CDPWM, and PDPWM for different PF: (a) MI 0.9 and (b) MI 0.4.

VSC-2. The load of the motor was set to 20 Nm. The SVPWM, the CDPWM and the PDPWM were mutually applied to both VSCs. Fig. 14 shows the DC-Link capacitor current ripple comparison for the three modulation methods. As shown, the PDPWM method is more superior in terms of the DC-link current ripple reduction compared to the CDPWM and SVPWM. The THD comparison for all three modulation methods is given in Fig. 15. Obviously, the THD level is the least for the SVPWM. At lower MI, the THD level of the PDPWM is higher than that of the CDPWM. However, at higher MI, the THD of the PDPWM decreases compared to that of the CDPWM. The performance of the proposed method with different Power Factor (PF) of the VSC-1 can be seen in

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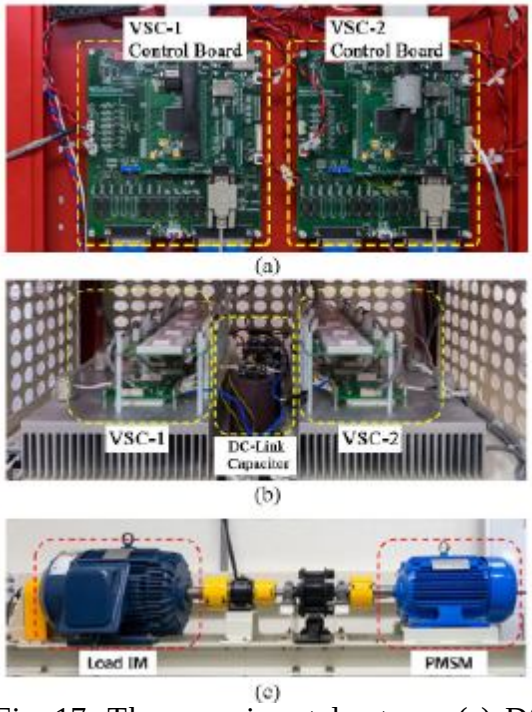

Fig. 17. The experimental set-up: (a) DSP Control boards, (b) Back-to- back converter set, and (c) Motor-load set.

Fig. 16. As is evident, the proposed method reduces the DC-Link capacitor current ripple compared to that of the CDPWM. However, with the higher MI, the performance of the proposed method decreases as the DC-Link capacitor current ripple level is higher compared to that of the SVPWM. However, owing to such advantages as the total loss minimization compared to that of the SVPWM and reduced DC-Link capacitor ripple in comparison to the CDPWM, the proposed method can be used as a tradeoff between the SVPWM and the CDPWM.

IV.EXPERIMENTAL RESULTS

To ensure the feasibility of the proposed method, it was implemented in a laboratory using a twolevel back-to-back converter set shown in Fig. 17. The experimental circuit and parameters are identical to those used for the simulation and given in Table I. The VSC-1 and VSC-2 are controlled by two TMS320F28335 digital signal processor (DSP) control boards. The IGBT switches used in the experimental setup are SK75MLI066T made by Semikron. The switching frequency is set to 10 kHz for both converters. The motor is operated at 600 r/min. Fig. 18 provides the experimental waveforms of the DC-Link capacitor current ripple for the SVPWM, the CDPWM method and the PDPWM method. Evidently, all the waveforms are intimately matched with the simulation results. It can be clearly observed, that the ripple level is increased when using the CDPWM method, given in Fig. 18(b) as compared to the SVPWM shown in Fig. 18(a).

In addition, the current ripple of the DC-Link component is reduced for the PDPWM method as compared to both the SVPWM and the CDPWM, as can be observed from Fig

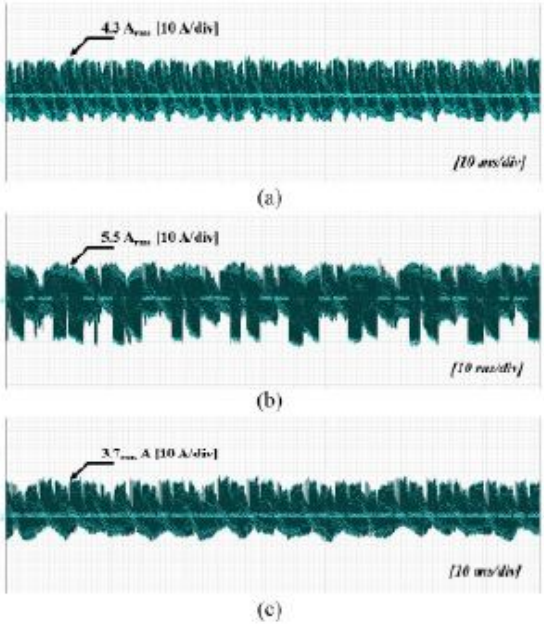

Fig. 18. The experimental results. DC-Link current ripple: (a) conventional SVPWM, (b) conventional DPWM, and (c) proposed DPWM.

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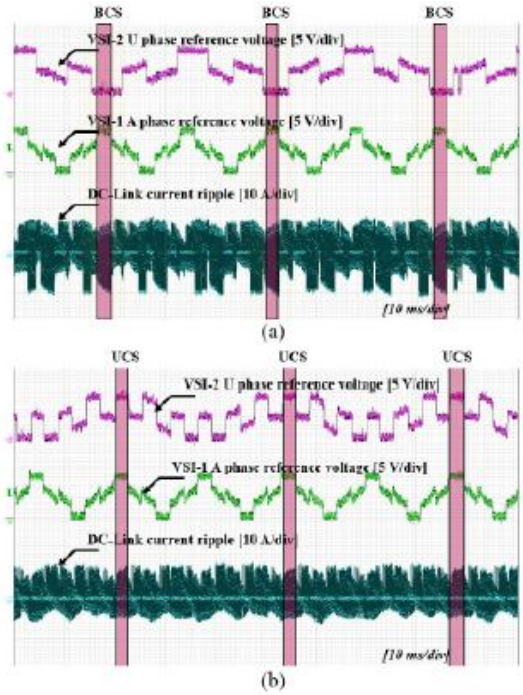

Fig. 19. The experimental results: (a) BCS under the conventional DPWM and (b) UCS under the proposed DPWM.

18(c). Furthermore, as discussed in section II, the prominent current peaks occur when the clamping states of the converters are not matched and the system is under the BCS as shown in Fig. 19(a). The A-phase reference voltage of the VSC-1 is clamped to the positive DC-link rail, while the U-phase reference of the VSC-2 is clamped to the opposite side. This mismatch of the clamping states causes the current peaks of the DC-link capacitor. On the other hand, by applying the PDPWM method to the system, the DC-Link current peaks are

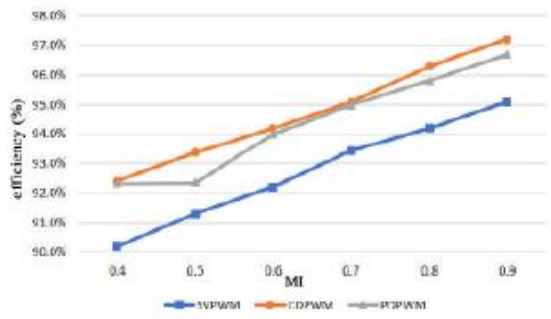

Fig. 20. The efficiency comparison between the SVPW M, the CDPWM, and the PDPWM for different
MI.

diminished with the clamping states of both converters being matched, as is evident from Fig. 19(b).

Therefore, the DC-Link current ripple is reduced from 5.5 A in the CDPWM to 3.7 A of the proposed method. Fig. 20 shows the efficiency comparison between the SVPWM, the CDPWM and the PDPWM. The efficiency is measured using Yokogawa WT3000 power analyzer. Obviously, the highest efficiency is obtained when using the CDPWM. In the case of the SVPWM, the efficiency is the lowest for all the MI. Finally, as can be seen from the graph, the efficiency of the proposed method is higher than that of the SVPWM. Therefore, in terms of the efficiency, the proposed method is a compromise between the SVPWM and the CDPWM.

CONCLUSION

This paper proposed a DPWM method to reduce the DC-Link capacitor current ripple in a back-to-back converter. The proposed method was verified by both simulation and experiment, showing that the DC-Link capacitor current ripple was reduced by approximately 30 % as compared to the CDPWM. The feature of the DPWM such as minimized switching loss of the power switch transistors is also inherent to the proposed method. The efficiency of the proposed method is higher than that of the SVPWM and lower than that of the CDPWM. However, the DC-Link capacitor current ripple is reduced compared to that of the CPDWM. Furthermore, the THD level is in a close range for the CDPWM and the PDPWM. In addition, the performance of the proposed method is still superior for different power factors and modulation indexes. The DC-Link capacitor and

switching devices endured less stress, when using the proposed method. This results in life-span expansion along with decreased size and cost of the whole system. On the other hand, one of the limitations of the proposed method is that the switching frequency of both converters should be the same, which is not typical for some applications, for example, the wind turbine systems. However, the proposed method can be effectively used in any other system, using the back-to-back topology.

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