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"Design of Basic Gates Using CMOS"

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ABSTRACT
In this paper we are going to design basic logic gates: AND, OR and INVERTER using CMOS technology. The paper includes the detailed description of all the basic logic gates (AND, OR and INVERTER), about CMOS technology and logic gates implementation using CMOS technology.

Keywords:
CMOS; AND; OR; INVERTER

INTRODUCTION
Complementary metal oxide semiconductor or CMOS is a widely used semiconductor technology. The term "complementary" refer to the fact that the typical design style with CMOS uses complementary pairs of p-type and n-type metal oxide semiconductor field effect transistors (MOSFETS) for logic functions. Two important characteristics of CMOS devices are high noise immunity and low static power consumption. CMOS uses both NMOS i.e. negative polarity semiconductor and PMOS i.e. positive polarity semiconductor circuit. Since, it consumes very less power. Thus, using this CMOS technology we can design logic gates which are highly efficient by consuming less power.

INVERTER using CMOS

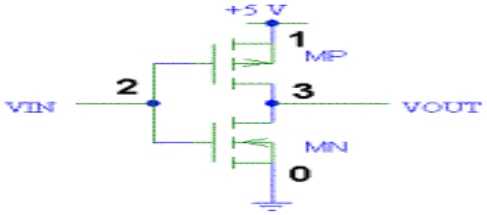

Fig 1. CMOS INVERTER

As we can see from fig 1, the inverter is made by using CMOS technology. In this the circuitry is composed by using two MOSFETs. On the top, it is a PMOS device, whereas the bottom one is the NMOS type. There is no body effect present in either of the two device in the circuit because device is not connected to the device source. Both the gates are connected to the input line. The output is conducted by the drain of both FETs.

OR gate using CMOS

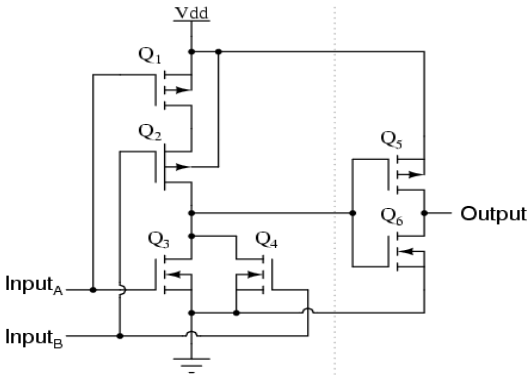

Fig 2. OR gate implementation using CMOS

The OR gate may be built up from the basic NOR gate with the addition of an inverter stage on the output. It uses 6 MOSFETs in the circuit. 4 MOSFETs are used in the NOR function whereas 2 MOSFETs are used in the inverter circuit. The two series-connected sourcing transistors and two parallel-connected sinking transistors. The transistors Q2 and Q4 work as a complementary pair. Each pair is controlled by a single input signal i.e. either input A or B is high.

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AND gate using CMOS

The AND CMOS is made up of two sections, NAND CMOS and INVERTER. Q1 and Q3 resemble the series-connected complementary pair from the inverter circuit. They are controlled by same input signal (input A). And Q2 and Q4 are similarly controlled by the same input signal (input B). The upper transistors of both pairs (Q1 and Q2) have their source and drain terminals paralleled, while the lower transistors (Q3 and Q4) are series-connected.

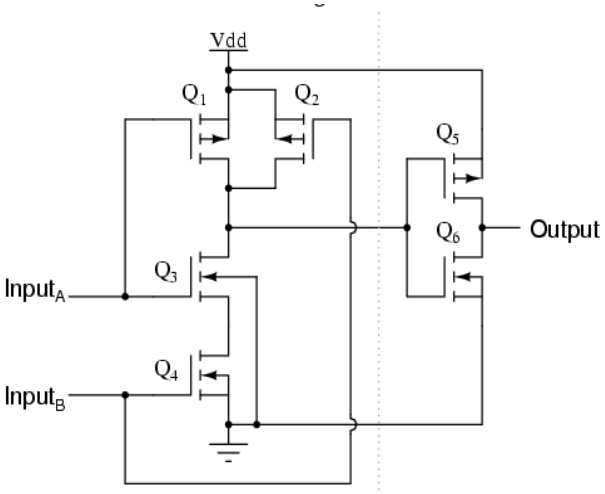

Fig 3. AND using CMOS

CONCLUSION

So, in this paper we have implemented the basic logic gates using CMOS: AND, OR and INVERTER (NOT gate) namely. In today's scenario the CMOS technology is coming best. Because it consumes low power. So, by consuming low power we are driving this era towards the future of CMOS. And by implementing simple logic gates using CMOS we are making our digital world very efficient and reliable on low power. Since, it also has a good size factor i.e. CMOS technology implements on chips and reducing the size of the gadgets.

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