International Journal of Research (IJR)
e-ISSN: 2348-6848, p- ISSN: 2348-795X Volume 2, Issue 05, May 2015
Available at http://internationaljournalofresearch.org

Design of full adder using VHDL

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ABSTRACT
*In thi paper we are going to design full adder using VHDL. The acronym VHDL stands for **V**HSIC (Very High Speed Integrated Circuits) **H**ardware **D**escription **L**anguage. This paper includes the design of full adder with behavioral modelling in VHDL, truth table and results are verified with simulation software Xilinx.*

Keywords:
VHDL, VHSIC, full adder, behavioral modelling, simulation, xilinx

INTRODUCTION

The digital systems include lots of digital systems on a chip and board. This paper implements the design of full adder using VHDL language. The VHDL is very flexible hardware description language. It offers multiple kinds of modeling to describe the hardware of the circuit we wants to implements. In this paper we are using behavioral modelling in designing full adder. Behavioral style of modelling specifies the behavior of an entity with the help of sequentially executed statements.

FULL ADDER

Full adder is a digital device which adds binary numbers and accounts for values carried in as well as out. A one-bit full adder adds three one-bit numbers, often written as A, B and Cin; A and B are the operands, and Cin is a bit carried in from the previous less significant stage. The full adder is usually a component in a cascade of adders, whch add 8, 16, 32, etc. bit binary numbers. The circuit produces a two-bit output, output carry and sum typically represented by the signals Cout and S. A full adder can be implemented in lots of ways such as with a custom transistor-level circuit or composed of other gates.

BOOLEAN EXPRESSION

$S = A \oplus B \oplus Cin$

$Cout = (A.B) + (Cin \,.\, (A \oplus B))$

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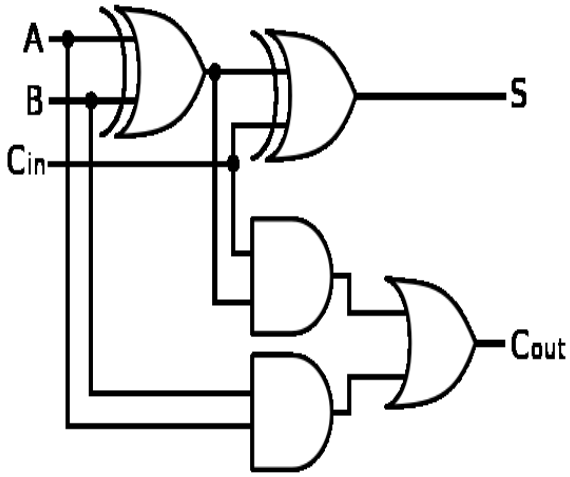

Fig. *Circuit Diagram of full adder*

INPUT			*OUTPUT*	
A	*B*	*Cin*	*S*	*Cout*
0	*0*	*0*	*0*	*0*
0	*0*	*1*	*1*	*0*
0	*1*	*0*	*1*	*0*
0	*1*	*1*	*0*	*1*
1	*0*	*0*	*1*	*0*
1	*0*	*1*	*0*	*1*
1	*1*	*0*	*0*	*1*
1	*1*	*1*	*1*	*1*

Fig. *Truth Table of Full Adder*

Program in VHDL

```
library IEEE;
use IEEE.STD_LOGIC_1164.ALL;
use IEEE.STD_LOGIC_ARITH.ALL;
use IEEE.STD_LOGIC_UNSIGNED.ALL;

---- Uncomment the following library declaration if instantiating
---- any Xilinx primitives in this code.
--library UNISIM;
--use UNISIM.VComponents.all;

entity full is
   Port ( a : in  STD_LOGIC;
          b : in  STD_LOGIC;
          Cin : in  STD_LOGIC;
          S : out  STD_LOGIC;
          Cout : out  STD_LOGIC);
end full;

architecture Behavioral of full is

begin
process(A,B,Cin)
begin
if(A='0' and B='0' and Cin='0')then
S<='0';
Cout<='0';
elsif(A='0' and B='0' and Cin='1')then
S<='1';
Cout<='0';
elsif(A='0' and B='1' and Cin='0')then
S<='1';
Cout<='0';
elsif(A='0' and B='1' and Cin='1')then
S<='0';
Cout<='1';
elsif(A='1' and B='0' and Cin='0')then
S<='1';
Cout<='0';
elsif(A='1' and B='0' and Cin='1')then
S<='0';
Cout<='1';
elsif(A='1' and B='1' and Cin='0')then
S<='0';
Cout<='1';
else
S<='1';
Cout<='1';
end if;
end process;


end Behavioral;
```

CONCLUSION

We have used VHDL coding for design of full adder. VHDL offers very high flexibility as it is the only most flexible Hardware description language. It offers flexibility in design reuse and move design between multiple vendors tools. VHDL facilitates a top-down design methodology using synthesis design at high implementation-independent level, Delay decision on implementation details, we can

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easily explore design alternatives, solve architecture problems before implementation and automatic mapping of a high-level description technology specific implementation.

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