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FPGA and a simulator core design for a-d communication

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ABSTRACT

The main purpous of this paper we present a Field Programmable Gate Array (FPGA) core (mega-function) design prepared to simulate the communication between an Analog to Digital Converter (ADC) and FPGA which were both located on an education board. The simulator core imitates ADS7824 coded ADC Integrated Circuit (IC). It is tested that the simulator core helps students to understand ADC theory better and make more practical and reliable designs related to ADC. We have preferred Graphics design for Educational purposes and all design steps were given in the study. This study included to a project called "FPGA based digital Electronic education" as an instructive and attractive example. This core can be used not only by students for educational purposes but also by Electronic Designers for general

INTRODUCTION

This study is a part of the project "FPGA Based Digital Electronic Education" presented at IKECCO`2006 in Bishkek (Kıray, 2006). The stages and details of the project were given at the conference.

There are lots of programs at the Universities in all over the world using the FPGAs as Education material. The names of the some similar studies were given at references part (Andreas and Ulrich (1993), Li and Chu, (1996), Mark (2004), Mark and Scott (2003), Camilo et al. (2005), Jerry, (2004). What makes our project different from others is that it aims to teach digital electronics and it involves some special design samples.

ADC-SIMULATOR CORE DESIGN

Modules for data channel selection, parallel and serial conversions are developed at the rest three steps. All the modules seen in Figure A-1 at appendix are combined under a block named ADC_IC_SIM_1 seen in Figure 4. It is impossible to represent the analogue data at simulator. That's why the 4 different 12-bit extra data inputs named TEST_DATA _IN_A, B, C and D were used instead of analogue data. The rest inputs and outputs are the same with ADS7824 IC. After testing any design by using the ACD simulator core, the inputs and outputs connected to the simulator core will be connected to those pins devoted to ADS7824 in the FPGA.

Data channel selection module

This module simulates the ADS7824 data channel selection function. Figure A-2 at appendix shows internal design of data channel selection module. The module consists of four 12-bits Dff registers, a multiplexer and a decoder. All channel outputs located after 12-bits registers are connected to multiplexer. Decoder and the multiplexer work parallel. While decoder makes the output of selected channel active, the multiplexer sends the selected data of the channel to out of the module. Both of them complete their functions according to position of CHN (3.0).

A parallel conversion module

All data can be received as serial or parallel after the completion of analog to digital conversion in ADS7824 IC. According to simulator's PAR-SER pin position (0 or 1); the parallel or serial conversion module is selected. 12-bit parallel data in 8-bit channel is sent in two stages: firstly 11-4 bits of data are sent and then the rest 3-0 bits are sent. The design of the module can be seen in Figure A3. Main function of this module is to imitate the operation of 12-bits parallel data getting through 8-bits bus in two stages. BYTE signal plays active role for this operation. The first byte (11-4 bits) is received while BYTE signal is low and then second byte (3-0) is received while BYTE

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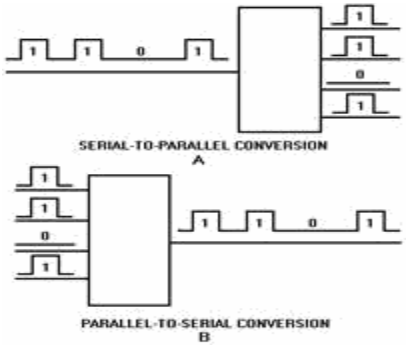
signal is high. There is an assistant module named schaltung3 used to generate BUSY_PAR signal. Main function of the assistant module is to make delay.

Serial conversion module

The operation of this module is based on shift register and counter logics. Serial data reading starts with CS or RC signal. There are three assistant blocks. First one is 1294 Sci. Res. Essays



Busy signals

At the end of the parallel or serial conversion, simulator busy signal is sent by using multiplexer.

Conclusion

Altera Quartus II program is used to test the simulator core. An example was developed to test performance of the simulator. ABC, BCD, CDE and DEF values were given from the test inputs and serial-parallel outputs were observed by changing channel selection bits. All simulation results for the simulator core can be seen in Figure A-5a and A-5b at appendix. After completing the general simulation studies, Inputs and outputs which were connected to the simulator core, this time will be connected to those pins devoted to ADS7824 in the FPGA for hardware tests.

This study is important for two reasons:

a) A general example for students, which explains all steps of the design in details.
b) A good similator toll for designers, which makes any ADC related design easy.

FPGA based Digital Electronics Education was started as a project at International Ataturk Alatoo University in corparation with Zurich Technology University in 2006.

After teaching how to use the basic componets and some first level examples, some instructive and attractive projects were developed for the FPGA based Digital Electronic Education program. The Similator core design is one of them. The other four instructive and attractive projects are “clock-calender”, “calculator” ,“basic CPU” and “PID controller” designs. These projects will also be presented.

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