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Novel VLSI Architecture of Fir with Lut Less Method Using Distributive Arithmetic for DSP Applications

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ABSTRACT

Adder and multipliers are used in many processors to accomplish fast arithmetic function. Many different adder architecture designs have been developed to increase the efficiency of the adder. A filter is used to pass a specific band of frequency. Depending on the response of the system, digital filters can be classified into Finite Impulse Response (FIR) and Infinite Impulse Response (IIR). Digital filters are widely used in many digital signal processing applications. Therefore digital filtering is one of the basic need of digital signal processing. In traditional fir filter consumes more power and area because of multipliers usage to avoid this disadvantage in this paper designs a new approach to design a fir filter by using distributive arithmetic method in lutless method. In this paper fir with traditional adder is existed design and fir filter using parallel prefix adder is the proposed design. Parallel prefix adders are the good adder for fast execution it is reduce the complexity of the multiplication process, it causes to reduce the power and area of the design Performance of all adder designs. And this project implemented for 64 bit lut less fir structure; these structures are synthesized on Xilinx 12.3 ISE tool.

Key words: Registers, multiplexers, carry skip adder, Brent Kung adder, and accumulator and DA method.

I. INTRODUCTION

Area of Digital Signal Processing (DSP) is of extreme importance as it performs the processing of digital signal. A complex DSP system involves several adders and multipliers. An efficient design of adders and multipliers improves the performance of complex signal processing system.

Fundamental components are adders which are very frequently found in the many different networks that are in different blocks of many systems like controllers and processing chips. A system's performance is basically estimated by the ability of the working of adder and multiplier Filter is a frequency selective network.

A filter allows a particular band of frequencies and attenuates all the remaining frequencies. Analog and digital are the two types of filter. Depending on the impulse response of a filter it is classified into two types one is finite impulse response and the other is infinite impulse response. In the industry of electronics digital filters are used. Compared to analog filters digital filters have attain much signal to noise ratio for this reason we use digital filters than analog filters.

The digital filters will perform noiseless mathematical operations at each intermediate step in the transforms. Design

engineers use digital filters to achieve better performance level that are difficult to obtain with analog filters. The three operations will do in digital filters are Addition operation or subtraction, Multiplication of a signal by a constant value and Delaying a digital signal by one or more sample periods.

A graphical means of describing a digital filter whereby the behavior of the filter is described by in below figure

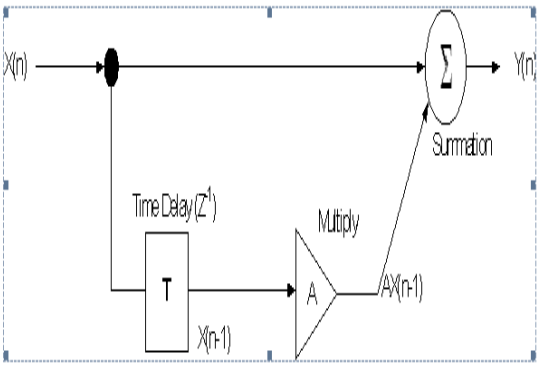

Fig.1: Block Diagram of a Simple Digital Filter

$\delta(n)$ Is the unit impulse function given as input to a filter and its response is h (n). if the impulse response of a system is known, it is possible to calculate the system response for any input sequence x (n). at sample index n = 0 the unit impulse is applied to the system.

The impulse is non-zero only for values of n greater than or equal to zero i.e., h (n) is zero for n<0. This impulse response is said to be casual otherwise the system would be producing a response before an input has been applied. It is known from the time-invariance property of a Linear Time Invariant System that the response of a system to a delayed unit impulse $(n-k)$. Tap delay fir filter equation (1)

$$y[n] = \sum_{k=0}^{N} h(n)\, x(n-k) \qquad (1)$$

II. DISTRIBUTED ARITHMETIC METHOD-OVERVIEW

Multipliers are the complex and time consuming process in the FIR filter. In order to remove the redundancy of multiplication process, several multipliers-less method have evaluated. This multiplier less method is classified into two types namely methods based on conversion and methods based on memory.

In conversion based method, the coefficients of the FIR filter are converted into other numerical forms other than the binary forms for effective hardware implementation and reduced delay. Canonical Signed Digit is the numerical form, in which the coefficients are written in terms of powers of two is used to reduce the complexity of the multiplication process.

On the other hand Look up Tables is used for storing the pre calculated co products in memory based techniques. DA (Distributed Arithmetic) based on memory based techniques is trending architecture in recent years because of its high performance.

Distributed Arithmetic is the extension of multiply and accumulate unit (MAC). It is efficient technique for calculation of inner product or sum of products or multiplies and accumulates. Distributed Arithmetic is a technique that is bit serial in nature. Efficiency of mech-anization is the advantage of Distributed Arithmetic (DA). The Expression of Distributed Arithmetic section is given as

$$Y = \sum_{k=1}^{K} A_k x_k \qquad (2)$$

Where the fixed coefficients are represented as AK, the input signal is represented as xk and K is the number of input words. X_k can be modeled as

$$x_k = -b_{ko} + \sum_{n=1}^{N-1} b_{kn} 2^{-n} \qquad (3)$$

Where xk={bk0……..b k(N-1)}, the output equations can be expressed as

$$y = \sum_{n=1}^{n-1} [\sum_{k=1}^{K} A_k b_{kn}] 2^{-n} + \sum_{k=1}^{K} A_k (-b_{k0}) \qquad (4)$$

The equation (4) is the finalized form of Distributed Arithmetic Technique. The value of is either 0 or 1 and has 2k possible values. The pre-computed results are store in the ROM. The Size of the ROM is 2 x 2^k, since it has to store both positive and negative values of b_{kn} .hence the size of the memory increases with the word size.

The Diagrammatic representation of the Binary based Distributed Arithmetic is shown in the figure 1.X1, X2, X3, X4 are the input lines which are carried as single bit with Least Significant Bit of $b_{kN-1}$and the sign bit of b_{k0}as the Most Significant bit. S is the sign bit timing signal. If S is set at position1 then S is set as 1 for sign bits and set as 0 for others. During the Clock cycle, the switch will be in position 2.

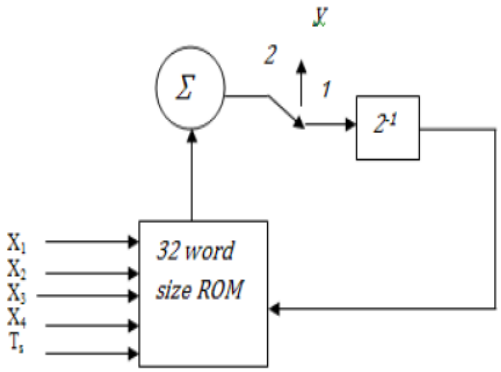

Figure2: Binary Based DA Technique

III.DISTRIBUTED ARITHMETIC ARCHITECTURE WITH LUTLESS FIR FILTERS:

In LUT less DA method, the LUT is replaced with multiplexers and adders as shown in fig 6. Because of the absence of LUT, the structure is called LUT less architecture [8]. This results in reducing area and power consumption. The hardware requirement is less compared to the DA technique. For a 3rd order FIR filter, four multiplexers are used. Each multiplexer has two inputs.

One input is the coefficient of FIR filter and the other input is binary value 0. The LSB of input shift register is used as a select line for the multiplexer. If the select line is '1', then the coefficient of the filter is passed to output. If the select line is '0', then the binary value 0 is passed to the output.

The output of first two multiplexer is added and the output of remaining two multiplexer is added. The result obtained from both adders are added using another adder. The LUT based DA filter can be used only for fixed coefficients. LUT less FIR filter is used for dynamic structures highly advantageous for reconfigurable filter where coefficients change during run time.

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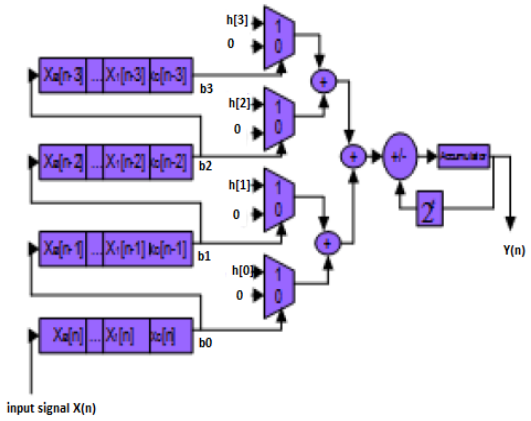

Figure 3: LUT-less DA architectures

IV. BRENT-KUNG ADDER

Brent Kung adder is one of the parallel prefix adders. It is the most popular adder that is used to increase the speed of operation. These adders are designed by using carry look ahead adders structure. It consists of three stages Pre-processing carry propagation (p) and carry generation (g) signals. Calculation of the sum value by using carry generation and propagation signals. In the preprocessing stage carry propagate and generate equations are found by using the generalized equation $P_i = A_i$ XOR B_i and $G_i = A_i$ AND B_i

By using these equations we proceed for further process i.e., calculating the carry values.

- ❖ The carry value c0 is generated by using p0 and g0 values.
- ❖ The carry value c1 is generated by using p1 and g1 and also the previous values p0 and g0.
- ❖ Similarly carry value c2 is generated using p2, g2 and previous values p1 and g1.
- ❖ The end value will be the final value of carry which is denoted here as Cout.

The generalized carry generate and carry propagate equations are

$C_p = P_i\ P_{i-1}$ and $C_g = G_i + (P_i\ G_{i-1})$

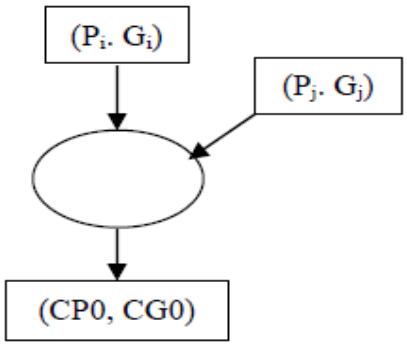

Fig 4: carry generation and propagation network

The next stage is post processing stage in which final value of sum is calculated. The generalized equations are $S_i = P_i . C_i$ and $C_{i+1} = (P_i . C_i) + G_i$

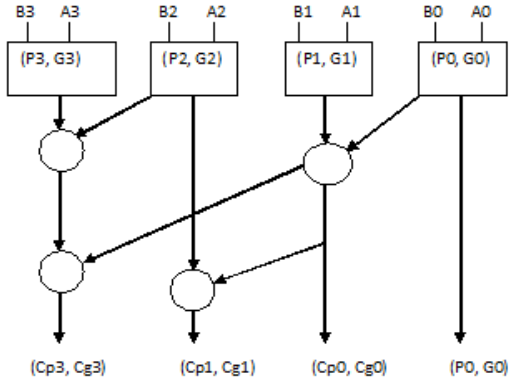

Fig5: 4-bit Brent Kung adder

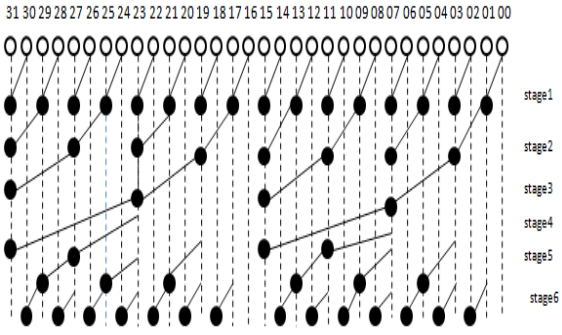

Fig6: 32-bit Brent Kung adder

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V. RESULTS

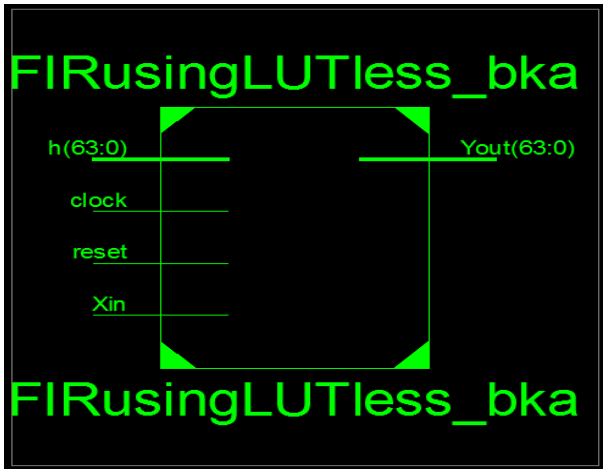

Figure 7: RTL Schematic

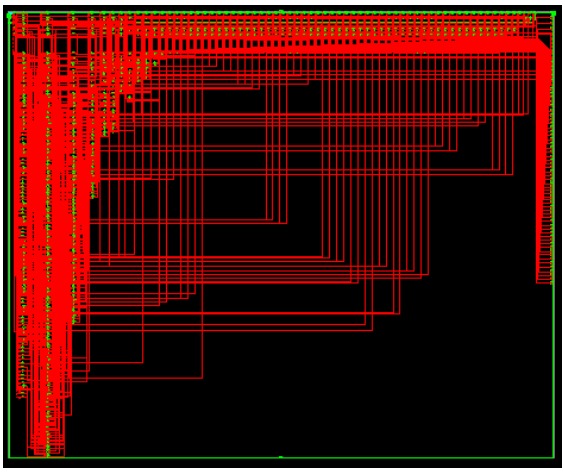

Figure 8: view technology schematic

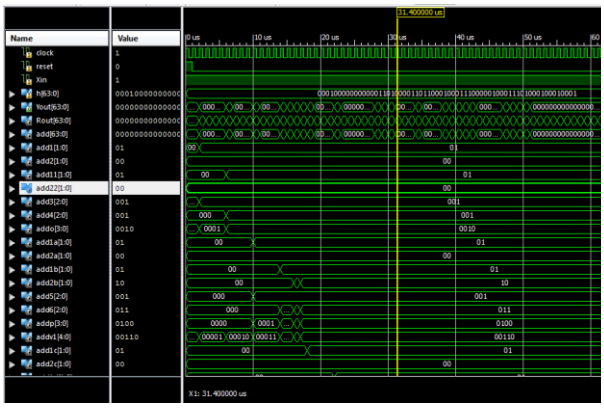

Figure9: simulated waveform

Parameter	FIR with CSKA	FIR with BKA
No of LUTs	554	401
Power (m Watt)	4.521	3.272

Table 1: parameter comparison table

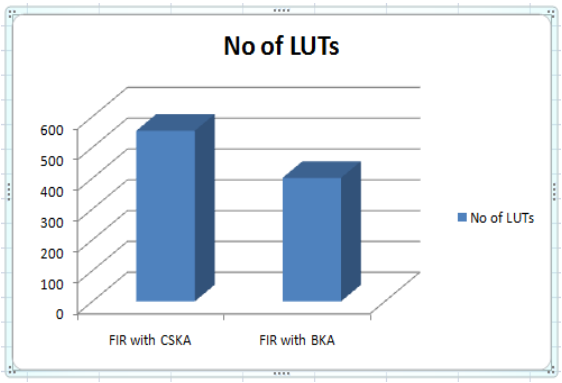

Fig10: LUT comparison bar graph

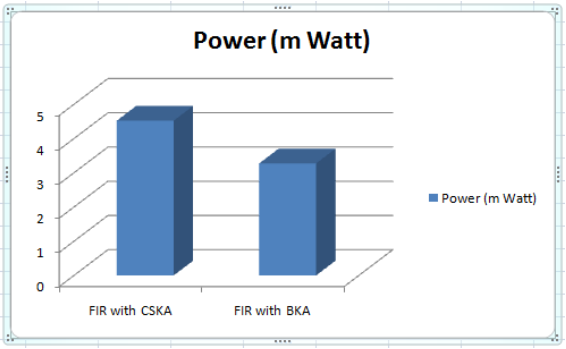

Fig 11: power comparison bar graph

VI. CONCLUSION

In the last two decades, much architecture has been introduced for the design of low complexity fir operation. But there is no such improvement in the FIR design. This project gives the solution for that type of requirements. In traditional filter design methodologies consumes much power due to multiplier.

To avoid this disadvantage this introduces distributive arithmetic method .From the table it can be concluded that the FIR with Brent Kung adder structure occupies less area, and consumes less power compare with the FIR with carry skip adder structure and the experimental results were verified in Xilinx 12.3 ISE Tool.

So from this project it has a chance to use the corresponding structure based on the industrial requirements. In future there may be a chance to develop the layouts for the structures.

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