

High Speed and Low Power VLSI Architecture for Inexact Speculative Adder

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ABSTRACT

This paper presents carry-look ahead adder (CLA) based design of the contemporary inexact-speculative adder (ISA) which is fine grain pipelined to include few logic gates along its critical path. Approximate computing is an efficient approach for error-tolerant applications because it can trade off accuracy for speed. Addition is a key fundamental function for these applications. In this project, proposing with a high speed accuracy-configurable adder. The proposed adder is based on the conventional carry look-ahead adder, and its configurability of accuracy is realized by carry propagation at runtime. Compared with the conventional carry skip adder, the proposed experimental result demonstrates the achievement of the original purpose of optimizing speed simultaneously without reducing the accuracy.

Index Terms—in exact speculative adder, carry look ahead adder, very-large scale-integration (VLSI) and Carry skip adder.

I. INTRODUCTION

Applications that have recently emerged (such as image recognition and synthesis, digital signal processing, which is computationally demanding, and wearable devices, which require battery power) have created challenges relative to power

consumption. Addition is a fundamental arithmetic function for these applications. Most of these applications have an inherent tolerance for insignificant inaccuracies. By exploiting the inherent tolerance feature, approximate computing can be adopted for a tradeoff between accuracy and power. At present, this tradeoff plays a significant role in such application domains.

As computation quality requirements of an application may vary significantly at runtime, it is preferable to design quality configurable systems that are able to tradeoff computation quality and computational effort according to application requirements. The previous proposals for configurability suffer the cost of the increase in power or in delay. In order to benefit such application, a high-speed adder for configurable approximation is strongly required.

In this project, we propose a configurable approximate adder, which consumes lesser power than does with a comparable delay. In addition, the delay observed with the proposed adder is much smaller than that of with comparable power consumption. Our primary contribution is that, to achieve accuracy configurability the proposed adder achieved the optimization of power and delay simultaneously and with no bias toward either.

II. LITERATURE SURVEY

Speculative adders [1] exploit the fact that the typical carry propagation chain of an addition does not span the whole length of the adder, making it possible to estimate an intermediate carry using a limited number of previous stages. Thus, the carry propagation chain, which is the critical path of the adder, can be split in two or more shorter paths, relaxing constraints over the entire design, reducing spurious glitching power, and improving the Energy-Delay-Area Product (EDAP) beyond the theoretical bounds of exact adders.

A number of speculative adders have been proposed in literature with different approaches in order to reduce the error frequency or magnitude. The ETAII adder [2] consists of regular sub-adder blocks with input carries speculated from Carry Look Ahead (CLA) blocks of the same length. In the ETAIIM version, several of the most significant CLA blocks are chained in order to increase accuracy. The ETBA adder [3], direct descendent of the ETAIIM, adds variable speculation signs and sub-adder sum balancing multiplexer blocks to mitigate relative errors.

N. Zhu *et al.* [4] and Y. Kim *et al.* [5] have recently demonstrated adders with improved accuracy by considering two prior carry speculation blocks instead of one, coupled with a carry select (ETAIV) [4] or a carry skip [5] technique, with the latter also using sum balancing over several sub-adder blocks. One room for improvement in the existing speculative adders is that the circuit hardware is not utilized efficiently enough.

Indeed, the overhead due to carry speculation is huge and lies entirely in the

critical path. On the other hand, the sum balancing blocks, containing parallel multiplexers, take also a part in the critical path, require large fan-outs, but are very weakly exploited due to the low probability of incorrect speculations. Thanks to its new speculative path and compensation scheme, the ISA architecture proposed herein greatly improves hardware efficiency upon the state-of-the-art and introduces a new way to control errors.

III. CARRY SKIP ADDER

A **carry-skip adder** (also known as a **carry**) an adder implementation that improves on the delay of a ripple-carry adder with little effort compared to other adders. The improvement of the worst-case delay is achieved by using several carry-skip adders to form a block-carry-skip adder. The worst case for a simple one level carry-ripple-adder occurs, when the propagate-condition is true for each digit pair (a_i, b_i) . Then the carry-in ripples through the n -bit adder and appears as the carry-out after $T_{CRA}(n) \approx n \cdot T_{VA}$.

For each operand input bit pair (a_i, b_i) the propagate-conditions $p_i = (a_i \text{ XOR } b_i)$. Are determined using an XOR-Gate (see). When all propagate-conditions are *true*, then the carry-in bit c_0 determines the carry-out bit the n -bit-carry-skip adder consists of a n -bit-carry-ripple-chain, a n -input AND-gate and one multiplexer. Each propagate bit p_i , that is provided by the carry-ripple-chain is connected to the n -input AND-gate. The resulting bit is used as the select bit of a multiplexer that switches either the last carry-bit c_n or the carry-in c_0 to the carry-out signal c_{out} .

The critical path of a carry-skip-adder begins at the first full-adder, passes through all adders and ends at the sum-bit s_{n-1} . Carry-skip-adders are chained (see block-carry-skip-adders) to reduce the overall critical path, since a single n-bit carry-skip-adder has no real speed benefit compared to a n-bit carry-ripple-adder.

$$\tau_{CSA}(n) = \tau_{CRA}(n)$$

The skip-logic consists of a m-input AND-gate and one multiplexer.

$$T_{SK} = T_{AND}(m) + T_{MUX}$$

As the propagate signals are computed in parallel and are early available, the critical path for the skip logic in a carry-skip adder consists only of the delay imposed by the multiplexer (conditional skip).

$$T_{CSK} = T_{MUX} = 2D.$$

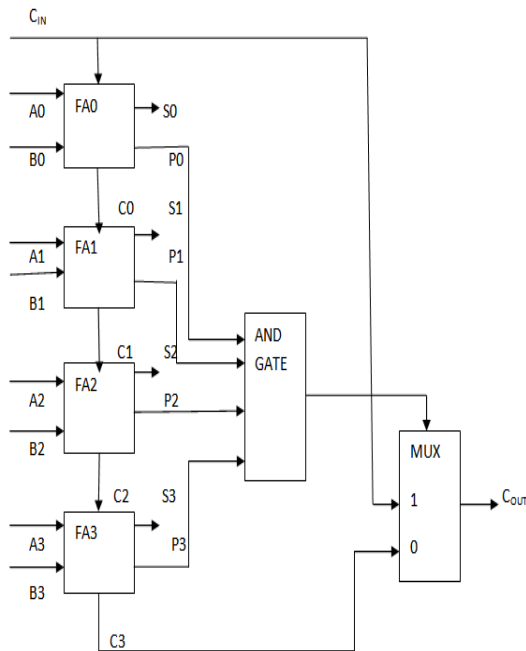


Fig1:4-bit carry skip adder

IV. PROPOSED INEXACT SPECULATIVE ADDER

Arithmetic logic units and digital signal processors widely uses adders. It is the most complicated arithmetic circuits in digital electronics. The existing adders suffer from critical path delay, area overhead and power consumption. Speculative adders are designed with variable latency that combines speculation technique along with correction methodology to attain high performance in terms of low area overhead over the existing adders.

In speculative adders the sum and carry generation part is separated to reduce the area overhead. Inexact speculative adder (ISPA) uses carry predictor circuit to reduce power consumption and to reduce the computational time and it uses error recognition and error correction circuit to find the fault occurred in the partial sum generator and to recover it to get accurate results.

In the recent architectures Speed of operation is the prior factor for digital Adders. So why adders need to be highly optimized for low Power, low Area and low effective cost. For such, Speculative Adders are employed. In the proposed architecture, 'n' bit input info has been given into 4-bit blocks that is the estimation of $x = 4$. Each one of these blocks is fed as operand to the x-bit adders.

The adder unit has been developed with 4 bits carry look ahead adder to be effective in the operation speed. Let

consider two n -bit operands $A = \{A_0, A_1, A_2, \dots, A_{n-1}\}$ and $B = \{B_0, B_1, B_2, \dots, B_{n-1}\}$. During the sum operation, complete carry in and out are expressed as $S = \{S_0, S_1, S_2, \dots, S_{n-1}\}$, C_{in} and C_{out} individually. Speculator block is generally depending on CLA logic to speculate the output carry for every 4-bit adder block. It contains internal carry generator and sum generator blocks which are operated based on equations (1) and (2). The Carry generator, sum generator and multiter designs are shown in figures 1

$$C_g = A_i B_i + B_i C_i + A_i C_i \quad (1)$$

$$S_g = (A_i \text{ xor } B_i) \text{ xor } C_{in} \quad (2)$$

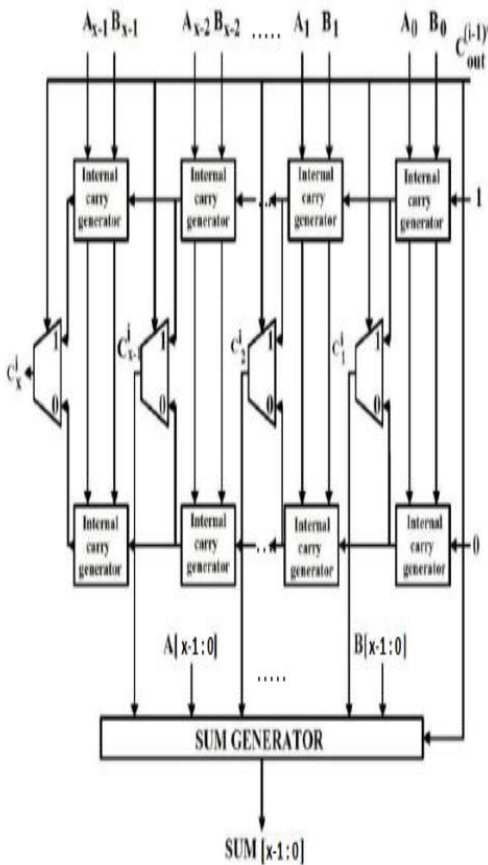


Figure 2: Block diagram of 4bit Speculative adder

V. RESULTS

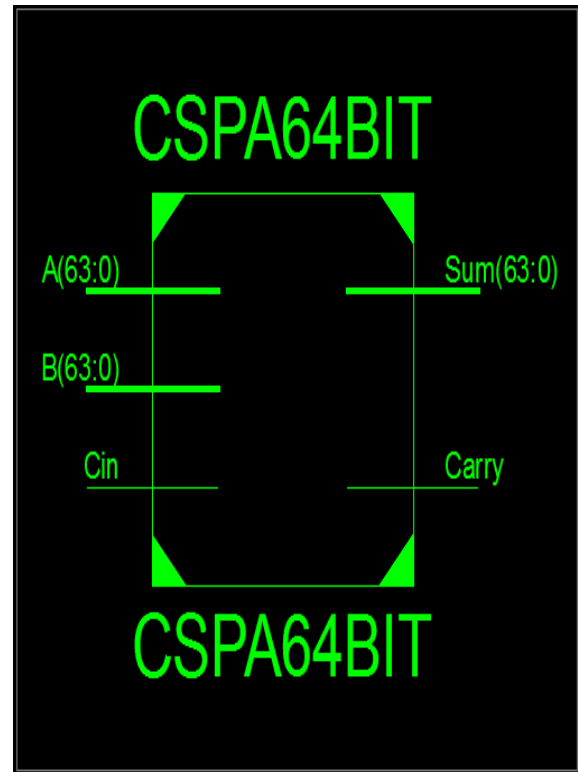


Fig3: RTL schematic view

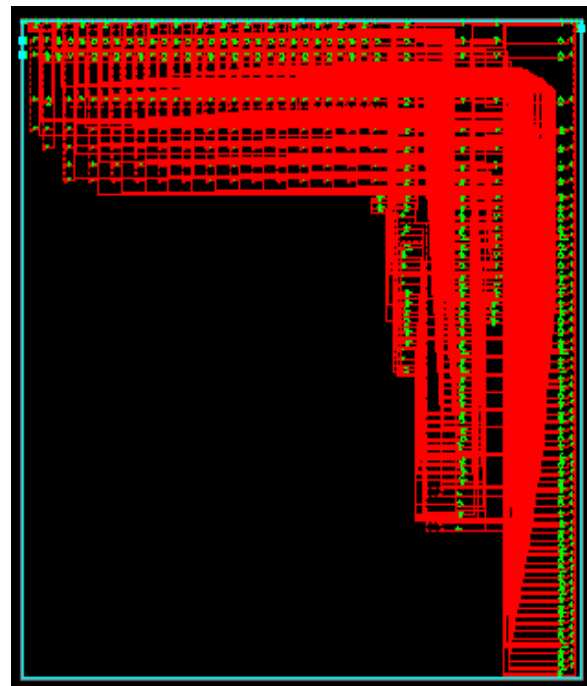


Fig 4: View technology schematic

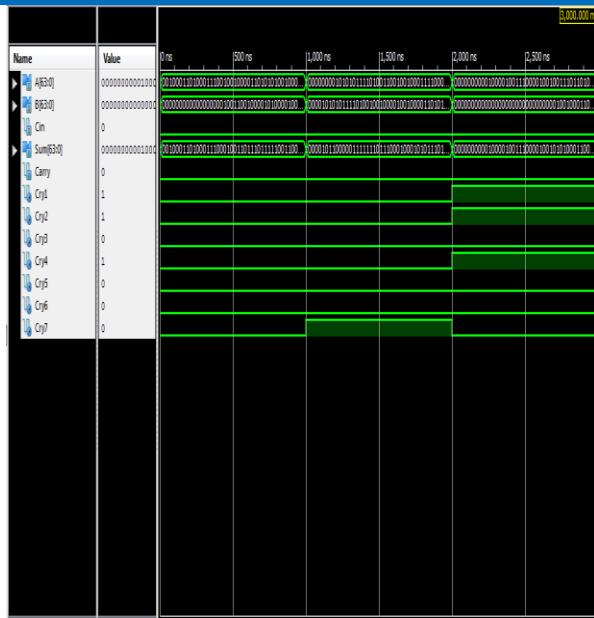


Fig5: simulated wave form

Parameter	CSKA	ISPA
Delay (ns)	103.614	48.411

Table1: Parameter Comparison Table

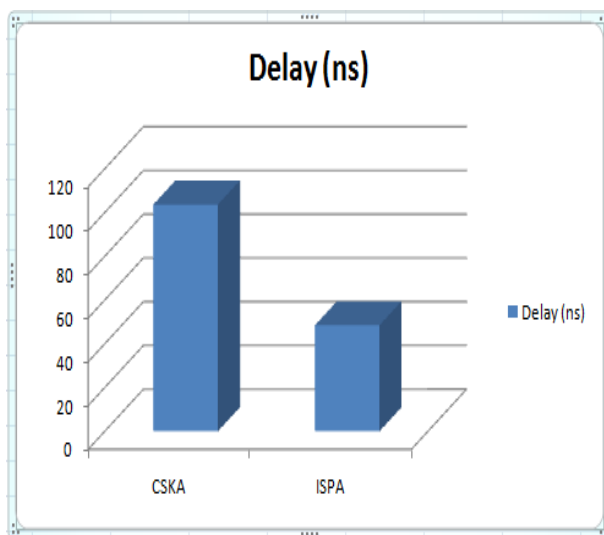


Fig6: Delay Comparison Bar graph

VI. CONCLUSION AND FUTURE SCOPE

In this project, The proposed configurable inexact in exact speculative adder is better than the existing traditional carry skip adder those results are shown in table 1. The proposed adder design based on the conventional Carry Skip Adder, and its configurability of accuracy is realized by carry propagation at runtime. The experimental results demonstrate that the proposed adder had 48.41ns delay and the conventional Carry Skip Adder had 103.614ns delay.

Furthermore, compared with previously studied configurable adders, the experimental results demonstrate that the proposed adder achieves the original purpose of delivering an unbiased optimized result between delay without sacrificing accuracy. Thereby, such design would definitely play significant role in the design of contemporary as well as future electronic devices for IoE and many other contemporary applications. However, the area issue can be resolved to some extent by using lower technology nodes in the design process.

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