International Journal of Research
Available at https://journals.pen2print.org/index.php/ijr/
e-ISSN: 2348-6848
p-ISSN: 2348-795X
Volume 07 Issue 06
June 2020

A Single-Phase Single-Stage Switched-Boost Inverter with Four Switches

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ABSTRACT

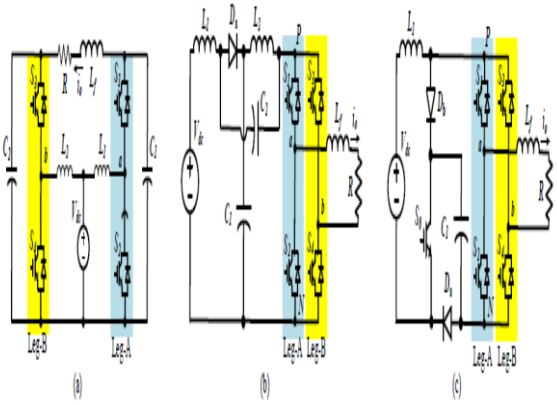
A new single-phase single-stage switched-boost inverter with four switches. Like the quasi-Z-source inverter (qZSI)and quasi-switched boost inverter(qSBI),the proposed inverter has the main features as continuous input current, buck/boost voltage with single-stage conversion and shoot-through immunity. Compared to the qSBI, the proposed inverter uses one more capacitor and one less witch. This paper presents the operating principles, PWM control strategy, parameter design guidelines, and simulation results for the proposed inverter. To verify the performance of the proposed inverter,an800W prototype was built with an 110V/50Hz output voltage in stand-alone and grid-connected modes. The simulation and experimental results matched those of the theoretical analysis.

INTRODUCTION

The traditional voltage source inverters (VSIs) [1]-[3] are a buck DC-AC power conversion, where the DC source voltage is lower than the peak AC output voltage. In addition, both power switches in a leg cannot be turned on at the same time because it causes a short circuit DC voltage source. Furthermore, an additional boost DC-DC converter is inserted in front of the inverter bridge to obtain a high AC output voltage when a low input voltage is used. The result in the additional power converter with two-stage DC-DC-AC power conversion is high cost and low efficiency. To solve the boost voltage problem, a single-stage boost DC-AC inverter was proposed in Fig. 1(a) shows the conventional single-phase single-stage boost inverter. It consists of two inductors, two capacitors, four switches, and a passive load (RLf). The boost inverter utilizes two bidirectional DC-DC boost converters, and the load is differentially connected between the output terminals of the converters. In the boost inverter, both individual boost DC-DC converters are controlled by two 180° phase-shifted dc-biased sinusoidal references to generate a sinusoidal voltage at the output. Because the single-phase boost inverter introduces a low-frequency (LF) ripple current at the source, a current feedback control method is proposed in [6], [7] to mitigate the second-order harmonic current component at the input side. Other single-stage boost inverter topologies were proposed in [8] and [9], where one of the bridge legs is shared with a boost converter. Compared to the single-stage boost inverter in [4], the inverters in [8]-[9] use one less boost inductor. However, the shoot-through state, where both of the power switches in a leg can be turned on at the same time, is forbidden in the single-stage boost inverters [4]-[9], because it will cause a short circuit across the capacitor and damage the devices. A dead time can be inserted into the upper and lower switches in a leg to against the short circuit with increasing the output waveform distortion. Even though the dead time is used, the VSI and boost

inverter may break down due to electromagnetic interference (EMI) which results in shorting of inverter legs. Also, a shoot-through protection scheme was used to solve the shoot-through problem as presented in [10] with increasing the cost. Although the traditional current-source inverters (CSIs) [11], [12] are not affected by the shoot-through situation, they have an open-circuit problem, where both of the power switches in a leg can be turned off at the same time. Moreover, the CSIs are a boost DC-AC power conversion, where the DC source voltage is higher than the peak AC output voltage. For introducing unique free-wheeling inductor current in the open-circuit state of the CSI, an additional switch is used in [13] with increasing the cost.

To overcome both the limitation of the output voltage and the shoot-through (or open-circuit) problem, the Z-source inverter (ZSI) was proposed in [14] for single-stage power conversion. Quasi-Z-source inverters (qZSIs) are proposed in [15]-[17] to reduce the voltage stress on the capacitor and improve the input current profile. Fig. 1(b) shows the single-phase qZSI [15], where a qZS network with two inductors and two capacitors is connected two legs of H-bridge inverter. In the qZSI, a shoot-through state is used to boost voltage without any damages in the power circuit. In one switching period, the number of the shoot-through states is two. Therefore, the operating frequency of the inductors is twice the switching frequency. Because the source voltage is directly connected to the inductor, the input current of the qZSI is continuous. The used Z-network with two inductors and two capacitors in the classic ZS/qZSIs increases the size, weight and cost of the power inverter. To reduce the size, weight and cost of the power inverters, a switched-boost inverter (SBI) is proposed in based on the inverse Watkins–Johnson topology. The SBI with a lower number of passive components also has the same features as the ZSI, where the shoot-through state is used to boost voltage with the single-stage power conversion. To overcome the shortcomings of the classical SBI in [18], a class of quasi-switched boost inverters (qSBIs) are proposed in [19], [20]. In comparison to the conventional SBI [18], the qSBI has the following advantages as increasing the boost factor and improving input profiles. Fig. 1(c) shows the single-phase single-stage qSBI [19]. Compared to the single-phase qZSI and boost inverter, the single-phase qSBI uses one less capacitor and one less inductor, but one more switch and one more diode. The single-phase qSBI has all inherent advantages of the single-phase qZSI including continuous input current, shoot-through immunity and buck-boost output voltage with single stage power conversion. The qSBI has the following advantages over the qZSI [21]: uses one less inductor with a higher inductance and one less capacitor with a lower capacitance; has a lower current rating on both switches and diodes; has a higher boost factor with the same equivalent parasitic effect; and has a higher efficiency



The boost factor of the classical qZSI and qSBI can be expressed as

$$B_z = \frac{V_{PN}}{V_{dc}} = \frac{1}{1-2D}$$

where VPN, D and Vdc are the DC-link voltage across the inverter bridge, the shoot-through duty cycle of each cycle and the input DC voltage, respectively. To improve the boost factor, a switched-

inductor structure [22] and transformer [23], [24] are applied to the qSBI. However, the qSBI has one more active switch than other single-stage boost inverters in [4], [8], [9] and [14]. Similar to the single-phase boost inverters, the single-phase qZSI and qSBI also introduce the low-frequency (LF) ripples in the capacitor voltage and inductor current [21], [25], [26]. To reduce the LF ripple effects of the single-phase ZSI, pulse-width modulation (PWM) control methods is introduced in [27]. A current ripple damping control method is proposed in [28] to minimize the qZS capacitance and inductance of the single-phase qZSI topology. In [29], an active-filter-integrated single-phase qZSI is proposed to remove the LF power ripple at the DC side. In this paper, a new single-phase single-stage switched-boost inverter with four switches is proposed. The proposed inverter benefits from shoot-through immunity over the boost inverters, and it has one less switch and one more capacitor compared to qSBI. In comparison to the qZSI, the proposed inverter uses one more diode and one less inductor. The proposed inverter has all inherent advantages of the qZSI and qSBI as single-stage power conversion, continuous input current, buck/boost voltage and shoot-through immunity. Section II presents operating principles, PWM control strategy, and modelling of the proposed inverter.

THE BUCK CONVERTER

The buck converter is a commonly used in circuits that steps down the voltage level from the input voltage according to the requirement. It has the advantages of simplicity and low cost. Figure 1 shows a buck converter the operation of the Buck converters start with a switch that is open (so no current flow through any part of circuit) When the switch is closed, the current flows through the inductor, slowly at first, but building up over time. When the switch is closed the inductor pulls current through the diode, and this means the voltage at the inductors "output" is lower than it first was. This is the very basic principle of operation of buck circuit.

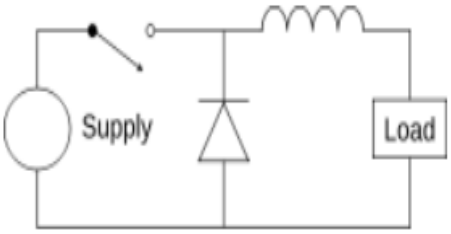


Figure 1: BUCK Converter

Analysis of the buck converter begins by making these assumptions:

1. The circuit is operating in the steady state.
2. The inductor current is continuous(always positive)
3. The capacitor is very large, and the output voltage is held constant at voltage Vo. This restriction will be relaxed later to show the effects of finite capacitance.
4. The switching period is T, the switch is closed for time DT and open for time (1-D)T
5. The components are ideal

The key to the analysis for determining the voltage Vo is to examine the inductor current and inductor voltage first for the switch closed and then for the switch open. The net change in inductor current over one period must be zero for steady state operation. The average inductor voltage is zero. There are two types of operational mode for this circuit.

a) Continuous Conduction Mode and
b) Discontinuous Conduction Mode.

They are described below.

A buck converter operates in continuous mode if the current through the inductor (I_L) never falls to zero during the commutation cycle. In this mode, the operating principle is described by the chronogram in Figure1.

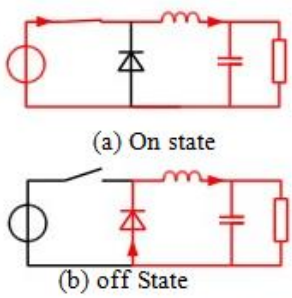


Figure2: Onand off stateof Buck converter

PROPOSED CONVERTER Fig. 2 shows the proposed single-phase single-stage switched-boost inverter with four switches. The switch S0 in the qSBI [see Fig. 1(c)] is replaced by the second H-bridge leg with two switches S3 and S4. As a result, the proposed inverter is reduced one active switch compared to the qSBI. A switched-boost network is a combination of one inductor (L1), one capacitor (C1), two diodes (Da, Db) and four switches. A capacitor Cd filter is used to remove the DC offset component at the output. The output of the inverter is connected to a passive load (RLf). When Da is fully forward-based, a combination of L1-C1-Db-S1-S2 plays a role as a boost converter. When Db is fully forward-based, a combination of L1-C1-Da-S3-S4 plays a role as another boost converter. As a result, two boost converters are integrated to one in the proposed inverter. Compared to the single-phase boost inverter, where two separated boost converters are used, the proposed inverter uses one less inductor and one less capacitor, but two more diodes. As shown in Fig. 2, the negative point of the input voltage source in the proposed topology is floating. This may increase the EMI noise in the proposed inverter. However, the effect of the EMI noise to the proposed inverter can be compensated by the shoot-through and open-circuit immunities.

Operating Principles Unlike the conventional single-phase four-switch inverters, the proposed inverter can operate in the shoot-through state, where both switches in the leg are turned on at the same time. Fig. 3 shows the operating modes in the shoot-through state of the proposed inverter. Mode 1 [see Fig. 3(a)]: S1, S2 and S3 are turned on, while S4♣ is turned off. The inductor L1 is charged through a loop Vdc-L1-S1-S2-Da. The capacitor C1 is discharged. The

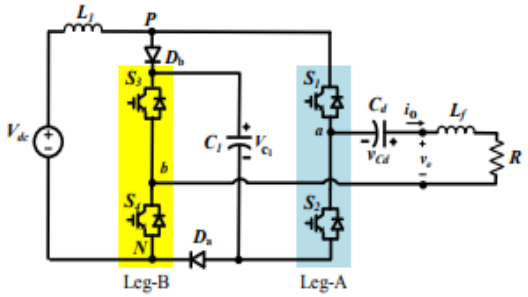


Fig. 2. Proposed inverter with four switches.

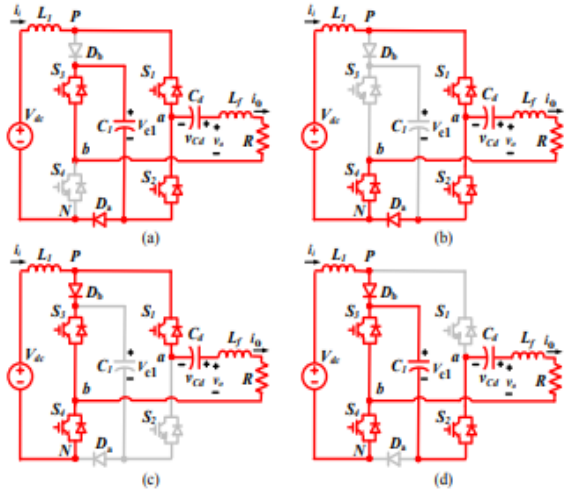


Fig. 3. Operating modes in the shoot-through state. (a) Mode 1, (b) mode 2, (c) mode 3 and (d) mode 4.

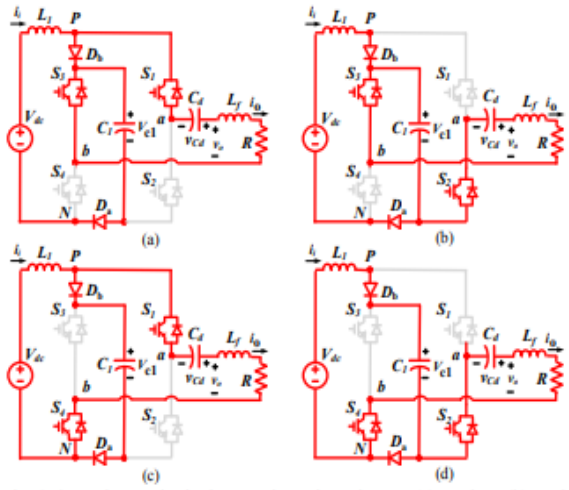


Fig. 4. Operating modes in the non-shoot-through state. (a) Mode 5, (b) mode 6, (c) mode 7 and (d) mode 8.

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inverted voltage, vab, equals a negative capacitor C1 voltage. We have

$$L_1 \frac{di_i}{dt} = V_{dc}.$$

Mode 2 [see Fig. 3(b)]: S1, S2 and S4 are turned on, while S3 is turned off. The inductor L1 is charged as in mode 1. The

TABLE I
SWITCHING STATES OF SEMICONDUCTOR DEVICES

State	Mode	Switch				Diode		v_{ab}
		S_1	S_2	S_3	S_4	D_a	D_b	
Shoot-through	1	On	On	On	Off	On	Off	$-V_{c1}$
	2	On	On	Off	On	On	Off	0
	3	On	Off	On	On	Off	On	0
	4	Off	On	On	On	Off	On	$-V_{c1}$
Non-shoot-through	5	On	Off	On	Off	On	On	0
	6	Off	On	On	Off	On	On	$-V_{c1}$
	7	On	Off	Off	On	On	On	V_{c1}
	8	Off	On	Off	On	On	On	0

capacitor C1 is disconnected. The inverted voltage, vab, equals zero. Mode 3 [see Fig. 3(c)]: S1, S3 and S4 are turned on, while S2♣ is turned off. The inductor L1 is charged through a short-circuit path Db-S3-S4. The capacitor C1 is disconnected. The inverted voltage, vab, is zero. Mode 4 [see Fig. 3(d)]: S2, S3 and S4 are turned on, while S1♣ is turned off. The inductor L1 is charged as in mode 3. The capacitor C1 is discharged. The inverted voltage, vab, equals a negative capacitor C1 voltage. The inductor L1 voltage in modes 2-4 is calculated as (2). Fig. 4 shows the operating modes in the non-shoot-through state of the proposed inverter. Mode 5 [see Fig. 4(a)]: S1 and S3 are turned on, while S2 and♣ S4 are turned off. The inverted voltage, vab, is zero. Mode 6 [see Fig. 4(b)]: S2 and S3 are turned on, while S1 and♣ S4 are turned off. The inverted voltage, vab, equals a negative capacitor C1 voltage. Mode 7 [see Fig. 4(c)]: S1 and S4 are turned on, while S2 and♣ S3 are turned off. The inverted voltage, vab, equals a positive capacitor C1 voltage. Mode 8 [see Fig. 4(d)]: S2 and S4 are turned on, while S1 and♣ S3 are turned off. The inverted voltage, vab, is zero. In modes 5-8, both Da and Db diodes are forward-based. The inductor L1 is charged, while the capacitor C1 is charged, we get

$$L_1 \frac{di_i}{dt} = V_{dc} - V_{C1}.$$

Table I summarizes the switching states of power semiconductor devices in a switching cycle. B. PWM Control Strategy Fig. 5 shows a control strategy for the proposed single-phase single-stage switched-boost inverter. A control waveform, vcontrol, is compared to a high-frequency (HF) triangle waveform, Vtri1, to generate control signals for the S1 and S2 switches in leg-A. Two constant voltages, VSH and -VSH, are compared to Vtri1 to generate the shoot-through control signal. The shoot-through control signal is then inserted into the control signals of switches S1 to S2 through OR logic gates to generate the shoot-through states in leg-A. Likewise, another HF triangle waveform, vtri2 that is shifted in 90 degree from vtri1 is compared to -vcontrol to generate control signals for the S3 and S4 switches in leg-B. Two constant voltages, VSH and -VSH, are

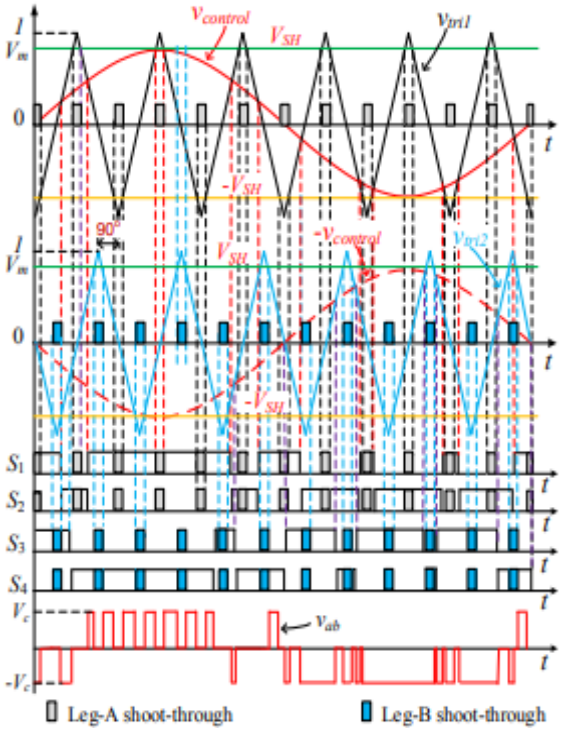

Fig. 5. PWM control strategy for the proposed inverter

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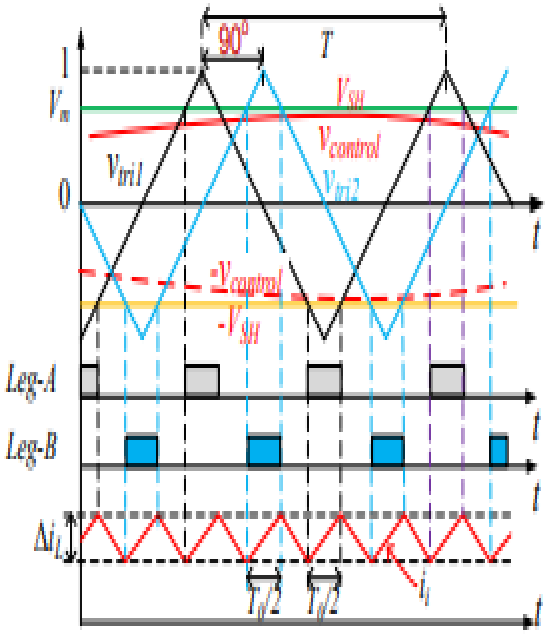

Fig. 6. PWM control strategy for the proposed single-phase switched-boost inverter

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compared to triangle waveform Vtri2 to generate the shoot-through control signal. The shoot-through control signal is then inserted into the control signals of switches S3 to S4 through other OR logic gates to generate the shoot-through states in leg-B. As a result, the number of shoot-through states in one switching period of the proposed inverter is four. With the modulation strategy in Fig. 5, the output voltage of the inverter has three levels (+VC, 0 and -VC). Compared to the conventional PWM strategies, the modified PWM strategy does not have any main advantages.

SIMULATION

A. Simulation Results

To verify the properties of the proposed inverter as shown in Fig. 2, PSIM simulation was performed with the following parameters: L_1 = 2 mH, C_1 = 1360 µF, C_d = 660 µF, L_f = 10 mH, and R = 20 Ω. The switching frequency was 10 kHz and the input voltage was 96 V. Table VII provides a list of the simulation parameters for the proposed inverter. Fig. 9 shows the simulation results for the proposed inverter when V_{dc} = 96 V, M = 0.69 and D = 0.31. From Fig. 9(a), we can see that the capacitor C_1 voltage is boosted to 253 V in the steady state. The average capacitor C_d voltage is 78 V. The RMS output voltage is 120 V, and the RMS output current is 5.9 A. These simulated values match the calculated values in (6), (9) and (11).

Fig. 10 shows the simulation results for the proposed inverter when V_{dc} = 160 V, M = 1 and D = 0. When the input voltage is high enough to produce the desired output voltage, the shoot-through state was not used. The capacitor voltage is 160V in the steady state, and the RMS output current is 5.6 A.

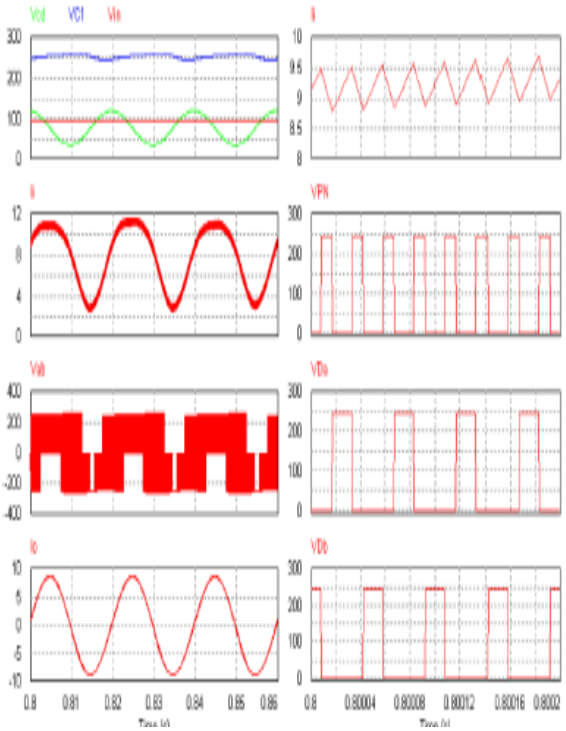

Fig. 9. Simulation results of the proposed inverter when V_{dc} = 96 V, M = 0.69, D = 0.31. From top to bottom: (a) capacitor C_1 voltage, input voltage, capacitor C_d voltage, input current, output voltage v_{ab}, and load current; and (b) input current, DC-link voltage, diode D_a and D_b voltages.

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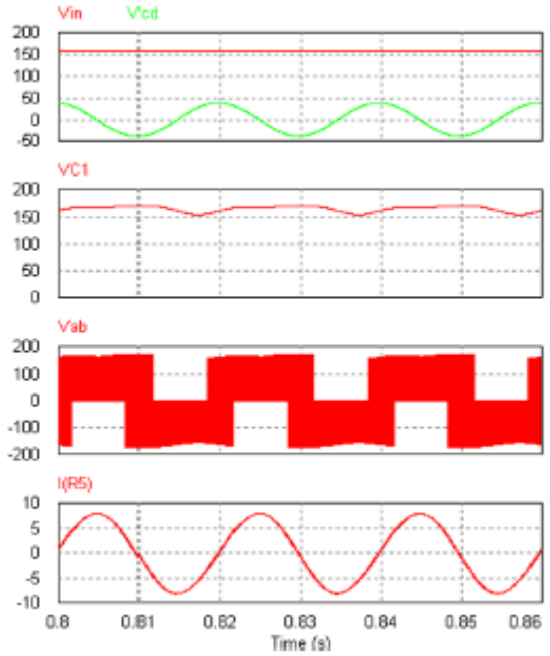

Fig. 10. Simulation results of the proposed inverter when V_{dc} = 160 V, M = 1 and D = 0.From top to bottom: input voltage, capacitor C_{cd} voltage, capacitor C_1 voltage, output voltage v_{ab}, and load current.

B. Experimental Results

We constructed an 800-W laboratory prototype based on a TMS320F28335 DSP to verify the properties of the proposed inverter in both stand-alone and grid-connected modes. The prototype used the parameters as those in the simulation in Table VII. The input voltage is 96 V; and the output voltage is 110 Vrms at 50 Hz. The C_1 capacitor was built by connecting two 680 µF/450-V electrolytic capacitors in parallel, while the C_d capacitor was built by connecting two 330 µF/200-V electrolytic capacitors in parallel.

1) Stand-Alone Mode

Fig. 11 shows the experimental results for the proposed inverter in stand-alone mode when M = 0.69 and D = 0.31. From Fig. 11(a), we can see that the capacitor voltage is boosted to 250 V in the steady state. The measured RMS output voltage is 110 V; and the measured RMS output current is 5.52 A. The peak DC-link voltage is boosted to 250 V and the input current is continuous. The average capacitor C_d voltage is 80 V

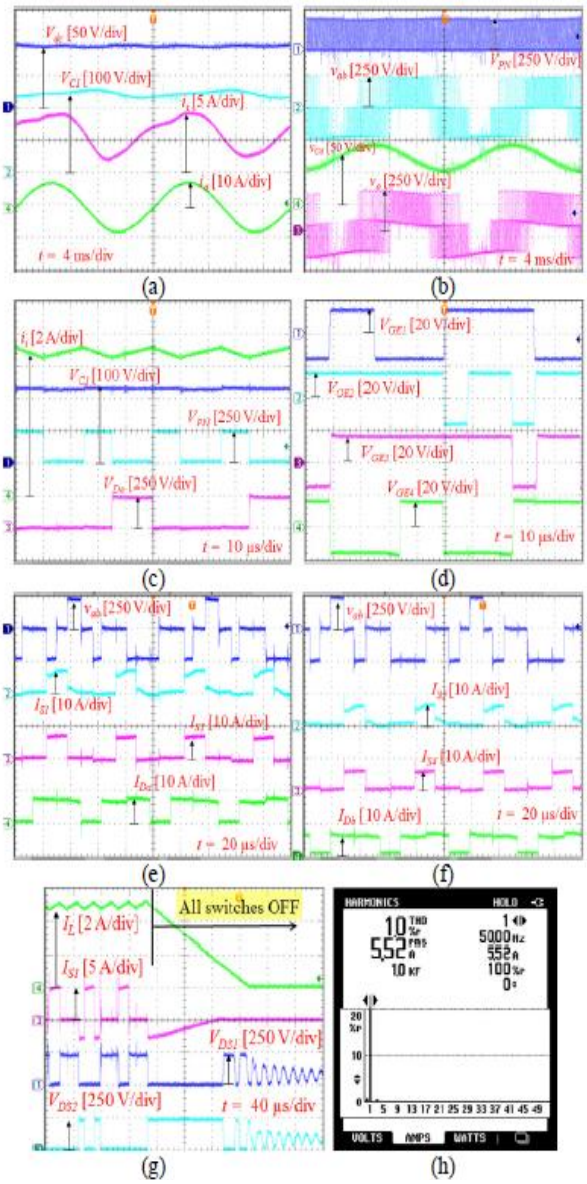

Fig. 11. Experimental results of the proposed inverter in stand-alone mode when V_{dc} = 96 V, M = 0.69, and D = 0.31. From top to bottom: (a) input voltage, capacitor C_1 voltage, input current, and load current; (b) DC-link voltage, output voltage v_{ab}, capacitor C_d voltage, and output voltage on load v_o; (c) input current, capacitor C_1 voltage, DC-link voltage, and diode D_a voltage; (d) control gate signals of S_1~S_4; (e) output voltage v_{ab}, drain-source currents of S_1 and S_2, and diode D_a current; (f)

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Available at https://journals.pen2print.org/index.php/ijr/
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output voltage v_{ab}, drain-source currents of S_3 and S_4, and diode D_b current; (g) harmonics of the output current; and (h) input current, drain-source current of S_1, drain-source voltages of S_1 and S_2 when the open-circuit state occurred suddenly.

with a small disturbance at AC output frequency. The voltage stress on diode D_a is 250 V. The measured values from the experiment are lower than those from the theory and simulation because parasites appeared in the experimental setup. The PWM switching signals for the proposed inverter are shown in Fig. 11(d) at the negative output voltage. Figs. 11(e) and 11(f) show the evidence to justify having three semiconductors in the current loops during the shoot-through state of the proposed inverter. As shown in Fig. 11(e), when all currents of S_1, S_2 and D_a are positive, the output voltage v_{ab} is negative or zero. When all currents of S3, S4 and Db are positive, the output voltage v_{ab} is also negative or zero as shown in Fig. 11(f). Fig. 11(g) shows the harmonics of the output load current that measured through the Fluke 43B power quality analyzer. The measured THD output current is 1.0%. The measured efficiency of the inverter

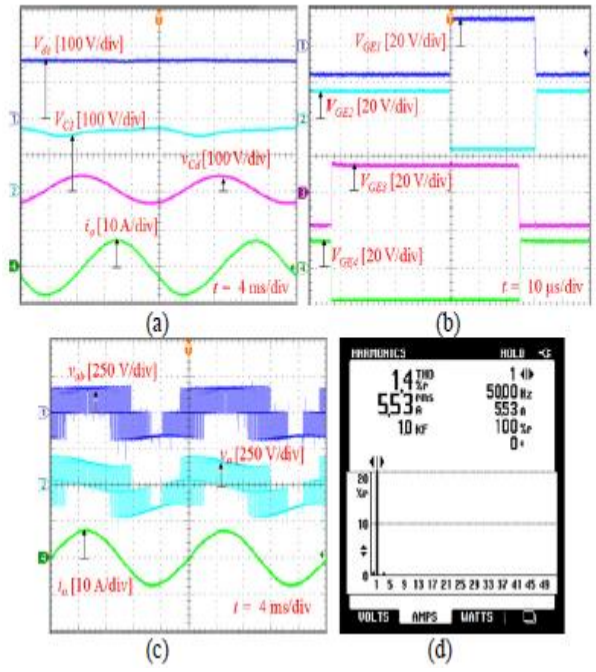

Fig. 12. Experimental results of the proposed inverter when V_{dc} = 160V, M = 1 and D = 0. From top to bottom: (a) input voltage, capacitor C_1 voltage, capacitor C_{cd} voltage and load current; (b) control gate signals of S_1~S_4; (c) output voltage v_{ab}, load voltage v_o, and load current; and (d) harmonics of the output current.

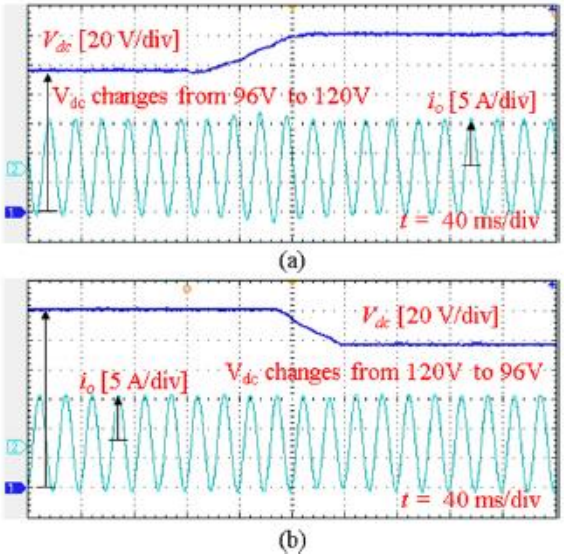

Fig. 13. Experimental results of the proposed inverter when (a) V_{dc} is increased from 96 V to 120 V and (b) V_{dc} is decreased from 120V to 96V. (a)-(b)Top: input voltage and bottom: output current.

is 89.3% at output power of 600 W. Fig. 11(h) shows the experimental results of the proposed inverter when all switches are turned off at the same time suddenly. Before occurring the open-circuit state, the inverter operates in the short-circuit state with D = 0.31. When the open-circuit state occurs, the inductor currents in the inverter free-wheel to the diodes. As shown in Fig. 11(h), the major voltage and current spikes are not appeared on the devices when the open-circuit state occurs suddenly. Therefore, the proposed inverter can operate in either short-circuit state or open-circuit state without causing any damages to the power devices.

Fig. 12 shows the experimental results for the proposed inverter at the buck mode

when V_{dc} = 160 V, M = 1 and D = 0. This mode is used when the input voltage is high enough to produce the desired output voltage. As shown in Fig. 12 (b), the shoot-through state was not used in both two switches on the same leg. The capacitor voltage is the same with the input

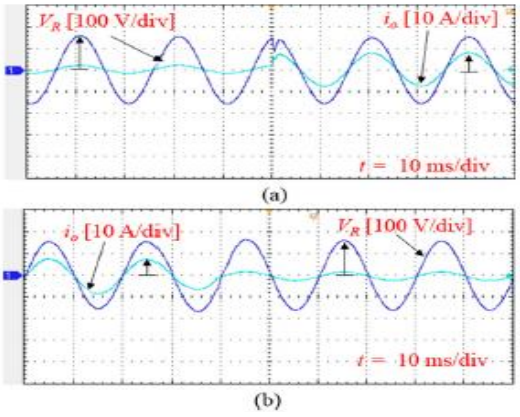

Fig. 14. Experimental results of the proposed inverter when load is changed. (a) Output power is increased from 160 W to 600 W at peak of output voltage and (b) output power is reduced from 600 W to 160 W at zero-crossing of output voltage.

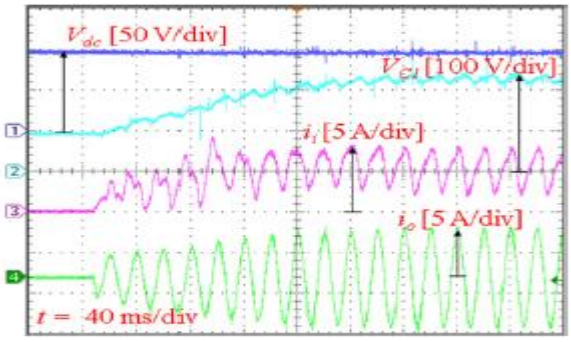

Fig. 15. Experimental results at startup of the proposed inverter. From top to bottom: input voltage, capacitor C_1 voltage, input current and output current.

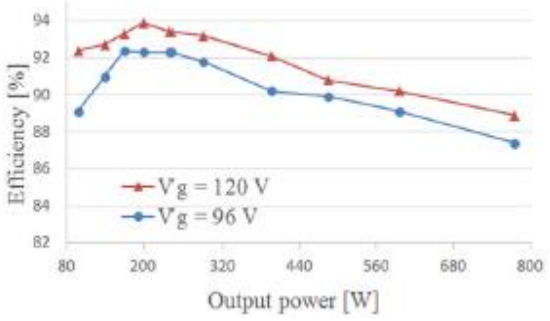

Fig. 16. Measured efficiency versus output power of the proposed inverter.

voltage of 160 V in the steady state; and the measured AC output current is 5.53 Arms. The measured THD output current is 1.4%. The DC-link voltage (VPN) of the proposed inverter is a pulse voltage waveform which its peak value equals to the capacitor C1 voltage. To control the DC-link voltage of the proposed inverter, a simple proportional-integral-derivative (PID) capacitor C_1 voltage regulator is used. Fig. 13 shows the dynamic response of the proposed inverter when the input voltage is changed. As shown in Figs. 13(a) and 13(b), the output current is maintained at 5.5 Arms when the input voltage is suddenly changed from 96V to 120V and vice versa.

Fig. 14 shows the dynamic response of the proposed inverter when the load is suddenly changed. We can see from Fig.14 that the resistor load voltage is kept the resistor load voltage is

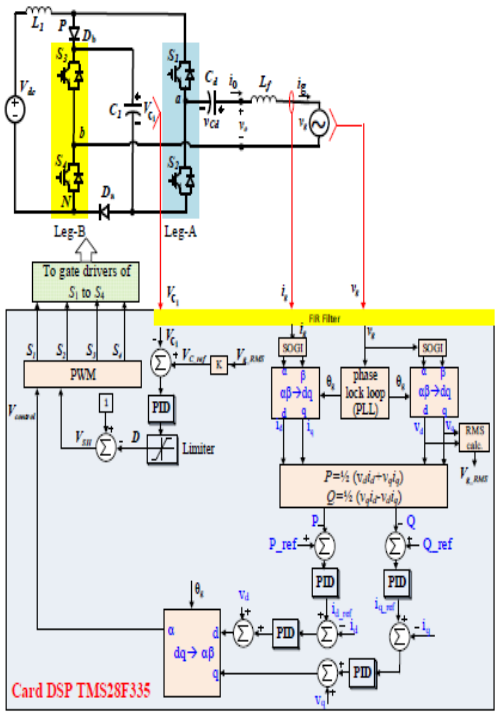

Fig. 17. Proposed single-phase grid-connected inverter with PLL controller.

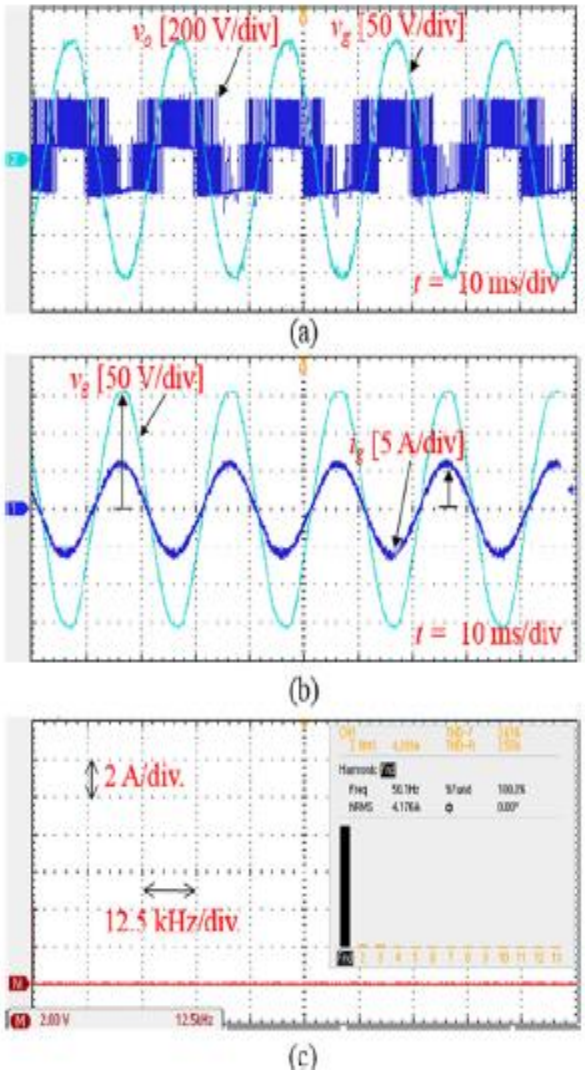

Fig. 18. Experimental results of the proposed inverter in grid-connected mode. (a) Output voltage of the inverter, v_o and grid voltage, v_g under using PLL controller, (b) voltage and current of the grid; and (c) harmonic spectrum of the grid current. kept constant at 110 Vrms, even though the load is changed from 160 W to 600 W and vice versa.

Fig. 15 shows the experimental waveforms of the proposed inverter at startup when M = 0.69. The shoot-through duty cycle is controlled to increase 0 to 0.32 gradually. The startup time of the inverter is 0.27 second.

Fig. 16 shows the measured efficiency of the proposed inverter with different input voltages. The measured efficiency of the proposed inverter is lower than the calculated value. This is because the ripple effects on the inductor current and capacitor voltage are ignored in the calculation.

2) Grid-Connected Mode

Fig. 17 shows the proposed single-phase grid-connected inverter with a phase-locked loop (PLL) controller. The control system is implemented by using DSP TMS320F28335 microcontroller. An filter L_f is used to ensure sinusoidal injected grid current with minimum THD. Three feedback signals v_g, V_C and i_g are filtered by a digital finite impulse response (FIR) filter. A second-order generalized integrator(SOGI) is used to generate the imaginary signal from the real signal (voltage or current) with the same characteristics but shifted 1/4 of period of the real signal. Then, the PLL function block gets the filtered signal of vg to generate synchronization signal. The RMS value of vg is used to calculate the reference capacitor voltage (V_{C_ref}). The PID controller is used to maintain stable output voltage of the inverter through controlling capacitor voltage. By using the dq transformation to estimate the active and reactive power, the active and reactive powers are controlled based on controlling d-q voltage components as shown in Fig. 17.

Fig. 18 shows the experimental results of the proposed inverter in grid-connected mode. Fig. 18(a) shows the output voltage of the inverter and the grid voltage, while Fig. 18(b) shows the voltage and current of the grid. From Fig. 18(b), wecan see that the injected current to the grid (i_g) is sinusoidal. The proposed inverter is tied with the grid at 110 Vrms. As shown in Fig 18(b), the inverter injects a real power of 450 W to the grid with the power factor of 0.99. The measured THD value of the grid current from oscilloscope is 2.61%. The FFT of the grid current are also illustrated in Fig. 18(c).

CONCLUSION

A new single-phase single-stage switched-boost inverter with four switches was proposed in this paper. The proposedinverter has a high reliability because it immunizes both shoot-through and open-circuit phenomenon. In addition, the AC output voltage of the proposed inverter is higher or lower than the DC input voltage. Because the DC capacitor filter is used to remove the DC component of the output voltage, the proposed inverter cannot operate with the capacitive load that the capacitor and resistor connected in series. Compared to the qZS/qSBI, the proposed inverter does not improve the boost voltage ability. Operating principles, analysis, PWM control scheme, parameter design guidelines, and simulation results are presented. The laboratory prototype was built to verify the operating theory of the proposed inverter in stand-alone and grid-connected modes. Like the conventional boost inverter [4], the proposed inverter introduces a LF current at the input. Further research should be carried out to eliminate the LF input current of the proposed inverter.

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