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An Active PWM Technique For A Transformer less H-Bridge Cascaded STATCOM With Wye Configuration

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ABSTRACT:

A transformer less static synchronous compensator (STATCOM) system based on multilevel H-bridge converter with wye configuration. This pwm technique holds two control strategies i.e. the current loop control and the dc capacitor voltage control. With regards to the current loop control, a nonlinear controller based on the passivity-based control (PBC) theory is used in this cascaded structure STATCOM for the first time. As to the dc capacitor voltage control, overall voltage control is realized by adopting a proportional resonant controller. Clustered balancing control is obtained by using an ac- tive disturbances rejection controller. Individual balancing control is achieved by shifting the modulation wave vertically which can be easily implemented in a field-programmable gate arrays or by digital signal processors with addition to pwm .the simulation results for al H-bridge cascaded STATCOMs rated at 10 kV 2 MVA are presented below with effective maintainance of dc capacitor voltage.

IndexTerms—
Active disturbances rejection controller (ADRC); H-bridge cascaded; passivity-based control (PBC); proportional resonant (PR) controller; shifting modulation wave; static syn- chronous compensator (STATCOM)

I .INTRODUCTION

Flexible ac transmission systems (FACTS) are being in- creasingly used in power system to enhance the system utilization, power transfer capacity as well as the power quality of ac system interconnections [1], [2]. As a typical shunt FACTS device, static synchronous compensator (STATCOM) is utilized at the point of common connection (PCC) to absorb or inject the required reactive power, through which the voltage quality of PCC is improved [3]. In recent years, many topologies have been applied to the STATCOM. Among these different types of topology, H-bridge cascaded STATCOM has been widely ac- cepted in high-power applications for the following advantages: quick response speed, small volume, high efficiency, minimal interaction with the supply grid and its individual phase control ability [4]–[7]. Compared with a diode-clamped converter or flying capacitor converter, H-bridge cascaded STATCOM can obtain a high number of levels more easily and can be con- nected to the grid directly without the bulky transformer. This enables us to reduce cost and improve performance of H-bridge cascaded STATCOM [8].

There are two technical challenges which exist in H-bridge cascaded STATCOM to date. First, the control method for the current loop is an important factor influencing the compen- sation performance. However, many nonideal factors, such as the limited bandwidth of the output current loop, the time de- lay induced by the signal detecting circuit, and the reference command current generation process, will deteriorate the com- pensation effect. Second, H-bridge cascaded STATCOM is a complicated system with many H-bridge cells in each phase, so the dc capacitor voltage imbalance issue which caused by dif- ferent active power losses among the cells, different switching patterns for different cells, parameter variations of active and passive components inside cells will influence the reliability of the system and even lead to the collapse of the system. Hence, lots of researches have focused on seeking the solutions to these problems.

In terms of current loop control, the majority of approaches involve the traditional linear control method, in which the non- linear equations of the STATCOM model are linearized with a specific equilibrium. The most widely used linear control schemes are PI controllers [9], [10]. In [9], to regulate reac- tive power, only a simple PI controller is carried out. In [10], through a decoupled control strategy, the PI controller is em- ployed in a synchronous *d*–*q* frame. However, it is hard to find the suitable parameters for designing the PI controller and the performance of the PI controller might degrade with the external disturbance. Thus, a number of intelligent methods have been proposed to adapt the PI controller gains such as particle swarm optimization [11], neural networks [12], and artificial immu- nity [13]. In literature [14], [15], adaptive control and linear robust control have been reported for their antiexternal distur- bance ability. In literature [16], [17], a popular dead-beat current controller is used. This control method has the high bandwidth and the fast reference current tracking speed. The steady-state performance of H-bridge cascaded STATCOM is improved,but the dynamic performance is not improved. In [18], a dc injec- tion elimination method called IDCF is proposed to build an extra feedback loop for the dc component of the output current. It can improve the output current qulity of STATCOM. How- ever, the circuit configuration of the cascaded STATCOM is the delta configuration, but not the star configuration. Moreover, an adaptive theory-based improved linear sinusoidal tracer control method is proposed in [19] and a leaky least mean square-based control method is proposed in [20]. But these methods are not for STATCOM with the cascaded structure. By using the tradi- tional linear control method, the controller is characterized by its simple control structure and parameter design convenience, but poor dynamic control stability.

Other control approaches apply nonlinear control which di- rectly compensate for the system nonlinearities without requir- ing a linear approximation. In [21], an input–output feedback linearization controller is designed. By adding a damping term, the oscillation amplitude of the internal dynamics can be ef- fectively decreased. However, the stability cannot be guaran- teed [22]. Then, many new modified damping controllers are designed to enhance the stability and performance of the inter- nal dynamics [23]–[26]. However, the implementation of these controllers is very complex. To enhance robustness and simplify the controller design, a passivity-based controller (PBC) based on error dynamics is proposed for STATCOM [27]–[30]. Fur- thermore, the exponential

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stability of system equilibrium point is guaranteed. Nevertheless, these methods are not designed on the basis of STATCOM with the H-bridge cascaded structure and there are no experimental verifications in these literatures.

In terms of dc capacitor voltage balancing control, there are three pivotal issues: overall voltage control, clustered balancing control, and individual balancing control. In literature [31], under the asumption of all dc capacitors being equally charged and balanced, they can only eliminate the imbalances caused by the inconsistent drive pulses without detecting all dc capacitor voltages. In [32]–[34], additional hardware circuits are required in the methods based on ac bus energy exchange and dc bus en- ergy exchange, which will increase the cost and the complexity of the system. In [35], a method based on zero-sequence volt- age injection is proposed and it will increase the dc capacitor voltage endurance capacity. On the contrary, the method using negative-sequence current in [36] does not need the wide mar- gin of dc capacitor voltage, but the function of STATCOM is limited. In [8], the active power of the individual phase clus- ter is controlled independently, while the circuit condition is considered to be limited in practical use. In [37] and [38], a cosine component of the system voltage is superposed to the clustered output voltage, but it is easy to be affected by an inacurate phase-locked loop (PLL). In [39], the active voltage vector superposition method is proposed. However, the simu- lated and experimental results do not show the differences in control area and voltage ripple. The selective harmonic elim- ination modulation method is used in [40] and [41], in which dc voltage balancing control and low-frequency modulation are achieved. Compared with the method in [40] and [41], a method changing the phase-shift angle for dc voltage balancing control is proposed in [42] and [43], through which the desirable effect can be easily achieved, whereas it is limited by the capacity of STATCOM. In [44], the dc voltage and reactive power are con- trolled. However, it cannot be widely used due to fact that many nonideal factors are neglected. In [45] and [46], the proposed method assumes that all cells are distributed with equal reactive power and it uses the cosine value of the current phase angle. It could lead to system instability, when using the zero-crossing point of the cosine value. In [47] and [48], the results of experi- ments are obtained in the downscaled laboratory system. Thus, they are not very persuasive in this condition.

In this paper, a new nonlinear control method based on PBC theory which can guarantee Lyapunov function dynamic stabil- ity is proposed to control the current loop. It performs satis- factorily to improve the steady and dynamic response. For dc capacitor voltage balancing control, by designing a proportional resonant (PR) controller for overall voltage control, the control effect is improved, compared with the traditional PI controller. Active disturbances rejection controller (ADRC) is first pro- posed by Han in his pioneer work [49], and widely employed in many engineering practices [50]–[53]; furthermore, it finds its new application in H-bridge cascaded STATCOM for clustered balancing control. It realizes the excellent dynamic compensa- tion for the outside disturbance. By shifting the modulation wave vertically for individual balancing control, it is much easier to be

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realized in field-programmable gate array (FPGA) compared with existing methods. Two actual H-bridge cascaded STAT- COMs rated at 10 kV 2 MVA are constructed and a series of verification tests are executed. The experimental results have verified the viability and effectiveness of the proposed control methods

II. CONFIGURATION OF 2MVA STATCOM SYSTEM

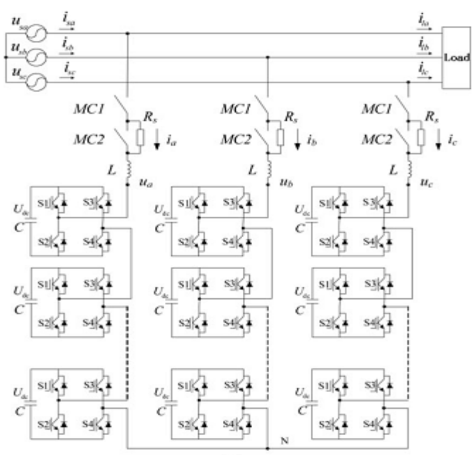

Fig.1. Configuration Of Experimental System

Fig. 1 shows the circuit configuration of the 10 kV 2 MVA star-configured STATCOM cascading 12 H-bridge pulse width modulation (PWM) converters in each phase and it can be ex- panded easily according to the requirement. By controlling the current of STATCOM directly, it can absorb or provide the required reactive current to achieve the purpose of dynamic re- active current compensation. Finally, the power quality of the grid is improved and the grid offers the active current only.

The power switching devices working in ideal condition is assumed. u_{sa} , u_{sb} , and u_{sc} are the three-phase voltage of grid. u_a , u_b , and u_c are the three-phase voltage of STATCOM. i_{sa} , i_{sb} , and i_{sc} are the three-phase current of grid. i_a , i_b , and i_c are the three-phase current of STATCOM. i_{la} , i_{lb} , and i_{lc} are the three-phase current of load. U_{dc} is the reference voltage of dc capacitor. C is the dc capacitor. L is the inductor. R_s is the starting resistor.

Table I summarizes the circuit parameters. The cascade num- ber of $N = 12$ is assigned to H-bridge cascaded STATCOM, re- sulting in 36 H-bridge cells in total. Every cell is equipped with nine isolated electrolytic capacitors which the capacitance is 5600 μF. The dc side has no external circuit and no power source except for the dc capacitor and the voltage sensor. In each cluster, an ac inductor supports the difference between the voltage of the grid and the ac PWM voltage of STATCOM. The ac inductor also plays an important role in filtering out switch ripples caused by PWM. For selecting insulated-gate bipolar transistor (IGBT), considering the complexities of prac- tical industrial fields, there might be the problems of the spike current and over load. Consequently, in order to ensure the sta- bility and reliability of H-bridge cascaded STATCOM, and also improve the over load capability, the current rating of the se- lected IGBT should be reserved enough safety margin. In the proposed system, 1.4 times rated current operation is guaran- teed, the peak current under the 1.4 times over load condition is224 A, the additional 76 A (30− 224 A = 76 A) is the safetymargin of IGBT modules. Due to the previous considerations,the voltage and current ratings of IGBT which is selected as the switching element in main circuit are

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1.7kVand 300 A (Infineon EF300R17KE3).

The modulation technology adopts the carrier phase-shifted sinusoidal PWM (abbreviated as CPS-SPWM) with the carrier frequency of 1 kHz. Then, with a cascade number of $N = 12$, the ac voltage cascaded results in a 25-level waveform in line to neutral and a 49-level waveform in line to line. In each cluster,12 carrier signals with the same frequency as 1 kHz are phase shifted by $2\pi/12$ from each other. When a carrier frequency is as low as 1 kHz, using the method of phase-shifted unipolar sinusoidal PWM, it can make an equivalent carrier frequency as high as 24 kHz. The lower carrier frequency can also reduce the switching losses to each cell.

III.CONTROL ALGORITHM

Fig. 3 shows a block diagram of the control algorithm forH-bridge cascaded STATCOM.The whole control algorithmmainly consists of four parts, namely, PBC, overall voltagecontrol, clustered balancing control, and individual balancing control. The first three parts are achieved in DSP, while the last part is achieved in the FPGA.

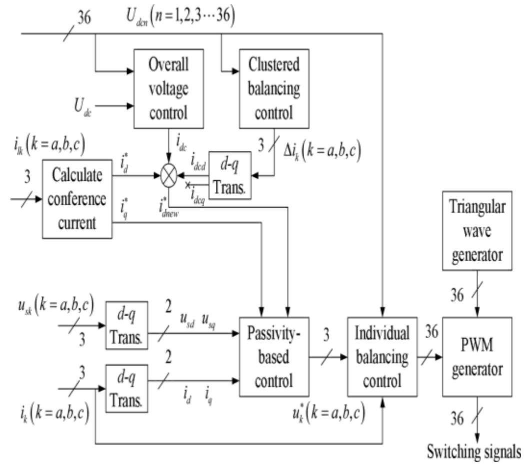

Fig. 2. Control block diagram for the 10 kV 2 MVA H-bridge cascaded STATCOM

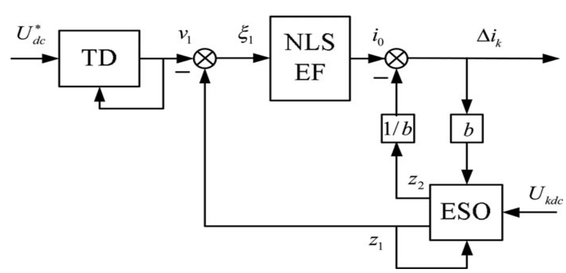

Fig. 3. Block diagram of PBC.

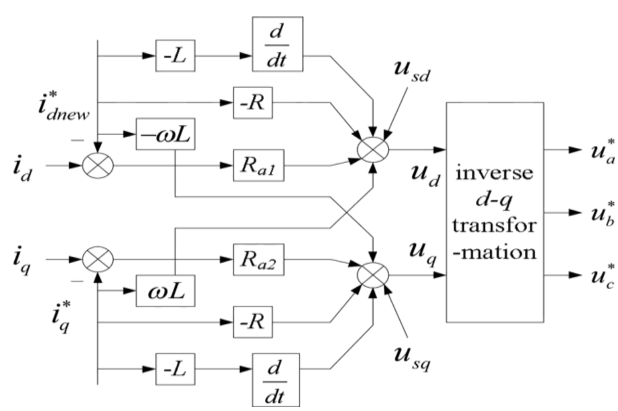

Fig. 4. Block diagram of clustered balancing control

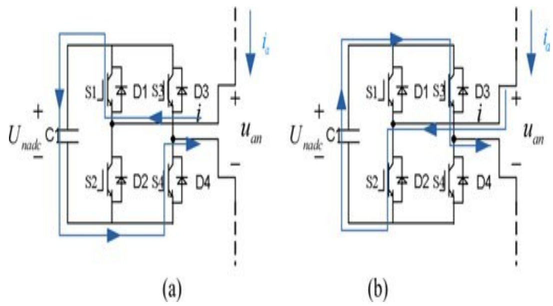

Fig. 5. Charging and discharging states of one cell. (a) Charging state. (b) Discharging state.

As shown in Fig. 5, at some point, the direction of the current is from the grid to STATCOM. If S1 and S4 are open, the output voltage of the *n*th cell is positive. The current flows into the dc capacitor along the direction which is shown in Fig. 5(a) and charges the capacitor. Likewise, if S2 and S3 are open, the output voltage of the *n*th cell is negative. The current flows into the dc capacitor along the direction which is shown in Fig. 5(b) and discharges the capacitor. Obviously, to make the capacitor voltage of each cell tend to be consistent, the turn- on time of the cell with the lower voltage should be extended and the turn-on time of the cell withthe higher voltage should be shortened in charging state. Then, in discharging state, the process is contrary. The adjustment principle of the dc capacitor voltage can be summarized as follows.

1) When $(i_a \times u_{an}) > 0$, if $U_{na\,dc} < U_{a\,dc}$, it needs to in-crease the duty cycle. If $U_{na\,dc} > U_{a\,dc}$, it needs to reducethe duty cycle.

2) When $(i_a \times u_{an}) < 0$, if $U_{na\,dc} > U_{a\,dc}$, it needs to in-crease the duty cycle. If $U_{na\,dc} < U_{a\,dc}$, it needs to reducethe duty cycle.

i_a is output current of a-phase cluster. u_{an} is ac output voltage of the *n*th ($n =$ 1, 2, $\cdots$, 12) cell of a-phase cluster. $U_{a\,dc}$ is the dcmean voltage of 12 cascaded converter cells in a-phase cluster. $U_{na\,dc}$ is the capacitor voltage of the *n*th cell of a-phase cluster. According to the previous method, the direction and the mag- nitude of adjustment of the duty cycle for one cell can be achieved easily at some point.

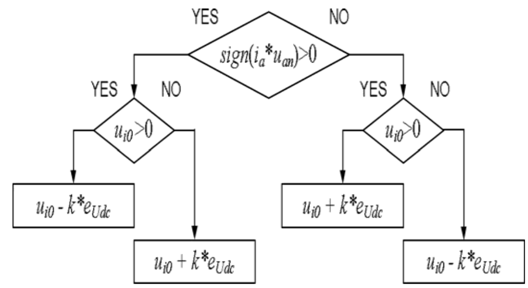

Fig. 6 Flowchart of shifting modulation wave.

The previous principle is also suitable for reducing discharg- ing time and prolonging the charging and discharging times of the cell. Summing up the previous analysis, the method can beillustrated as follows.

1) If the requirement is to reduce the duty cycle, it needs to shift down the normal modulation wave and shift up the opposite modulation wave.

2) If the requirement is to prolong the duty cycle, it needs to shift up the normal modulation wave and shift down the opposite modulation wave.

The value of shifting is decided by $k * e_{U\,dc}$ and the flowchartis shown in Fig. 6.

The previous method is the modulation strategy that is based on CPS-SPWM in this paper and it is very easy to be realized in the FPGA. But, it is not to say that this method must be used like this only. In order to regulate the duty cycle, as long as the pulse signal is achieved by comparing the modulation wave with the carrier, the modulation strategy is able to use this method. The implementation block diagram of the individual balancing control method is shown in Fig. 7

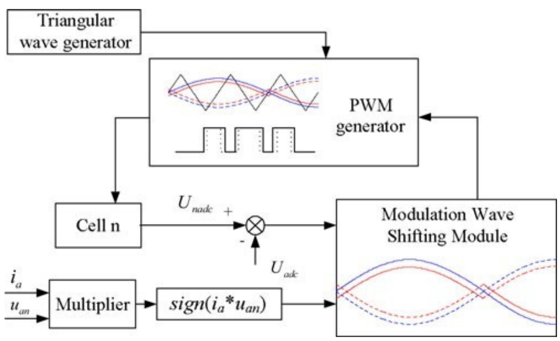

Fig. 7. Block diagram of individual balancing control.

IV. SIMULATION RESULTS

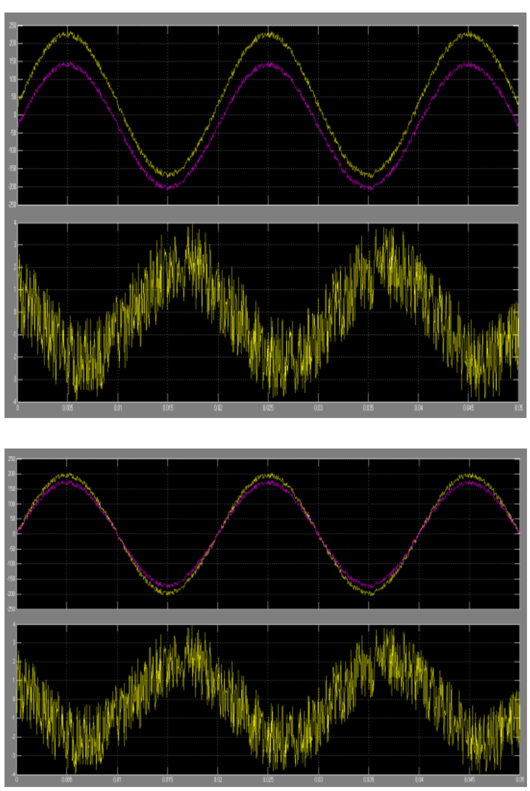

Fig. 8. Experimental results verify the effect of PBC in steady-state process. (a) Ch1: reactive current; Ch2: compensating current; Ch3: residual current of grid. (b) Ch1: reactive current; Ch2: compensating current; Ch3: residual current of grid.

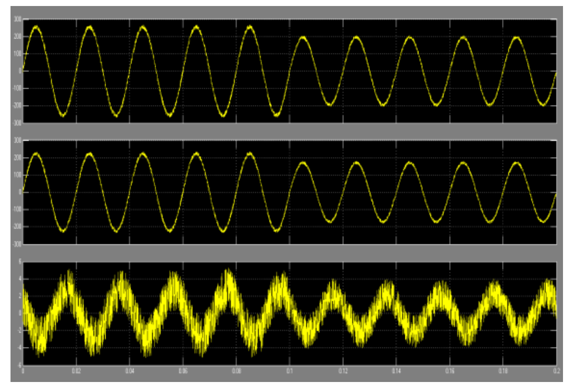

Fig. 9. Experimental results show the dynamic performance of STATCOM in the dynamic process. Ch1: reactive current; Ch2: compensating current; Ch3: residual current of grid

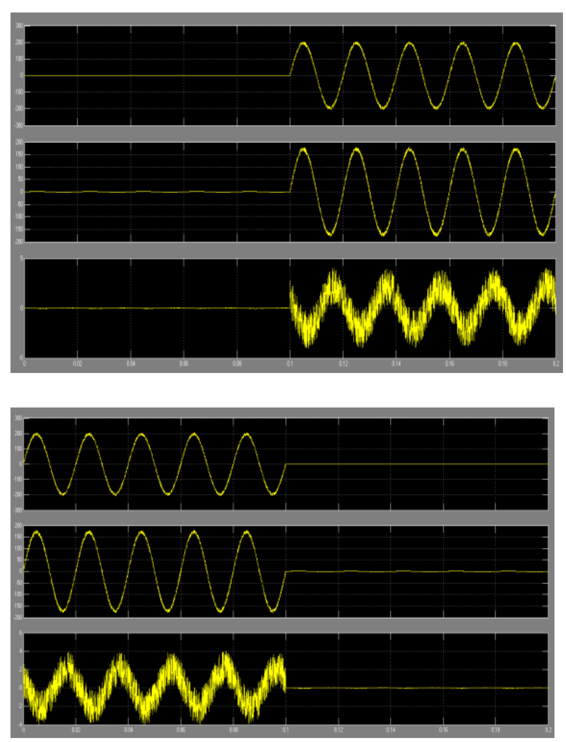

Fig. 10. Experimental results in the startup process and stopping process. (a) Ch1:

reactive current; Ch2: compensating current; Ch3: residual current of grid. (b) Ch1: reactive current; Ch2: compensating current; Ch3: residual current of grid.

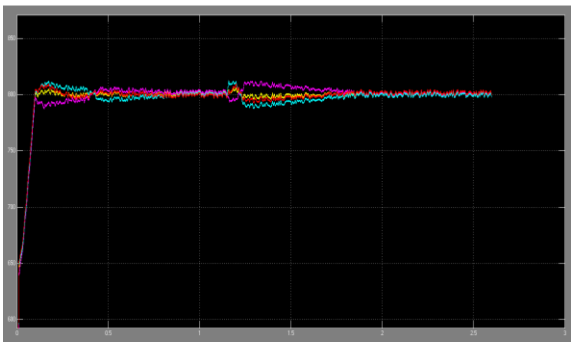

Fig. 11. Experimental waveforms for testing clustered balancing control in the startup process and dynamic process. (a) DC mean voltage of all converter cells *U* ∗dc ; dc mean voltage *Uk* dc (*k = a, b, c*) of 12 cascaded converter cells in each cluster.

V.CONCLUSION

This paper has analyzed the fundamentals of STATCOM based on multilevel H-bridge converter with star configuration. And then, the actual H-bridge cascaded STATCOM rated at10 kV 2 MVA is constructed and the novel control methods are also proposed in detail. The proposed methods has the following characteristics.

1) A PBC theory-based nonlinear controller is first used in STATCOM with this cascaded structure for the current loop control, and the viability is verified by the experi- mental results.

2) The PR controller is designed for overall voltage control and the experimental result proves that it has better per- formance in terms of response time and damping profile compared with the PI controller.

3) The ADRC is first used in H-bridge cascaded STATCOM for clustered balancing control and the experimental re- sults verify that it can realize excellent dynamic compen- sation for the outside disturbance.

4) The individual balancing control method which is realized by shifting the modulation wave vertically can be easily implemented in the FPGA.

The Simulation results have confirmed that the proposed methods are feasible and effective. In addition, the findings of this study can be extended to the control of any multilevel voltage source converte especially those with H-bridge cascaded structure.

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