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Vlsi Modelling of Efficient Carry Select Adder with Redundant Encoding Technique

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Abstract—
Carry Select Adder (CSLA) is one of the best adders used in many data-processing processors to perform fast arithmetic functions. From the structure of the CSLA, it is obvious that there is possibility for reducing the area and power consumption in the CSLA. CSLA is used in numerous computational systems to easy the problem of carry propagation delay (CPD) by autonomously generating multiple carries and then select a carry to produce the sum. However, the CSLA is not area competent because it uses several pairs of Ripple Carry Adders (RCA) to generate partial sum and carry by in view of carry input Cin=0 and Cin=1, then thefinal-sum and carry are selected by the multiplexers (MUX).Since the CSLA suffering with Redundancy problem this paper presented a novel technique to eliminate all the redundant logic operations present in the traditional CSLA and proposed a new encoding technique for CSLA. In this encoding technique the carry selection operation is done earlier than the final sum generation. This is unlike from the traditional approach. The Bit patterns of two anticipating carry words (Cin = 0 and 1) and fixed Cin bits are used for logic optimization of CS and CG units. The optimized logic units improve the efficiency of CSLA design.Due to the small carry-output delay, the proposed CSLA design has aconsiderably less area and delay than the recently proposed CSLA's.The proposed design is simulated, synthesized and verified by Xilinx tools along with Virtex – 5 FPGA board.

Index Terms —
RCA; CSLA;Square-root CSLA; Xilinx tools and Virtex -5 FPGA.

I. INTRODUCTION

Adders are of essential substance in a wide variety of digital systems. Many fast adders exist, but adding fast using low area and power is still challenging. Due to the fast growing mobile industry not only the faster arithmetic unit but also less area and low power arithmetic units are needed.The performance of a DSP processors is depends up on the adder efficiency. The importance of a fast, low-cost binary adder in a digital system is difficult to miscalculate. Not only are adders used in every arithmetic operation, they are also needed for computing the physical address in virtually every memory Fetch operation in most modern CPUs. Ripple CarryAdders are the smallest but also the slowest. More recently, carry-skip adders, Carry-look-ahead and carry-select adders are very fast but far larger and consume much more power than ripple or carry-skip adders In the case of digital adders, the speed ofaddition is inadequate by the time required by the carryto propagate through the adder which is known aspropagation delay time. The sum for each bit in anadder is generated in succession only after thepreceding bits have been summed and a carry isobtained to the next position. The carry select adderis used in many digital computational systems toreduce the difficulty of propagation delay. It can bedone by in parallel generation of multiple carriesand then select a carry to generate the sum.

Yet, the CSLA is not competent in the case ofarea because it uses multiple pairs of Ripple CarryAdders (RCA) to generate partial sum and carry byconsidering carry input Cin=0 and Cin=1alone, then the final-sum and carry are selectedby the multiplexer . In the case of MCSLAthe basic idea is to use Binary to Excess-1Converter (BEC) instead of RCA with Cin = 1 inthe regular CSLA to achieve lower area and powerconsumption The main benefit of this BEC logiccomes from the lesser number of logic gates thanthe n-bit Full Adder (FA) structure.

Practical studies are observed that logicoptimization largely depends on ease of use of outmoded operationsin the formulation, whereas adder delays mainly a function of data dependence. In the active designs, logic is optimizedwithout giving any contemplation to the data dependence. Hence it is proposed to make an examination on logic operations involved inconventional and BEC-based CSLAs to swot the data dependenceand

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to identify redundant logic operations. Based on thisexamination, a logic formulation for the CSLA can be suggested.The main role in this concern is to formulae logic basedon data dependence and optimized carry generator CG andCS designBecause of all the units are logic optimized, the proposed CSLA may involves appreciably less ADP thanthe active CSLAs.

The rest of this brief is organized as follows.Design developmentis presented in Section II.Modelling of proposed CSLA to overcome redundancyis presented in sectionIII.Simulation and synthesis results are presented in Section IV.Andthe conclusion is given in Section V.

II. DESIGN DEVELOPMENT

To promote low power high performance applications of computing architectures, varioushigh speed Techniques are modeled on VLSI. The VLSI architecture for the proposed method has implemented as follows.

It is very familiar that the CSLA has two major entities and they aresum and carry generatorunit (SCG) and the sum and carry selection unit (SCS). TheSCG unit consumes most of the logic utilities of CSLA andconsiderably contributes to the critical path. Meanwhile various logicdesigns have been recommended for competentexecution of theSCG unit.Therefore certain exercise is needed before implementing the techniques to the practical world. The main intention of this exercise is to recognize the redundant logic operations and data dependence. As a result,we avoided all redundant logic operations andsequence logic operations based on their data dependence.

TABLE 1
SUMMARY OF DESIGN CONSIDERATIONS

S.no	Design consideration	Selection
1	Compiler	Xilinix14.1Vivado
2	Programming Language	Verilog
3	FPGA	Virtex -5
4	Interface	Digilent USB cable
5	simulator	Xilinx ISIM
6	Synthesizer	Xilinx ISE14.1- XST

III. MODELING OF PROPOSED CSLA TO OVERCOME REDUNDANCY

Conventional CSLA:

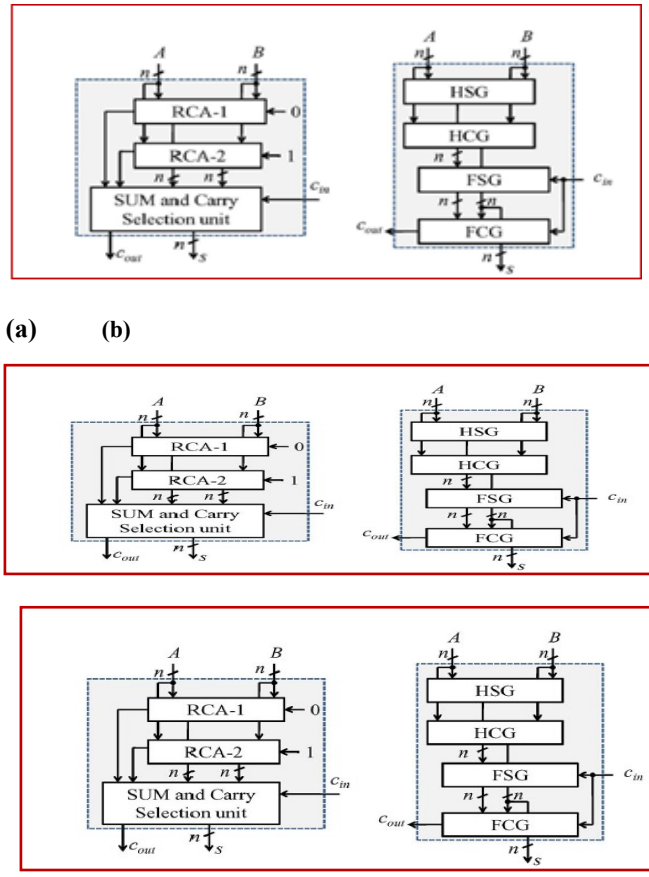

Figure1 :(a) Conventional CSLA (b) RCA

The conventional CSLA is shown in the figure1in which the Sum and Carry Generation unit consists of twon-bit RCAs, where n is the adder bit-width. The logic implementation of n-bit RCA is performed in four stages: 1) half-sum generation (HSG); 2) half-carry generation (HCG); 3) full-sum generation (FSG); and 4) fullcarry generation (FCG). Assume that two n-bit operands are added in the conventional CSLA, then RCA-1 and RCA-2 generate n-bit sum (s0 and s1) and output-carry (c0 out and c1 out) correspondingto input-carry (Cin = 0 and Cin = 1), correspondingly and whose logic expressions are shown in figure2.

$$s_0^0(i) = A(i) \oplus B(i) \quad c_0^0(i) = A(i) \cdot B(i)$$
$$s_1^0(i) = s_0^0(i) \oplus c_1^0(i-1)$$
$$c_1^0(i) = c_0^0(i) + s_0^0(i) \cdot c_1^0(i-1) \quad c_{\text{out}}^0 = c_1^0(n-1)$$
$$s_0^1(i) = A(i) \oplus B(i) \quad c_0^1(i) = A(i) \cdot B(i)$$
$$s_1^1(i) = s_0^1(i) \oplus c_1^1(i-1)$$
$$c_1^1(i) = c_0^1(i) + s_0^1(i) \cdot c_1^1(i-1) \quad c_{\text{out}}^1 = c_1^1(n-1)$$

Figure2: Logic Expressions of Conventional CSLA-SCG

In the figure2 it is obvious that the conventional CSLA unit is exhibiting redundant logic expressions. This

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redundancy is the root cause of loss of efficiency of the CSLA unit. The proposed architecture suggests the design with removal of this redundancy nature of the logic expressions. Theproposed system is shown in figure3.The proposed CSLA contains one HSG unit, one FSG unit, one CG unit, and one CS unit. The CG unit is composed of two CGs (CG0 and CG1) analogous to input-carry '0' and '1'. The HSG receives two n-bit operands (A and B) and produce half-sum word s0 and half-carry word c0 of size n bits each. Both CG0 and CG1 receive s0 and c0 from the HSG unit and produce two n-bit full-carry words c01 and c11 resultant to input-carry '0' and '1', correspondingly.

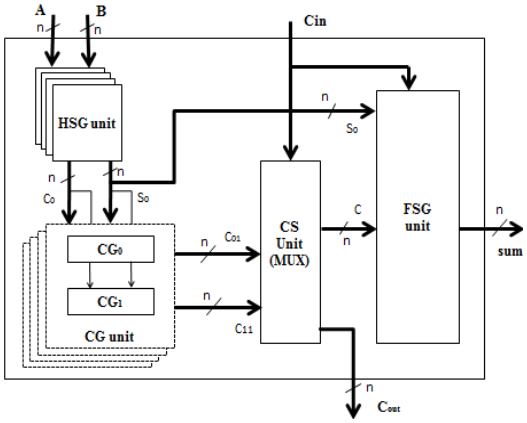

Figure3: proposed CSLA with removal of Redundancy

The proposed logic expressions are shown in figure3

Front-End Modeling:

This phase of implementation contains the following stages simulation using Xilinx 14.1Vivado suite, synthesis using Xilinx 14.1 XST and verifying on Virtex – 5 FPGA board.

$$s_0(i) = A(i) \oplus B(i) \quad c_0(i) = A(i) \cdot B(i)$$
$$c_1^0(i) = c_1^0(i-1) \cdot s_0(i) + c_0(i) \quad \text{for } (c_1^0(0) = 0)$$
$$c_1^1(i) = c_1^1(i-1) \cdot s_0(i) + c_0(i) \quad \text{for } (c_1^1(0) = 1)$$
$$c(i) = c_1^0(i) \quad \text{if } (c_{in} = 0)$$
$$c(i) = c_1^1(i) \quad \text{if } (c_{in} = 1)$$
$$c_{out} = c(n-1)$$
$$s(0) = s_0(0) \oplus c_{in} \quad s(i) = s_0(i) \oplus c(i-1).$$

Figure4: Logic Expressions of proposed architecture

IV. SIMULATION AND SYNTHESIS RESULTS

The Verilog RTL Description of the above article is simulatedand synthesized using Xilinx14.1 (ISE-Simulator), implementation of all the above proposed techniques are successfully synthesized and verified on Virtex -5 FPGA board and the results are shown below.

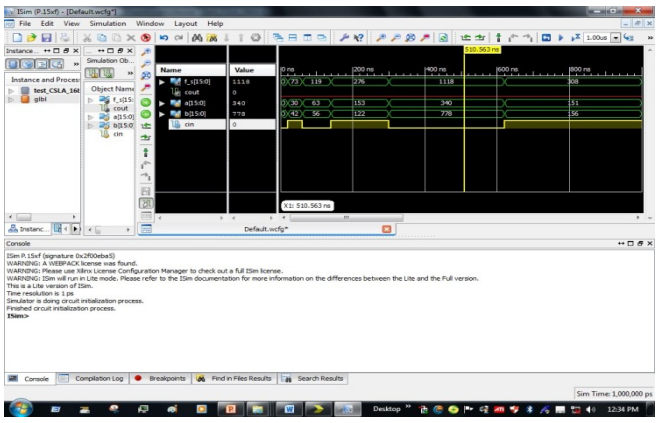

Figure5: Simulation output of proposed CSLA

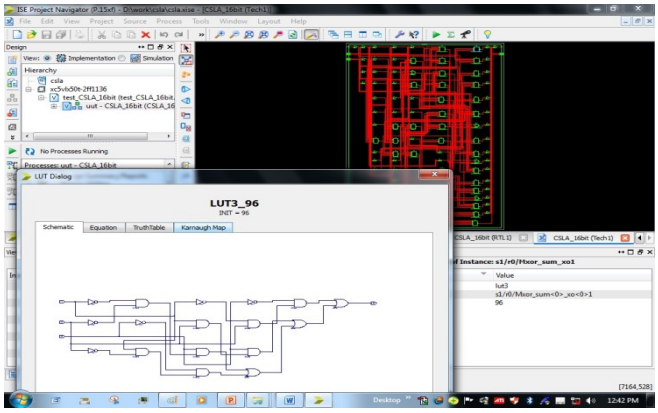

Figure6: Synthesis output of proposed CSLA

The Synthesized report is summarized in the following Table2.

TABLE 2
SUMMARY OF SYNTHESIS REPORT

Sno	Parameter	Quantification
1	Target Device	xc5vlx50t-2-ff1136
2	Slice Logic utilization	Less than 5%
3	Slice logic distribution	100%
4	IO utilization	1%
5	Specific feature factor	8%
6	Total logic delay	7.330nS
7	Total offset delay	Less than onenS
8	Total path delay	7.330nS
9	Real time compilation	10.00 S
10	Total memory usage	292836 Kb

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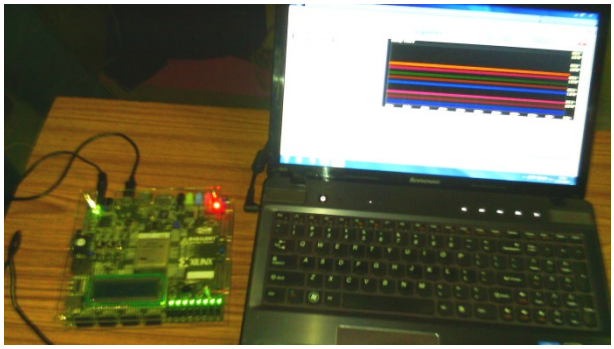

Figure 7: Proposed CSLA synthesized in Virtex-5 FPGA

TABLE 3
VERIFICATION OF POWER CONSUMPTION IN VIRTEX-5 FPGA

Channels	Voltage (V)	Current (mA)	Power (mW)
1.0	1.012	306	310
1.8	1.820	26	47
2.5	2.556	80	204
3.3	3.352	488	1636

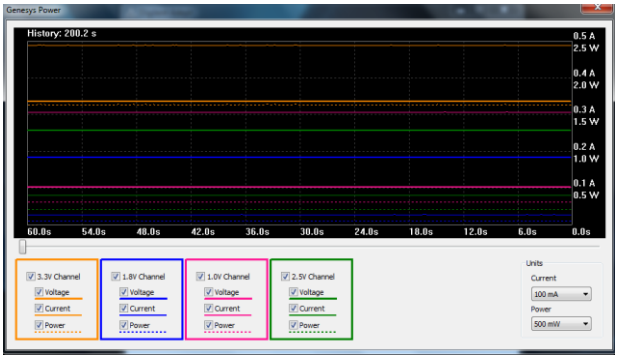

Figure 8: power graph analysis in Virtex-5 FPGA

V. CONCLUSION

In this paper, proposed a new encoding technique for the CSLA.In the projected system, the CS operation is planned before the calculation of final-sum, which is altered from the conventional CSLA. Carry words equivalent to input-carry '0' and '1' generated by the CSLA based on the proposed system follow a specific bit pattern, due to this the CS unit is logically optimized. For logical optimization the CS unit allowsfixed input bits. Based on this, significantly reduced design for CS and CG units are obtained. Using these optimized logic units, a competent design is obtained for the CSLA. The proposed CSLA design presents a considerably less area and delay.This paper has realized with Xilinx tools along with Virtex -5 FPGA. Such designs are suggested to exhibits a competitive performance with current work.

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