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Design of Digital Fir Filter Using MCM Technique

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Abstract

Finite impulse response (FIR) filters which are widely used in multi standard wireless communication systems have the key advantages of low power consumption and low area occupancy. The response of periodical system under any circumstances can be found by FIR filter. Digital FIR filter involves additions, shifting operations, along with storing of resulted outputs. Many algorithms such as mathematical can be analyzed through digital filters since digital filters work on digital input so it can be modified as desired. These methods include low power multiplier and adder. So digital filters are heavily used in many DSP applications and electronics applications as well. In this paper, an efficient implementation of FIR filter is presented.

Key Words: Shifter; Adder; Multiplier; Filter; FPGA

I. Introduction

The filters usually produce an impulse response which can be finite or infinite depending upon type of filter is to be designed. The implementation of FIR and IIR filters falls under totally different. When a unit impulse is given to the FIR filter, it produces a finite impulse response contrary to IIR filter produces an infinite response in terms of duration. FIR and IIR filters are preferred in different condition according to the requirements and provides efficient work for different situation and hence both filters have different advantages and disadvantages. FIR filters are implemented using either recursive or non-recursive techniques but usually non-recursive techniques are preferred. The DSP domain uses filters extensively since the characterization is performed by the extensive sequence of multiplied operations. There are different usages of filters depending upon the requirements, the FIR filter circuit operates at high sample rates or a low-power circuit operates at moderate sample rates. The Fig.1 is the logical diagram of the filter with the multiplier and adders being used. The adders and multiplier are used to reduce the parameter such as power consumption. However there are particular multipliers which are used for only specified reasons such as Wallace multiplier is used to increase the speed but at the cost of increased power consumption.

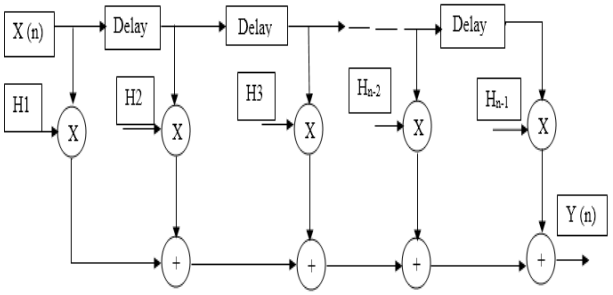

Fig.1.The logical diagram of filter

For FIR filter of order *N*, each value of the output sequence is a weighted sum of the most recent input values:

$$y[n] = \sum_{i=0}^{N} bi \,.\, x[n-1] \qquad (1)$$

The impulse response of the filter is defined as nonzero over a finite duration. Including

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zeros, the impulse response is the infinite sequence:

$$h[n] = \sum_{i=0}^{N} bi.\delta[n-1] \qquad (2)$$

There are four popular types of filters which are used widely in industry. The low pass filter which let only those frequencies to pass which are below specified level. The high pass filter which let only those frequencies to pass which are above specified level. The band pass filter which let only those frequencies to pass which are given in the range of minimum and maximum frequency. The band stop filter which stops all the frequency which is specified in the range. The band pass and band stop filter is opposite of each other.

II. Literature survey

An efficient parallel FIR filter implementation technique increase in the hardware cost [1]. The filter spectrum characteristics are exploited to select the best fast filter structure and a novel block filter quantization algorithm is used. Using benchmarks, the appropriate use of fast FIR filter structure and the quantization scheme can result in reduction in number of binary adders up to 20%. Power consumption is improved by using the pipeline gating scheme. FPGA implementation is applied. Now there is a method, based on the input, the clock gating is done to data flow direction and vertical to data flow direction. For signed multipliers using 2'scomplement representation, sign extension, which wastes power and causes longer delay, could be avoided by implementing this technique. Very little additional area is needed for this technique. Thus by implementing this technique, the delay is reduced but at the cost of increased area and hence cost of the filter is increased and power is increased as well if the filter is used for high number of inputs [2].Low power and low area filter is designed which is constructed using booth algorithm and gated driver techniques. The gated driver technique requires parallel adders and low power array to function. The output of the booth algorithm is to be saved and hence the storing elements are also required and because of this, the additional devices are used and the area and power consumption is increased. This is reconfigurable FIR filter and so it can be reconfigured according to the needs of the designer. This technique of filter implementation holds true only up to certain number of input if the inputs are increased the booth algorithm becomes complex and the designing becomes much more difficult.

III. Proposed method

In this paper, an efficient and less complex method of designing the filter is proposed. The multiple constant multiplication technique (MCM) can be used to reduce the hardware complexity of the filter. FIR filters based on MCM technique is called symmetric FIR filter. The Fig.2 is the proposed symmetric FIR filter block diagram.

The MCM technique is called multiplier less technique since in this the multiplication is reformed as shifts and adds and subtraction.

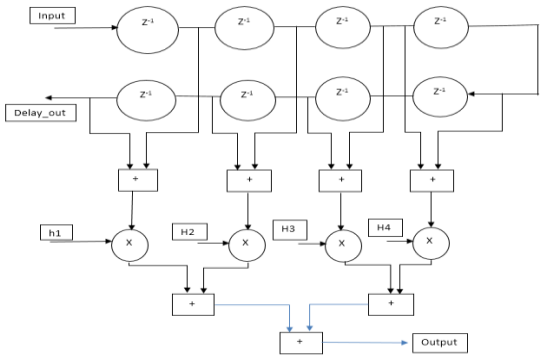

Fig.2.The logical diagram of proposed symmetric FIR filter.

The MCM can be done for single constants multiplication (SCM) and multiple constants

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multiplication (MCM).The multiplication $y = tx$ of a variable x by a known integer or fixed-point constant t can be decomposed into additions (adds), subtractions (subtracts), and binary shifts. The following example can explain the SCM perfectly.

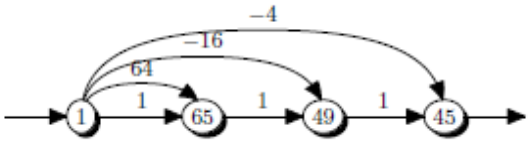

Fig.3.Example1 for SCM technique.

$$65x = x + 64x \quad (3)$$

$$49x = 65x - 16x \quad (4)$$

$$45x = 49x - 4x \quad (5)$$

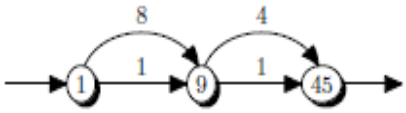

Fig.4. Example 2 for SCM technique

$$9x = 8x + x \quad (6)$$

$$45x = 5(9x) = 9x + 4(9x) \quad (7)$$

In the Fig.3 and Fig.4 example explains the single constant multiplication. An extension of SCM is the problem of multiplying a variable $x$by several constants t_1 to t_n in parallel and the below example will explain the multiple constant multiplication technique.

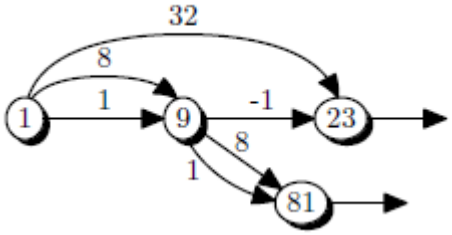

Fig.5. Example for MCM technique

In the Fig.5 example, the MCM technique is explained in simple terms. Here, 23 and 81 are taken as constants.

$$9x = 8x + x \quad (8)$$

$$23x = 32x - 9x \quad (9)$$

$$81x = 8(9x) + 9x \quad (10)$$

IV. Conclusion

There have been many techniques proposed to design FIR filter but the design proposed in this paper reduces the hardware complexity up to 40% compare to the other technique. The proposed FIR filter reduces power consumption since the addition and multiplications get reduced up to N times and N/2 times respectively. Thus the power consumption and hardware complexity reduces in the proposed symmetric FIR filter.

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