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PHY Monitor for PCIE 3.0

Sagar Kumar K S[1]& Venkategowda N[2]
P.G. Student, Dept. of ECE, MITE College, Moodabidri, Karnataka, India[1]
Assistant Professor, Dept. of ECE, MITE College, Moodabidri, Karnataka, India[2]
EMAIL: sagarkumar289@gmail.com[1]

Abstract

The serial protocols like PCI Express and USB have evolved over the years to provide very high operating speeds and throughput. This evolution has resulted in their physical layer protocol becoming very complex. One of the important task in the Physical layer of PCIe 3.0 is the monitoring and sampling different Ordered sets and Data Packets that come from different layers.

Key Words: Sampling; Ordered Sets;Data Packets; Verification Introduction

Introduction

The PCIe 3.0 architecture utilizes very efficient and productive algorithms for maintaining reliable link, highly optimized power consumption and extremely fast and flawless data transfer rate.

The serial protocols like PCI Express and USB have evolved over the years to provide very high operating speeds and throughput. PCI Express is a high performance, general purpose I/O interconnect defined for a wide variety of future computing and communication platforms. Key PCI attributes, such as its usage model, load-store architecture, and software interfaces, are maintained, whereas its parallel bus implementation is replaced by a highly scalable, fully serial interface. PCI Express takes advantage of recent advances in point-to-point interconnects,

Switch-based technology, and packetized protocol to deliver new levels of performance and features. Power Management, Quality of Service (QoS), Hot Plug/Hot-Swap support, Data Integrity, and Error Handling are among some of the advanced features supported by PCI Express.

The architecture of PCI Express is specified in terms of three discreet logic layers:

1. The Transaction layer
2. The Data Link Layer
3. The Physical Layer

Each of these layers is divided into two sub-divisions, one that processes outbound (to be transmitted) information and one that processes inbound (to be received) information, as shown in Fig. 1

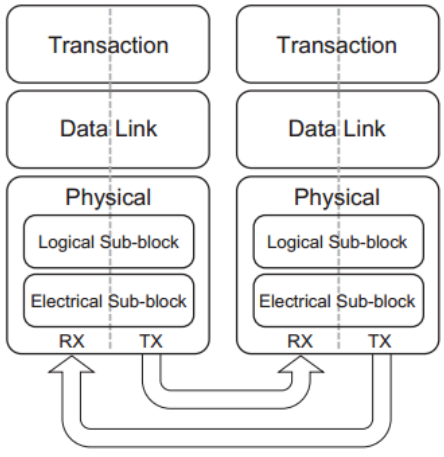

Fig. 1 High Level Layering Diagram

The communication between the components in PCI Express is done in the form of packets. The packets are created in the Transaction and Data Link Layers to carry the

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information from the transmitting to the receiving component. When the transmitted packets flow through the different logical layers, additional information will be appended in order to handle the packets at those layers. The reverse process takes place at the receiving side and packets get transformed from their Physical Layer representation to the Data Link Layer representation and finally (for Transaction Layer Packets) to the form that can be processed by the Transaction Layer of the receiving device. Fig. 2 shows the conceptual flow of transaction level packet information through the layers.

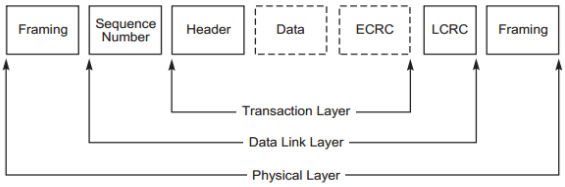

Fig. 2 Packet Flow through the Layers

Case Study

All In the world of communication protocols, PCI-Express presents throughput in 2.5 GT/s, 5.0 GT/s and 8.0 GT/s. It is important to not forget the purpose of each protocol. PCIe is a high-speed serial computer expansion bus standard designed to replace the older PCI, PCI-X, and AGP bus standards. PCIe has numerous improvements over the older standards, including higher maximum system bus throughput, lower I/O pin count and smaller physical footprint, better performance scaling for bus devices, a more detailed error detection and reporting mechanism and native hot-plug functionality. More recent revisions of the PCIe standard provide hardware support for I/O virtualization [1],[2],[3],[4].

[5] describes the controller support functionality of Transaction Layer and Data Link Layer of PCIe which also propose an efficient buffer management scheme to obey replay machanism.

[6] describes the design and implementation of novel MAC-PHY interface based on peripheral component interconnect express bus and FPGA.

With the evolution of modern verification methodologies, system-level verification using constrained-random stimulus is a high priority, especially in very large communication applications. A key goal to address is providing fast, effective test coverage. By analysing the real time coverage results from the simulation and thereafter intelligently modifying the corresponding stimulus, this novel method iteratively improves coverage. As a result, the GA can more effectively generate stimulus. The experimental results from both a C-based testbench and a real application (PCIe system) prove that the proposed GA method can streamline the verification effort and sharply reduce simulation time to achieve thorough coverage [10].

The SystemVerilog Language Reference Manual and Universal Verification Methodology User's Guide has been referred wherever required for language constructs [11][12].

Framing and Application Of Symbols To Lanes

The architecture of PCIe is classified in terms of three discrete logical layers: the Transaction Layer, the Data Link Layer, and the Physical Layer. The Physical Layer isolates the Transaction and Data Link Layers from the signaling technology used for Link data interchange.

There are two classes of framing and application of Symbols to Lanes. The first class consists of the Ordered Sets and the second class consists of TLPs and DLLPs packets. Ordered Sets are always transmitted serially on each Lane, such that a full Ordered Set appears

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simultaneously on all Lanes of a multi-Lane Link.

The Framing mechanism uses Special Symbol K28.2 “SDP” to start a DLLP and Special Symbol K27.7 “STP” to start a TLP. The Special Symbol K29.7 “END” is used to mark the end of either a TLP or a DLLP.

Different types of ordered sets are Training Sequence, Electrical Idle Sequences, Lane Polarity Inversion, Fast Training Sequence, Start of Data Stream Ordered Set.

Training Sequences are composed of Ordered Sets used for initializing bit alignment, Symbol alignment and to exchange Physical Layer parameters. When the data rate is 2.5 GT/s or 5.0 GT/s, Training sequence Ordered Sets are never scrambled but are always 8b/10b encoded. When the data rate is 8.0 GT/s or higher, the 128b/130b encoding is used and Symbols may or may not be scrambled. Training sequences (TS1 or TS2)are transmitted consecutively and can only be interrupted by SKP Ordered Sets and EIEOS in data rates other than 2.5GT/s.

Electrical Idle Sequences Before a Transmitter enters Electrical Idle, it must always send the Electrical Idle Ordered Set (EIOS). When using 8b/10b encoding, an EIOS is a K28.5 (COM) followed by three K28.3 (IDL)Symbols. Transmitters must transmit all Symbols of an EIOS. An EIOS is received when the COM and two of the three IDL Symbols are received. When using 128b/130b encoding, an EIOS is an Ordered Set block, Transmitters must transmit all Symbols of an EIOS if additional EIOSs are to be transmitted following it. Transmitters must transmit Symbols 0-13 of an EIOS, but are permitted to terminate the EIOS anywhere in Symbols 14 or 15, when transitioning to Electrical Idle after it. An EIOS is considered received when Symbols 0-3 of an Ordered Set Block match the definition of an EIOS.

Lane Polarity Inversion During the training sequence in Polling, the Receiver looks at Symbols 6-15 of the TS1 and TS2 Ordered Sets as the indicator of Lane polarity inversion (D+ and D- are swapped). If Lane polarity inversion occurs, the TS1 Symbols 6-15 received will be D21.5 as opposed to the expected D10.2. Similarly, if Lane polarity inversion occurs, Symbols 6-15 of the TS2 Ordered Set will be D26.5 as opposed to the expected D5.2. This provides the clear indication of Lane polarity inversion. If polarity inversion is detected the Receiver must invert the received data. The Transmitter must never invert the transmitted data. Support for Lane Polarity Inversion is required on all PCI Express Receivers across all Lanes independently.

Fast Training Sequence (FTS) is the mechanism that is used for bit and Symbol lock when transitioning from L0s to L0. The FTS is used by the Receiver to detect the exit from Electrical Idle and align the Receiver’s bit and /Symbol receive circuitry to the incoming data.

Start of Data Stream Ordered Set It is defined only for 128b/130b encoding. It is transmitted in the Con Fig. uration. Idle, Recovery. Idle, and Tx_L0s.FTS LTSSM states to define the transition from Ordered Set Blocks to a Data Stream, and Loopback Masters are permitted to transmit it. It must not be transmitted at any other time. While not in the Loopback state, the Block following an SDS Ordered Set must be a Data Block, and the first Symbol of that Data Block is the first Symbol of the Data Stream.

Verification Architecture

The LTSSM has been designed and verified using UVM methodology. The verification architecture is as shown in Fig 3(a). The MAC driver has the driving LTSSM which will keep track of the state machine transitions, whereas the MAC monitor monitors the arrival and sampling of the data packets and ordered

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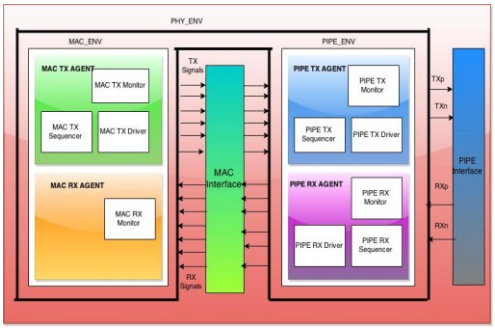
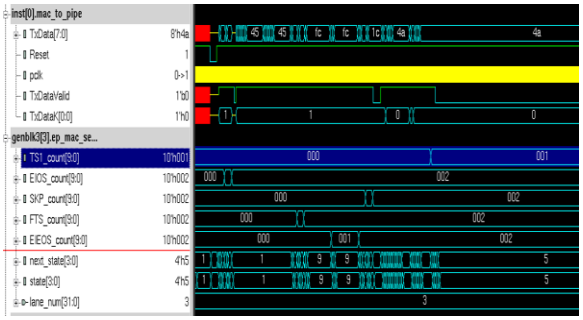
sets from the upper layers at the transmit side of the MAC agent. The receive side of the MAC agent samples the data packets and ordered sets from the PIPE interface and drives it to the upper layers. The data packets are scrambled and descrambled in the MAC agents. The transmit side of the PIPE agent encodes and serializes the data packets on to the PIPE interface. The receive side of the PIPE agent decodes and desterilizes the data packets from the PIPE interface.

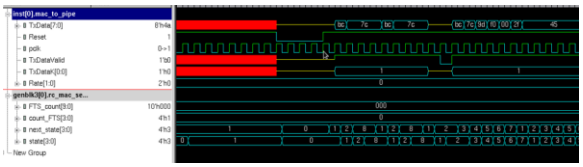
Fig 3(b) shows the simulation result of the detection of all the Ordered Sets depending on the sequence of symbols that has received. Fig(c) shows the simulation result of the FTS and TS1 Ordered Set when it receives the definite sequence of symbols



(a)



(b)



(c)

Fig 3 Verification and Simulation Results (a) Verification Environment (b) Simulation of detection of all Ordered Sets (c) Simulation result of FTS and TS1 Ordered Set

The MAC driver has the driving LTSSM which will keep track of the state machine transitions, whereas the MAC monitor monitors the arrival and sampling of the data packets and ordered sets from the upper layers at the transmit side of the MAC agent.

The receive side of the MAC agent samples the data packets and ordered sets from the PIPE interface and drives it to the upper layers. The data packets are scrambled and descrambled in the MAC agents.

The transmit side of the PIPE agent encodes and serializes the data packets on to the PIPE interface. The receive side of the PIPE agent decodes and deserializes the data packets from the PIPE interface.

Conclusion

The MAC Monitor is designed and verified for different sets of ordered sets. The ordered sets are tapped from the MAC interface and are sampled at each clock pulse. The ordered sets are checked for its particular sequence and sampled and monitoring its behaviour. The MAC monitor is designed and verified both at the transmitter and the receiver side.

Acknowledgement

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