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Realization of Data Encoding Schemes in Network on Chip Using Verilog HDI

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Abstract:

Power has become a paramount design criterion in modern system designs, especially in portable battery-driven applications. A paramount portion of total power dissipation is due to the transitions on the off-chip address buses. This is because of the astronomically immense switching capacitances associated with these bus lines. There are many encoding schemes in the literature that achieve an immensely colossal reduction in transition activity on the ordinant dictation address bus. However, on data and multiplexed address buses, none of the subsisting schemes consistently achieve consequential reduction in transition activity. Additionally, many of the subsisting techniques integrate redundancy in space and/or time. In this paper, novel encoding schemes are proposed that significantly reduce transitions on these buses without integrating redundancy in space or time. Additionally, for applications with tight delay constraints, configurations with minimal delay overhead while still achieving paramount reduction in transition activity are proposed. Results show that, for sundry benchmark programs, these techniques achieve reduction of up to 54% in transition activity on a data address bus. On a multiplexed address bus, there is a reduction of up to 61% utilizing our techniques. The proposed schemes are then compared with the subsisting schemes. It is optically discerned that on an average, the reductions achieved by our techniques are twice those obtained utilizing the current scheme on a data address bus and 55% more than those for multiplexed address bus.

Keywords: Binary to gray conversion; Data encoding; Interconnection on chip; Low power; Network-on-chip (NOC); Power analysis; Gray to binary conversion.

Introduction

As VLSI technologies perpetuate to scale, wire densities increases to fortify ever-minuscule transistor geometries and casuses on-chip wires to present incrementing latency and energy quandary. In particular, the high latency of cross-chip communication can still limit total performance by incrementing the delay between on-chip unit. Such scalable bandwidth requisite can be satiated by utilizing on-chip packet-switched micro-network of interconnects, generally kenned as Network-on-Chip (NoC) architecture. The rudimental conception emanated from the traditional sizably voluminous-scale multi-processors and distributed computing networks. The scalable and modular nature of NoC and their fortification for efficient onchip communication lead to the NoC-predicated system implementations. In order to meet typical SoCs or multicore multiprocessing and rudimentary module of network interconnection like switching logic, routing algorithm and the packet definition should be light-weighted to result in facilely implemental solutions.

Another approach to exceed such a circumscription of communication and overcome such a cyclopean wiring delay in future technology is to adopt network-like interconnections which is called Network-on-

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Chip (NoC) architecture. Fundamental concept of such kind of interconnections emanates from the modern computer network evolution as mentioned afore. By applying network-like communication which inserts some routers in-between each communication object, the required wiring can be minimized. Therefore, the switch-predicated interconnection mechanism provides a plethora of scalability and liberation from the circumscription of involute wiring. Supersession of SoC busses by NoCs will follow the same path of data communications when the economics prove that the NoC either reduces SoC manufacturing cost, SoC time to market, SoC time to volume, and SoC design risk or increases SoC performance.

According to the NoC approach has a clear advantage over traditional busses and most eminently system throughput. And hierarchies of crossbars or multilayered busses have characteristics somewhere in between traditional busses and NoC, however they still fall far short of the NoC with veneration to performance and involution.The prosperity of the NoC design depends on the research of the interfaces between processing elements of NoC and interconnection fabric. The interconnection of a SoC established procedures has some impuissant points in those venerations of slow bus replication time, energy circumscription, scalability quandary and bandwidth inhibition. Bus interconnection composed of an astronomically immense number of components in a network interface can cause slow interface time though the influence of sharing the bus. In integration the interconnection has a defect that power consumption is high on the score of connecting all objects in the communication. Moreover it is infeasible to increment the number of connection of the elements illimitably by reason of the circumscription of bandwidth in a bus.

As a consequence, the performance of the NoC design relies greatly on the interconnection paradigm .Though the network technology in computer network is already well developed, it is virtually infeasible to apply to a chip-level intercommunication environment without any modification or reduction. For that reason, many researchers are endeavoring to develop felicitous network architectures for on-chip communication. To be eligible for NoC architecture, the rudimentary

functionality should be simple and light-weighted because the implemented component of NoC architecture should be minute enough to be a fundamental component constructing a SoC. In order to be low powered one has to consider many parameters such as clock rate, operating voltages, power management.

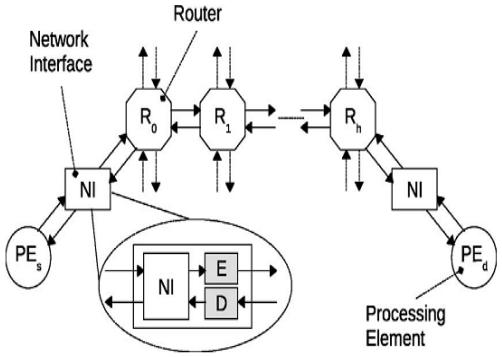

Fig 1: Fundamental concept of NOC.

As shown in Fig the NI is augmented with an encoder(E) and a decoder (D) block. With the exception of the header flit, the encoder encodes the outgoing flits of the packet in such a way as to minimize the potency dissipated by the inter-router point-to-point links which form the routing path of the current packet. Since the routers are not equipped with any encoding/decoding logic, the header flit is not encoded as it contains control information (destination address, packet size, and so on) which have to be processed by the routers through the routing path. Similarly to the above description, all the incoming flits in the network interface (with the exception of the header flit) are decoded by the encoder block. It should be pointed out that the proposed scheme is de-signed to be applied in the context of no VC predicated implementations. In fact, if VCs are utilized, the postulation that the flits belonging to different packets are not

interleaved in the same link is not valid anymore. At any rate, it does not denote that the proposed scheme cannot be applied in VC predicated implementations but, instead, that the potential power savings are reduced.

1. Related Work

In the next several years, the availability of the chips with 1000 cores is premised [6]. In these chips, a consequential fraction of the total system power budget is dissipated by interconnection network. Therefore, the design of power efficient interconnection networks has been the focus of many works published in the literature dealing with NoC architecture. These works concentrate on different components of the interconnection networks such as routers, NI, and links. Since the focus of this paper is on reducing the puissance dissipation by the links, in this section, briefly review some of the works in the area of link power reduction. These include the techniques that make utilization of shielding [7], [8], incrementing line-to-line spacing [9], [10], repeater insertion [11]. They all increase the chip area. The data encoding scheme is another method that was employed to reducing the link power dissipation. The data encoding techniques may be relegated into two types. In the first type, encoding techniques concentrate on lowering the potency due to self-switching activity of individual bus lines while ignoring the puissance dissipation owing to their coupling switching activity. In this type, bus invert (BI) [12] and INC-XOR [13] have been proposed for the case that arbitrary data patterns are transmitted through these lines. On the other hand, gray code [14], T0 [15], working-zone encoding [16], and T0-XOR [17] were suggested for the case of correlated data patterns. Application specific approaches have additionally been proposed [18]–[22].This category of encoding is not opportune to applied in the deep sub micron meter technology nodes where the coupling capacitance constitutes a major part of the total interconnect capacitance. This causes the puissance consumption due to the coupling switching activity to become an immensely colossal fraction of the total link power consumption, making the above mentioned techniques, which ignore such contributions, inefficient [23].The works in the second type concentrate on reducing power dissipation through the reduction of the coupling witching [10], [22] Among these schemes [10], [24]–[28], the switching activity is reduced utilizing many extra control lines. For example, data bus width grows from 32 to 55 in [24]. The techniques proposed in [20] have a more diminutive number of control lines but the intricacy of their decoding logic is high. The technique is described as follows: first, the data are both aberrant inverted and even inverted, and the transmission is performed utilizing the kind of inversion that reduces more the switching activity. In [30],the coupling switching activity is reduced up to 39%. In this paper, compared to [30], we utilize a simpler encoder and decoder while achieving a higher activity reduction. Let us now discuss in more detail the works with which we compare our proposed data encoding schemes. In [12], the number of transitions from 0 to 1 for two consecutive flits (the flit that just traversed and the one which is about to traverse the link) is counted. If the number is more sizably voluminous than a moiety of the link width, the inversion will be perfo ed to reduce thenumber of 0 to 1 transitions when the flit is transferred via the link. This technique is only concerned about the self-switching without worrying the coupling switching. Note that the coupling capacitance in the state-of–the-art silicon technology is considerably more sizably voluminous (e.g., four times) compared with the self-capacitance, and should be considered in any scheme proposed for the link power reduction.

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Time	Normal			Odd Inverted		
	Type I			Types II, III, and IV		
$t-1$	00, 11	00, 11, 01, 10	01, 10	00, 11	00, 11, 01, 10	01, 10
t	10, 01	01, 10, 00, 11	11, 00	11, 00	00, 11, 01, 10	10, 01
	T1*	T1**	T1***	Type III	Type IV	Type II
$t-1$	Type II			Type I		
t	01, 10			01, 10		
	10, 01			11, 00		
$t-1$	Type III			Type I		
t	00, 11			00, 11		
	11, 00			10, 01		
$t-1$	Type IV			Type I		
t	00, 11, 01, 10			00, 11, 01, 10		
	00, 11, 01, 10			01, 10, 00, 11		

Table 1: Effect of Odd Inversion on Change of Transition Types.

2. Implementation

3.1 Proposed Encoding Schemes:

In this section, present the proposed encoding scheme whose goal is to reduce power dissipation by minimizing the coupling transition activity on the links of the interconnection network. Let us first describe the puissance model that contains the different components of puissance dissipation of a link.. One can relegate four types of coupling transitions. A Type I transition occurs when one of the lines switches when the other remains unchanged. In a Type II transition, one line switches from low to high, other makes transition from high to low .A Type III transition corresponds to the case where both lines switch simultaneously. Determinately, in a Type IV transition both lines do not transmute. The efficacious switched capacitance varies from type to indite and hence, the coupling transition activity, is a weighted sum of variants of coupling transition contributions .Here, we calculate the occurrence probability for variants of transitions. Consider that flit (t − 1) and flit (t) refer to the antecedent flit which was transferred through the link and the flit is about to pass through the link, respectively.We consider only two adjacent bits of the physical channel.Sixteen different coalescences of these four bits could occur (Table I). Note that the first bit is the value of the generic i th line of the link, whereas the second bit represents the value of its (i + 1)th line. The number of transitions for Types I, II, III, and IV are 8, 2, 2, and 4, respectively. For an arbitrary set of data, each of these sixteen transitions has the same probability. Therefore, the occurrence probability for Types I, II, III, and IV are 1/2, 1/8, 1/8, and 1/4, respectively. In the rest of this section, we present three data encoding schemes designed for reducing the dynamic power dissipation of the network links along with a possible hardware implementation of the decoder.

3.1(a) SCHEME I:

In Scheme I, we fixate on reducing Type I transitions while in Scheme II, both Types I and II transitions are taken into account for deciding between half and full invert, depending the amount of switching reduction. Determinately, in Scheme III, we consider the fact that Type I transitions show different comportments in the case of eccentric and even invert and make the inversion which leads to the higher power preserving.

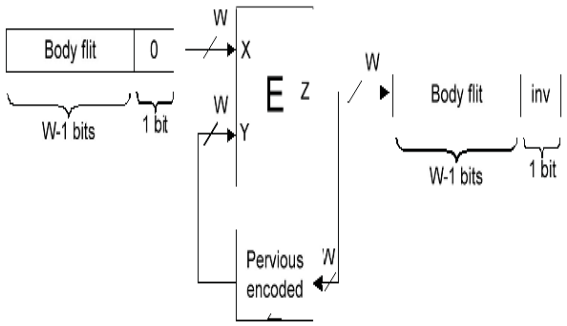

Fig 2: Circuit diagram of encoder architecture of scheme I.

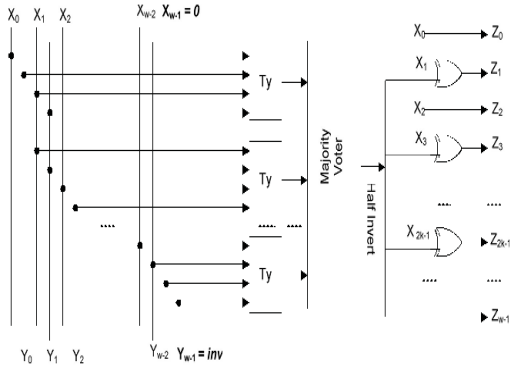

Fig 3: Internal view of encoder block.

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In scheme I, we fixate on reducing the numbers of Type I transitions (by converting them to Types III and IV transitions) and Type II transitions (by converting them to Type I transition). The scheme compare the current data with the antecedent data one to decide whether aberrant inversion or no inversion of the current data can lead to the link power reduction. Table I reports, for each transition, the relationship between the coupling transition activities of the flit when transmitted and when its bits are eccentric inverted. Data are organized as follows. The first bit is the value of the generic i th line of thelink, whereas the second bit represent the value of its (i + 1)th line. For each partition, the first line represents the values at time t − 1(t). As Table I shows, if the flit is aberrant inverted, Types II, III, and IV transitions convert to Type I transitions. In the case of Type I transitions, the inversion leads to one of Types II, III, or Type IV transitions. In particular, the transitions betokened as T∗1, T∗∗1,andT∗∗∗1 in the table convert to Types II, III, and IV transitions, respectively.

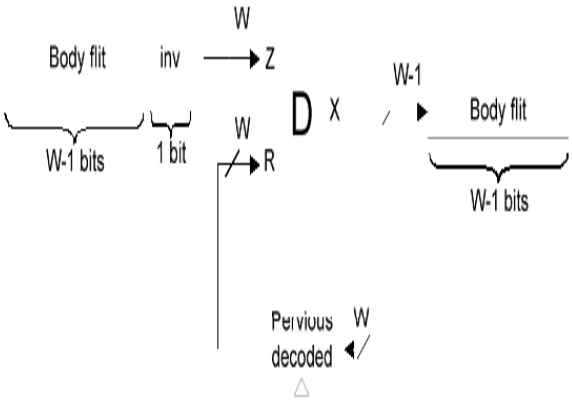

Fig 4: circuit diagram of decoder architecture.

3.1(b) SCHEME II:

In the proposed encoding scheme II, we make utilization of both aberrant (as discussed anteriorly) and full inversion. The full inversion operation converts Type II transitions to Type IV transitions. The scheme compares the current data with the precedent one to decide whether the aberrant, plenary, or no inversion of the current data can give elevate to the link power reduction.

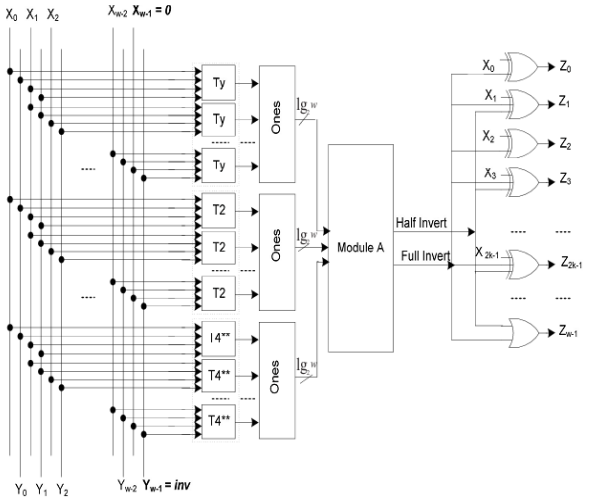

Fig 4: Encoder architecture scheme II.

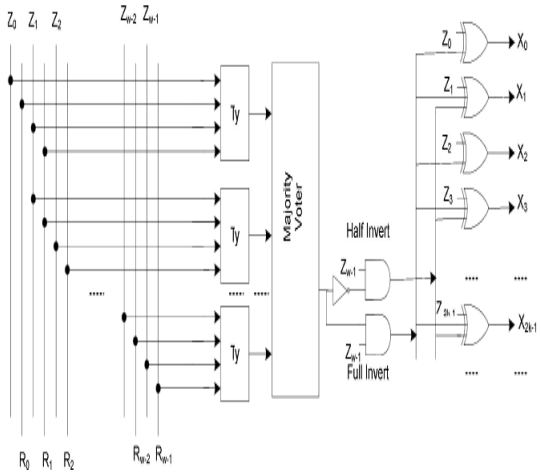

Fig 5: Internal view of the decoder block scheme II.

The w bits of the incoming body flit are designated by Z I (R I), i = 0 , 1 ,...,w− 1. The w th bit of the body flit is denoted by inv which shows if it was inverted (inv = 1) or left as it was (inv = 0). For the decoder, we only need to have the Ty block to determine which action has been taken place in the encoder. Predicated on the outputs of these blocks , the majority voter block checks the validity of the inequality .If the output is “0” (“1”) and the inv = 1,it signifies that half (full) inversion of the bits has been per-composed. Utilizing this output and the logical gates, the inversion action is tenacious. If two inversion bits were utilized,

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the overhead of the decoder hardware could be substantially reduced.

This module determines if aberrant, even, plenary, or no invert action corresponding to the outputs "10,""01," "11," or "00," respectively, should be performed. The outputs "01," "11," and "10" show that whether respectively, are gratified. In this paper, Module C was designed predicated on the conditions given .Similar to the procedure used to design the decoder for scheme II, the decoder for scheme III may be designed .This article has been accepted for inclusion in a future issue of this journal. Content is final as presented, with the exception.

Time	Normal			Even Inverted		
	Type I			Types II, III, and IV		
$t-1$	01, 10	00, 11, 01, 10	00, 11	01, 10	00, 11, 01, 10	00, 11
t	00, 11	10, 01, 11, 00	01, 10	10, 01	00, 11, 01, 10	11, 00
	T1*	T1**	T1***	Type II	Type IV	Type III
$t-1$	Type II			Type I		
t	01, 10			01, 10		
	10, 01			00, 11		
$t-1$	Type III			Type I		
t	00, 11			00, 11		
	11, 00			01, 10		
$t-1$	Type IV			Type I		
t	00, 11, 01, 10			00, 11, 01, 10		
	00, 11, 01, 10			10, 01, 11, 00		

Table 2: Effect of Even Inversion on Change of Transition Types.

3.1(c) SCHEME III:

In the proposed encoding Scheme III, we integrate even inversion to Scheme II. The reason is that aberrant inversion converts some of Type I (T***1) transitions to Type II transitions. As can be observed from Table II, if the flit is even inverted, the transitions designated as T**1/ T***1 in the table are converted to Type IV/Type III transitions. Therefore, the even inversion may reduce the link power dissipation as well. The scheme compares the current data with the anterior one to decide whether eccentric, even, plenary, or no inversion of the current data can give elevate to the link power reduction.

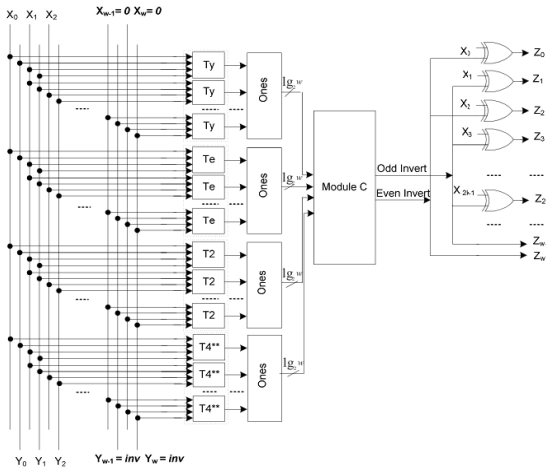
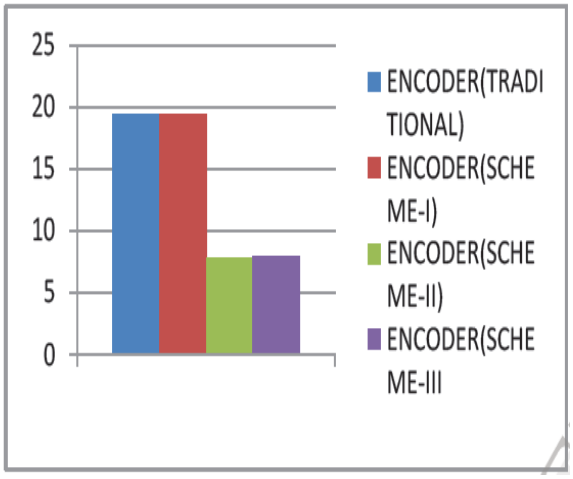


Fig 6: Encoder architecture scheme III.

3. Experimental Results

Dynamic Power Dissipation for Encoder:

ENCODER (TRADITIONAL)	ENCODER(PROPOSED) SCHEME –I	ENCODER(PROPOSED) SCHEME –II	ENCODER(PROPOSED) SCHEME – III
19.45 mw	19.43mw	7.76mw	7.87mw



Dynamic Power Dissipation for Decoder:

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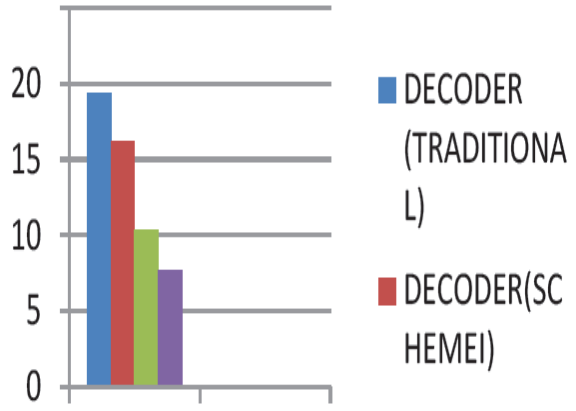
DECODER (TRADITIONAL)	DECODER(PROPOSED) SCHEME –I	DECODER (PROPOSED) SCHEME - II	DECODER(PROPOSED) SCHEME –III
19.35mw	16.19mw	10.37mw	7.66mw



4. Conclusion

In this paper, a set of incipient data encoding schemes aimed at reducing the puissance dissipated by the links of an NoC. As compared to the antecedent encoding schemes the rationale abaft the proposed schemes is to minimize not only the switching activity, but additionally the coupling switching activity which is mainly responsible for link power dissipation. By utilizing the proposed encoding schemes in NoC architecture their application does not require any modification neither in the routers nor in the links. As per the performance evaluation results, the proposed system has lower dynamic power dissipation than classical one.

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