International Journal of Research (IJR)
e-ISSN: 2348-6848, p- ISSN: 2348-795X Volume 2, Issue 07, July 2015
Available at http://internationaljournalofresearch.org

High Speed Low Power Combinational and Sequential Booth Multiplayer Using Trong Circuits using Reversible logic

[1] M. Divya & [2] B. Shoba rani
1. M.Tech Chaitanya institute of technology and science, Warangal, T.S India.
2. M.Tech Associate Professor, Chaitanya institute of technology and science, Warangal, T.S India..

ABSTRACT:

The proposed testable reversible architecture scheme yields significantly reduced complexity, low power and high speed features. It is a key issue in the interface of computation and physics, and of growing importance as miniaturization progresses towards its physical limits. With the advent of nanotechnology the fault detection and testability is of high interest for accuracy. This research work describes the reversible testable design of high-speed modified Booth multipliers. The proposed multiplier circuits are based on the modified Booth algorithm can be used to accelerate the multiplication speed with reduced power consumption Reversible logic has presented itself as a prominent technology which plays an imperative role in Quantum Computing. Quantum computing devices theoretically operate at ultra high speed and consume infinitesimally less power. Research done in this paper aims to utilize the idea of reversible logic to break the conventional speed-power trade-off, thereby getting a step closer to realize Quantum computing devices.

1. Introduction

Garbage output refers to the output that is not used as a primary output or as an input to other gate. Reversible logic is likely to be in demand in high speed power aware circuits. The digital signal processing (DSP gates used and garbage outputs produced) is one of the core technologies in multimedia and communication systems. Many application systems based on DSP, especially the recent next-generation optical communication systems, require extremely fast processing of a huge amount of digital data. Most of DSP applications such as fast Fourier transform (FFT) require additions and multiplications. Since the multipliers have a significant impact on the performance of the entire system, many high-performance algorithms and architectures have been proposed to accelerate multiplication1,9. Well-structured design of the booth multiplier is given by Wang2 . Further optimization can be achieved using reversible logic11. The reversible computation in a system can be performed only when the system comprises of reversible gates. These circuits can generate unique output vector from each input vector and vice versa, that is, there is a one-to-one mapping between input and output vectors. The major goal in reversible logic design is to minimize the number of reversible. 1.1 Reversible Logic Reversible circuits are of high interest in low power CMOS design, optical computing 7, quantum computing and nanotechnology3. The most prominent application of reversible logic lies in quantum computers. A quantum computer can be viewed as a quantum network (or a family of quantum networks) composed of quantum logic gates; each gate performs an elementary unitary operation on one, two or more two–state quantum systems called qubits. Each qubit represents an elementary unit of information corresponding to the classical bit values 0 and 1. Any unitary operation is reversible, hence quantum networks effecting elementary arithmetic

International Journal of Research (IJR)
e-ISSN: 2348-6848, p- ISSN: 2348-795X Volume 2, Issue 07, July 2015
Available at http://internationaljournalofresearch.org

operations such as addition, multiplication and exponentiation cannot be directly deduced from their classical Boolean counterparts (classical logic gates such as AND or OR are clearly irreversible)8 . There are various reversible gates available in literature3,5,6,10. The concept of testability is being introduced for higher accuracy concerns4–6. 1.2 Booth Encoding and Multiplier Booth9 introduced Booth Multiplier (BM). They are also called radix-2 multiplier. The main advantage is that it involves no correction cycles for signed terms. To multiply X by Y using the modified Booth algorithm starts from grouping Y by three bits and encoding into one of {–2, –1, 0, 1, 2}. Table 1 shows the rules to generate the encoded signals by booth encoding scheme. After Booth recoding, a digit number is changed from two's complement representation to Booth representation. In some cases, the weight of the latter is less than that of the former one; the Booth algorithm can be used in multiplier to reduce the number of partial products. But it is not for all the cases. For example, the weight of binary number 010101 is 3, the Booth representation for this number is (+ 1 – 1 + 1 – 1 + 1 – 1), and its weight is 6. Multiple bits scanning per cycle in booth recoding reduces the number of partial products significantly, hence reduces the area, power and speeds up the designs.

Goals of Reversible Logic:

A. Quantum Cost: Quantum cost of a circuit is the measure of implementation cost of quantum circuits. More precisely, quantum cost is defined as the number of elementary quantum operations needed to realize a gate.

B. Speed of Computation: The time delay of the circuits should be as low as possible as there are numerous computations that have to be done in a system involving a quantum processor; hence speed of computation is a very important parameter while examining such systems.

C. Garbage Outputs: Garbage outputs are those output signals which do not contribute in driving further blocks in the design. These outputs become redundant as they are not required for computation at a later stage. The garbage outputs make the system slower; hence for better efficiency it is necessary to minimize the number of garbage outputs.

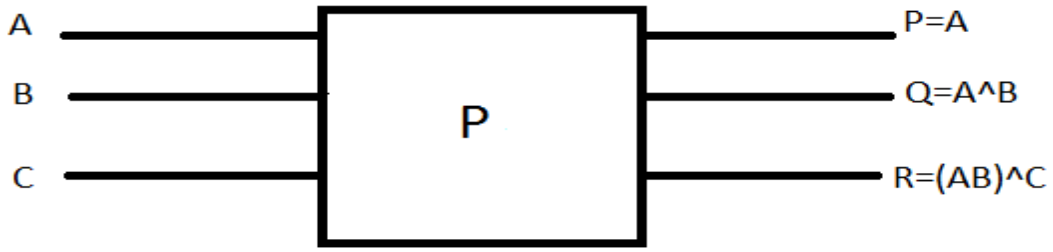
D. Feedback: Looping is strictly prohibited when designing reversible circuits.

E. Fan-out: The output of a certain block in the design can only drive at most one block in the design. Hence it can be said that the Fan-out is restricted to

III. REVERSIBLE GATES

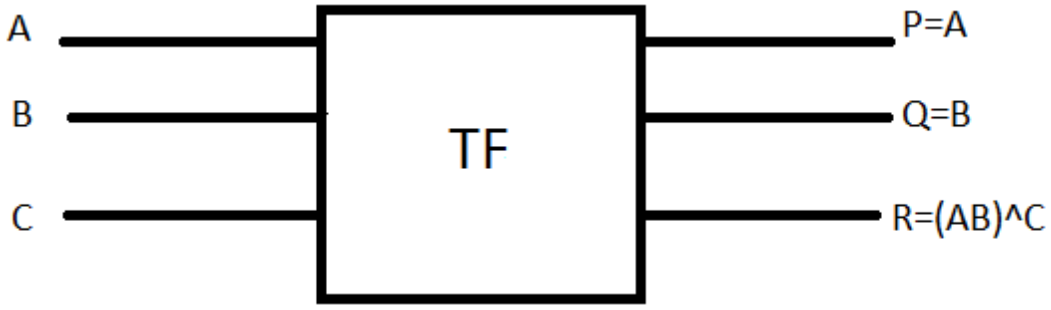
There are many reversible gates such as Feynman, Toffoli, TSG, Peres, etc [3]. As the universal gates in boole an logic are N and and Nor, for reversible logic, the universal gates are Feynman and Toffoli gates.

Peres Gate: It is a basic reversible gate which has 3- inputs and 3-outputs having inputs (A, B, C) and the mapped outputs (P=A, Q=A^B, R=(A.B)^C). The block diagram is as shown in fig. 3:

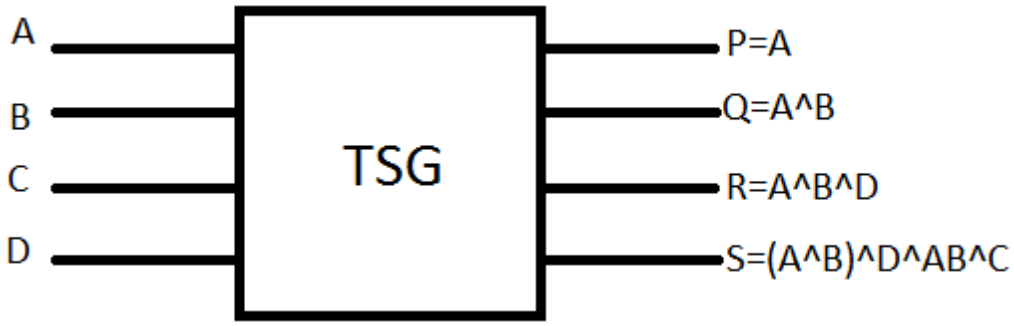


Toffoli Gate: Toffoli gate is a universal reversible gate which has three inputs (A, B, C) mapped to three outputs (P=A, Q=B, R= (A.B)^C). The block diagram of Toffoli gate is shown in fig. 4:

International Journal of Research (IJR)
e-ISSN: 2348-6848, p- ISSN: 2348-795X Volume 2, Issue 07, July 2015
Available at http://internationaljournalofresearch.org



TSG Gate: TSG gate is a reversible gate which has four inputs (A, B, C, D) mapped to four outputs (P=A,Q=A^B, R=A^B^D, S=(A^B)^D^AB^C). The block diagram of TSG Gate is shown in fig. 5:



Design and Implementation:

In booth multiplier the reversible adders and reversible barrel shifters are used as basic building block, the logic behind booth multiplier implemented using testable reversible NTG logic the computation results for delay, power and logical complexity are compared later. Booth Multiplier: The Booth recoding multiplier is one such multiplier; it scans the three bits at a time to reduce the number of partial products. These three bits are: the two bit from the present pair; and a third bit from the high order bit of an adjacent lower order pair. After examining each triplet of bits, the triplets are converted by Booth logic into a set of five control signals used by the adder cells in the array to control the operations performed by the adder cells. The method of Booth recording reduces the numbers of adders and hence the delay required to produce the partial sums by examining three bits at a time. To speed up the multiplication Booth encoding performs several steps of multiplication at once. Booth's algorithm takes advantage of the fact that an adder subtracted is nearly as fast and small as a simple adder. Conclusion: The drawbacks of booth multiplier are number of add subtract operations and the number of shift operation becomes variable and becomes inconvenient in designing parallel multipliers. The algorithm becomes inefficient when there are isolated 1's.which results in more power consumption due to large number of adders. Summing the partially redundant partial products requires as much hardware as representing them in the fully redundant form along the evaluation path

Reversible Logic Gate: A reversible logic circuit should have the following features: · Use minimum number of reversible gates. · Use minimum number of garbage outputs. · Use minimum constant inputs Reversible

Gates are circuits in which number of outputs is equal to the number of inputs and there is a one to one correspondence between the vector of inputs and outputs. It not only helps us to determine the outputs from the inputs but also helps us to uniquely recover the inputs from the outputs. A 4* 4 reversible DKG gate that can work singly as a reversible Full adder and a reversible Full subtract or is shown in Fig 6a. It can be verified that input pattern corresponding to a particular output pattern can be uniquely determined. If input A=0, the proposed gate works as a reversible Full adder, and if input A=1, then it works as a reversible Full subtract or. It has been proved that a reversible full adder circuit requires at least two garbage outputs to make the output combinations unique.

CONCLUSION:

It can be seen that the performance of digital circuits can be enhanced using reversible gates and have compared 8-bit ripple carry reversible adder with an irreversible adder in terms of speed and power; thereby concluding that reversible designs are faster and power efficient.

APPLICATIONS AND FUTURE SCOPE:

Reversible logic design finds applications in various fields including Quantum computing, Nano-computing, optical computing, Quantum Computing Automata (QCA: study of mathematical objects called Abstract machines and the computational problems that can be solved using them), ultra- low power VLSI designing, Quantum dot cellular etc. The future of computer chips is limited by Moore's law; hence an alternative is to build quantum chips. Our future research topic is designing a new reversible gate and to implement reversible logic into a complete Quantum processor capable of ultra-high speed and infinitesimally low power computing.

References

[1.] K.Nagarjun, S.Srinivas, "A New Design of Multiplier using Modified Booth Algorithm and Reversible Gate Logic," International Journal of Computer Applications Technology and Research, Vol.2, Issue.6, pp.743-747, 2013

[2.] Sukhmeet Kaur, Suman and Manpreet Signh Manna, "Implementation of Modified Booth Algorithm (Radix 4) and its Comparison with Booth Algorithm (Radix-2)" Advance in Electronic and Electric Engineering. ISSN 2231-1297, Volume 3, 2013, pp. 683- 690.

[3.] Nishat Bano, "VLSI Design of Low Power Booth Multiplier" International Journal of Scientific & Engineering Research, Volume 3, Issue 2, 2012 ISSN 2229-5518.

[4.] K.V.Ganesh, T. Sudha Rani, P.N.Venkateswara Rao, K.Venkatesh," Constructing a low power multiplier using Modified Booth Encoding Algorithm in redundant binary number system" International Journal of Engineering Research and Applications Vol. 2, Issue 3, May-Jun 2012, pp.2734-2740.

[5.] Soojin Kim and Kyeongsoon Cho, "Design of high-speed modified booth multipliers operating at GHz range", World academy of science, Engineering and Technology 61, 2010.

[6.] P. Assady, "A new multiplication algorithm using high speed counters", European journal of scientific research, ISSN 1450- 216X Vol.26 No.3 (2009), pp.362-368.

[7.] G.Jaya Prada, N.C. Pant, "Design and Verification of Faster Multiplier", international journal of engineering Research and Applications(IJERA), Vol. 1, Issue 3, pp.683-686.