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Data Encoding Techniques for Lower Power Dissipation in Network on Chip using parity encoder

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ABSTRACT:

In this project, a low-power data encoding scheme is proposed. In general, system-on-chip (soc) based system has so many disadvantages in power-dissipation as well as clock rate wise such transfer the data from one system to another system in on-chip. At the same time, a higher operated system does not support the lower operated bus network for data transfer. However an alternative scheme is proposed for high speed data transfer. But this scheme is limited to SOCs. Unlike soc, network on- chip (NOC) has so many advantages for data transfer. It has a special feature to transfer the data in on-chip named as transitional encoder. Its operation is based on transitions of input data. At the same time it supports systems which are operated at higher frequencies. The proposed system yields lower dynamic power dissipation due to the reduction of switching activity and coupling switching activity when compared to existing system. The proposed schemes are general and transparent with respect to the underlying NoC fabric (i.e., their application does not require any modification of the routers and link architecture).

INTRODUCTION:

As VLSI technologies continue to scale, wire densities increases to support ever-small transistor geometries and causes on-chip wires to present increasing latency and energy problem. In particular, the high latency of cross-chip communication can still limit total performance by increasing the delay between on-chip unit. Such scalable bandwidth requirement can be satisfied by using on-chip packet-switched micro-network of interconnects, generally known as Network-on-Chip (NoC) architecture. The basic idea came from the traditional large-scale multi-processors and distributed computing networks. The scalable and modular nature of NoC and their support for efficient onchip communication lead to the NoC-based system implementations. In order to meet typical SoCs or multicore processing and basic module of network interconnection like switching logic, routing algorithm and the packet definition should be light-weighted to result in easily implemental solutions. Another approach to exceed such a limitation of communication and overcome such an enormous wiring delay in future technology is to adopt network-like interconnections which is called Network-on- Chip (NoC) architecture. Basic concept of such kind of interconnections is from the modern computer network evolution as mentioned before. By applying network-like communication which inserts some routers in-between each communication object, the required wiring can be shortened. Therefore, the switch-based interconnection mechanism provides a lot of scalability and freedom from the limitation of complex wiring. Replacement of SoC busses by NoCs will follow the same path of data communications when the economics prove that the NoC either reduces SoC manufacturing cost, SoC time to market, SoC time to volume, and SoC design risk or increases SoC performance. According to the

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NoC approach has a clear advantage over traditional busses and most notably system throughput. And hierarchies of crossbars or multilayered busses have characteristics somewhere in between traditional busses and NoC, however they still fall far short of the NoC with respect to performance and complexity. The success of the NoC design depends on the research of the interfaces between processing elements of NoC and interconnection fabric. The interconnection of a SoC established procedures has some weak points in those respects of slow bus response time, energy limitation, scalability problem and bandwidth limitation. Bus interconnection composed of a large number of components in a network interface can cause slow interface time though the influence of sharing the bus. In addition the interconnection has a defect that power consumption is high on the score of connecting all objects in the communication. Moreover it is impossible to increase the number of connection of the elements infinitely by reason of the limitation of bandwidth in a bus. As a consequence, the performance of the NoC design relies greatly on the interconnection paradigm .Though the network technology in computer network is already well developed, it is almost impossible to apply to a chip-level inter communication environment without any modification or reduction. For that reason, many researchers are trying to develop appropriate network architectures for on-chip communication. To be eligible for NoC architecture, the basic functionality should be simple and light-weighted because the implemented component of NoC architecture should be small enough to be a basic component constructing a SoC.

RELATED WORKS AND CONTRIBUTIONS

In the next several years, the availability of chips with 1000 cores is foreseen [6]. In these chips, a significant fraction of the total system power budget is dissipated by interconnection networks. Therefore, the design of power-efficient interconnection networks has been the focus of many works published in the literature dealing with NoC architectures. These works concentrate on different components of the interconnection networks such as routers, NIs, and links. Since the focus of this paper is on reducing the power dissipated by the links, in this section, we briefly review some of the works in the area of link power reduction. These include the techniques that make use of shielding [7], [8], increasing line-to-line spacing [9], [10], and repeater insertion [11]. They all increase the chip area. The data encoding scheme is another method that was employed to reduce the link power dissipation. The data encoding techniques may be classified into two categories. In the first category, encoding techniques concentrate on lowering the power due to self-switching activity of individual bus lines while ignoring the power dissipation owing to their coupling switching activity. In this category, bus invert (BI) [12] and INC-XOR [13] have been proposed for the case that random data patterns are transmitted via these lines. On the other hand, gray code [14], T0 [15], working-zone encoding [16], and T0-XOR [17] were suggested for the case of correlated data patterns. Application-specific approaches have also been proposed [18]–[22]. This category of encoding is not suitable to be applied in the deep sub micron meter technology nodes where the coupling capacitance constitutes a major part of the total interconnect capacitance. This causes the power consumption due to the coupling switching activity to become a large fraction of the total link power consumption, making the aforementioned techniques, which ignore such contributions, inefficient [23]. The works in the second category concentrate on reducing power dissipation through the reduction of the coupling switching [10], [22]–[30]. Among these schemes [10], [24]–[28], the switching activity is reduced using many extra control lines. For example, the data bus width grows from 32 to

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55 in [24]. The techniques proposed in [29] and [30] have a smaller number of control lines but the complexity of their decoding logic is high. The technique described in [29] is as follows: first, the data are both odd inverted and even inverted, and then transmission is performed using the kind of inversion which reduces more the switching activity. In [30], the coupling switching activity is reduced up to 39%. In this paper, compared to [30], we use a simpler decoder while achieving a higher activity reduction. Let us now discuss in more detail the works with which we compare our proposed schemes. In [12], the number of transitions from 0 to 1 for two consecutive flits (the flit that just traversed and the one which is about to traverse the link) is counted. If the number is larger than half of the link width, the inversion will be performed to reduce the number of 0 to 1 transitions when the flit is transferred via the link. This technique is only concerned about the self-switching without worrying the coupling switching. Note that the coupling capacitance in the state-of–the-art silicon technology is considerably larger (e.g., four times) compared with the self-capacitance, and hence, should be considered in any scheme proposed for the link power reduction.

PROPOSED ENCODING SCHEMES:

In this section, present the proposed encoding scheme whose goal is to reduce power dissipation by minimizing the coupling transition activity on the links of the interconnection network. Let us first describe the power model that contains the different components of power dissipation of a link.. One can classify four types of coupling transitions. A Type I transition occurs when one of the lines switches when the other remains unchanged. In a Type II transition, one line switches from low to high, other makes transition from high to low .A Type III transition corresponds to the case where both lines switch simultaneously. Finally, in a Type IV transition both lines do not change. The effective switched capacitance varies from type to type and hence, the coupling transition activity, is a weighted sum of different types of coupling transition contributions .Here, we calculate the occurrence probability for different types of transitions. Consider that flit (t − 1) and flit (t) refer to the previous flit which was transferred through the link and the flit is about to pass through the link, respectively. We consider only two adjacent bits of the physical channel. Sixteen different combinations of these four bits could occur (Table I). Note that the first bit is the value of the generic i th line of the link, whereas the second bit represents the value of its (i + 1)th line. The number of transitions for Types I, II, III, and IV are 8, 2, 2, and 4, respectively. For a random set of data, each of these sixteen transitions has the same probability.

Therefore, the occurrence probability for Types I, II, III, and IV are 1/2, 1/8, 1/8, and 1/4, respectively.

PARITY ENCODER:

As a widely used component of VLSI system, we always want to design a simpler PE with shorter propagation time and lower energy cost for optimized VLSI in characteristics of delay, energy consumption and complexity.
A **priority encoder** is a circuit or algorithm that compresses multiple binary inputs into a smaller number of outputs. The output of a priority encoder is the binary representation of the original number starting from zero of the most significant input bit. They are often used to control interrupt request by acting on the highest priority request. If two or more inputs are given at the same time, the input having the highest priority will take precedence. since it is superseded by higher-priority input. The output V indicates if the input is valid.

CONCLUSION

In this paper, a set of new data encoding schemes aimed at reducing the power dissipated by the links of an NoC. As compared to the

previous encoding schemes the rationale behind the proposed schemes is to minimize not only the switching activity, but also the coupling switching activity which is mainly responsible for link power dissipation. By using the proposed encoding schemes in NoC architecture their application does not require any modification neither in the routers nor in the links. As per the performance evaluation results, the proposed system has lower dynamic power dissipation than classical one.

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