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Optimized Reversible Vedic multipliers for High Speed Low Power Operations

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Abstract:
Multipliers are vital components of any processor or computing machine. More often than not, performance of microcontrollers and Digital signal processors are evaluated on the basis of number of multiplications performed in unit time. Hence better multiplier architectures are bound to increase the efficiency of the system. Vedic multiplier is one such promising solution. It's simple architecture coupled with increased speed forms an unparalleled combination for serving any complex multiplication computations. Tagged with these highlights, implementing this with reversible logic further reduces power dissipation. Power dissipation is another important constraint in an embedded system which cannot be neglected. In this paper we bring out a Vedic multiplier known as "Urdhva Tiryakbhayam" meaning vertical and crosswise, implemented using reversible logic, which is the first of its kind. This multiplier may find applications in Fast Fourier Transforms (FFTs), and other applications of DSP like imaging, software defined radios, wireless communications. For exiting system we are using 4-bit multiplier ,but the given proposed system we are implementing 8-bit multiplier using reversible vedic mathematics approach as shown in above diagram.

1.1 INTRODUCTION:

OVERVIEW OF PROJECT:

Multiplication is of immense importance in Digital Signal Processing (DSP) and Image Processing (IP). To implement the hardware module of Discrete Fourier Transformation (DFT), Discrete Cosine Transformation (DCT), Discrete Sine Transformation (DST) and modem broadband communications; large numbers of complex multipliers are required. Complex number multiplication is performed using four real number multiplications and two additions/ subtractions.In real number processing, carry needs to be propagated from the least significant bit (LSB) to the most significant bit (MSB) when binary partial products are added. Therefore, the addition and subtraction after binary multiplications limit the overall speed. Many alternative method had so far been proposed for complex number multiplication like algebraic transformation based implementation, bit-serial multiplication using offset binary and distributed arithmetic, the CORDIC (coordinate rotation digital computer) algorithm, the quadratic residue number system (QRNS), and recently, the redundant complex

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number system (RCNS) .Blahut et. al proposed a technique for complex number multiplication, where the algebraic transformation was used. This algebraic transformation saves one real multiplication, at the expense of three additions as compared to the direct method implementation. A left to right array for the fast multiplication has been reported in 2005, and the method is not further extended for complex multiplication. But, all the above techniques require either large overhead for pre/post processing or long latency. Further many design issues like as speed, accuracy, design overhead, power consumption etc., should not be addressed for fast multiplication.

In this work we formulate this mathematics for designing the complex multiplier architecture in transistor level with two clear goals in mind such as: i)Simplicity and modularity multiplications for VLSI implementations and ii) The elimination of carrypropagation for rapid additions and subtractions. Mehta et al. have been proposed a multiplier design using "Urdhva-tiryakbyham" sutras, which was adopted from the Vedas. The formulation using this sutra is similar to the modem array multiplication, which also indicating the carry propagation issues. Multiplier implementation in the gate level (FPGA) using Vedic Mathematics has already been reported but to the best of our knowledge till date there is no report on transistor level (ASIC) implementation of such complex multiplier.

The multiplier is fully parameterized, so any configuration of input and output word-lengths could be elaborated. Transistor level implementation for performance parameters such as propagation delay, dynamic leakage power and dynamic switching power consumption calculation of the proposed method was calculated by spice spectra using 90 nm standard CMOS technology and compared with the other design like distributed arithmetic parallel adder based implementation and algebraic transformation based implementation. The calculated results revealed (16, 16) x (16,16) complex multiplier have propagation delay only 4ns with 6.5 mW dynamic switching power.

EXISTING METHOD:

Booth's multiplication algorithm is a multiplication algorithm that multiplies two signed binary numbers in two's complement notation. The algorithm was invented by Andrew Donald Booth in 1950 while doing research on crystallography.

ALGORITHM

- Booth's algorithm examines adjacent pairs of bits of the N-bit multiplier Y in signed two's complement representation, including an implicit bit below the least significant bit, yi-1 = 0. For each bit yi, for i running from 0 to N-1, the bits yi and yi-1 are considered.

- Where these two bits are equal, the product accumulator P should be right shifted. Where yi = 0 and yi-1 should the multiplicand is added to P and then right shifted and where yi = 1 and yi-1 = 0, the multiplicand is subtracted from P and then right shifted. The final value of P is the signed product.

PROPOSED METHOD:

REVERSIBLE LOGIC GATES:

2.1 THEORETICAL OUTLINE:

Reversible computing was started when the basis of thermodynamics of information processing was shown that conventional

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irreversible circuits unavoidably generate heat because of losses of information during the computation. The different physical phenomena can be exploited to construct reversible circuits avoiding the energy losses. One of the most attractive architecture requirements is to build energy lossless small and fast quantum computers. Most of the gates used in digital design are not reversible for example NAND, OR and EXOR gates. A Reversible circuit/gate can generate unique output vector from each input vector, and vice versa, i.e., there is a one to one correspondence between the input and output vectors. Thus, the number of outputs in a reversible gate or circuit has the same as the number of inputs, and commonly used traditional NOT gate is the only reversible gate. Each Reversible gate has a cost associated with it called Quantum cost. The Quantum cost of a Reversible gate is the number of 2*2 Reversible gates or Quantum logic gates required in designing. One of the most important features of a Reversible gate is its garbage output i.e., every input of the gate which is not used as input to other gate or as a primary output is called garbage output. In digital design energy loss is considered as an important performance parameter. Part of the energy dissipation is related to non-ideality of switches and materials. Higher levels of integration and new fabrication processes have dramatically reduced the heat loss over the last decades. The power dissipation in a circuit can be reduced by the use of Reversible logic.

Reversible Function: The multiple output Boolean functionF(x1; x2; :::; xn) ofnBoolean variables is called reversible if:The number of outputs is equal to the number of inputs; Any output pattern has a unique pre-image. In other words, reversible functions are those that perform permutations of the set of input vectors.

3.1 MATHEMATICAL FORMULATION OF VEDIC SUTRAS:

The gifts of the ancient Indian mathematics in the world history of mathematical science are not well recognized. The contributions of saint and mathematician in the field of number theory, 'Sri BharatiKrsnaThirthaji Maharaja', in the form of Vedic Sutras (formulas) are significant for calculations. He had explored the mathematical potentials from Vedic primers and showed that the mathematical operations can be carried out mentally to produce fast answers using the Sutras. In this paper we are concentrating on "Urdhva-tiryakbyham",. A. "Urdhva-tiryakbyham " Sutra The meaning of this sutra is "Vertically and crosswise" and it is applicable to all the multiplication operations.

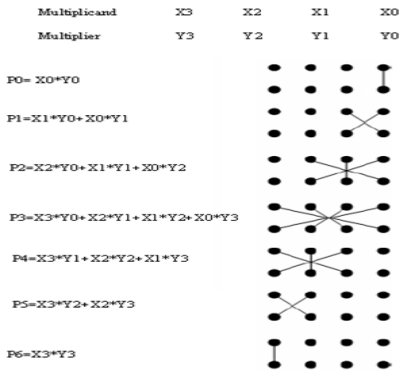

Fig 3.1: Multiplication procedure using "Urdhva-tiryakbyham " sutra.

4 IMPLEMENTATION OF VEDIC MULTIPLIER IN REVERSIBLE LOGIC:

The multiple output Boolean function F (x1 , x2 , ..., xn) of n Boolean variables is called reversible if

- The number of outputs is equal to the number of inputs;

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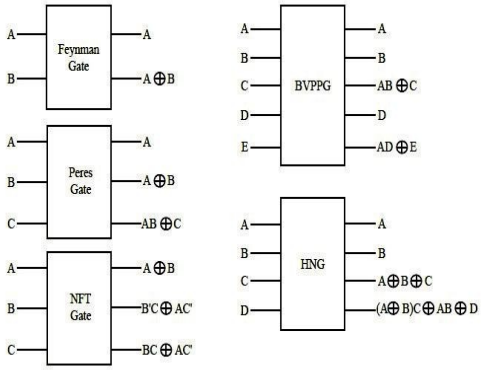
- Maps each input assignment to unique output assignment and vice versa.

3.5 BASIC REVERSIBLE GATES USED:



3.5.1 Important Parameters in Reversible Logic Circuit Designing:

Number of constant inputs (Gin):

The inputs that are added to an n*k function to make it reversible are called constant inputs.

Number of garbage outputs (Gout):

Garbage outputs are some outputs that are not used for further computations in the circuit.

Number of Gates (NOG):

The number of reversible gates used to realize the function.

Quantum Cost (QC):

The Quantum Cost (QC) of a reversible circuit is defined as the number of 1*1 or 2*2 reversible quantum or logic gates that are needed to realize the circuit.

Total logical calculations (circuit cost): One of the main factors of a circuit is its hardware complexity.

α = A two input EX-OR gate calculation.

β = A two input AND gate calculation .

δ = A NOT calculation.

T = Total logical calculation.

3.6Circuit Optimization:

\3.6.1 REVERSIBLE CIRCUIT:

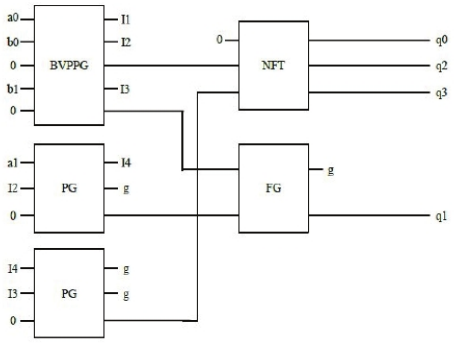


Fig 3.11 2*2 Multiplier.

2-bit multiplier is realized using partial products (earlier 2-bit multiplier is realized using k-map Boolean equations).

To reduce garbage output and constant inputs, tools gate is used in 2-bit multiplier circuit. Half adder gates (peres gates) and 2-cnot gate(xor gate) is used in circuit where no carry is generated in the circuit and Hence full adder gate can be replaced with them.

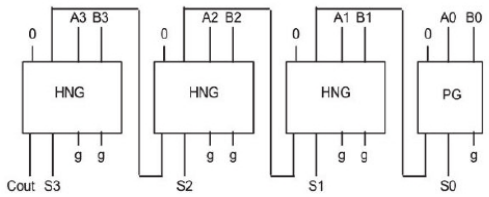


Fig.3. optimization of 4-bit full adder.

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By implementing the algorithm, reported quantum costs for reversible circuits from various sources, are compared with the existing results. It is found that the reported quantum cost is optimal in all the cases. In the thesis we have also provided optimized quantum cost for reversible multiplier circuits, reversible sequential circuits and ALU of hardware cryptography. We have not described them in this section as we have already mentioned them in context of synthesis designs based on a new reversible TR gate (TR refers to ThapliyalRanganathan). In as the quantum gates implementation of the TR gate was not known, only the upper bound on the quantum cost of the reversible subtractors units were established. In this work, we present a new design of the reversible half subtractor based on the quantum gates implementation of the reversible TR gate.The reversible TR gate is designed from 2x2 quantum gates such as CNOT and Controlled-V and Controlled-V + gates.

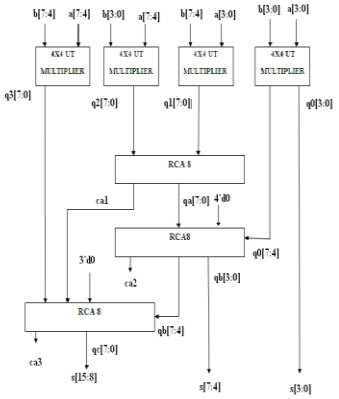


Fig:3.7 Architecture of 8*8 UT Multiplier.

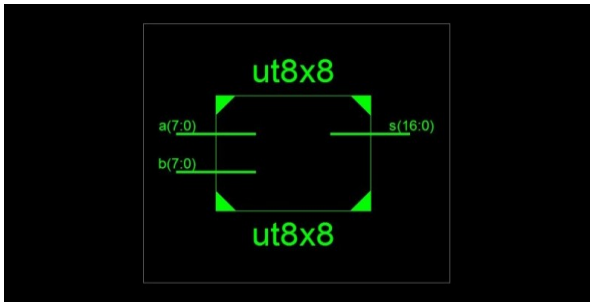
2.5 APPLICATIONS OF REVERSIBLE LOGIC:

Reversible computing may have applications in computer security and transaction processing, but the main long term benefit will be felt very well in those areas which require high energy efficiency, speed and performance it include the area like

- Low power CMOS.
- Quantum computer.
- Nanotechnology.
- Optical computing.
- DNA computing.
- Computer graphics.
- Communication.
- Design of low power arithmetic and data path for digital signal processing (DSP).
- Field Programmable Gate Arrays (FPGAs) in CMOS technology.
- Nano computing.
- Bio Molecular Computation.
- Laptop/Handheld/Wearable.
- Computers Spacecraft.

RTL SCHEMATICS AND RESULT

RTL FOR REVERSIBLE VEDIC MULTIPLIER FOR 8 BIT:



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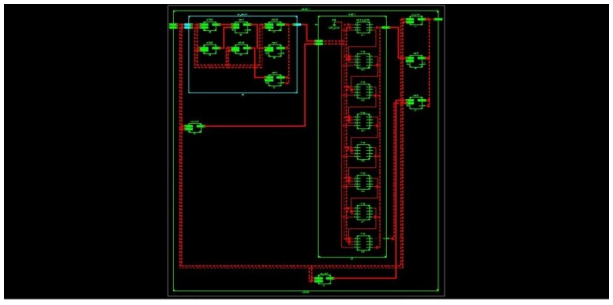
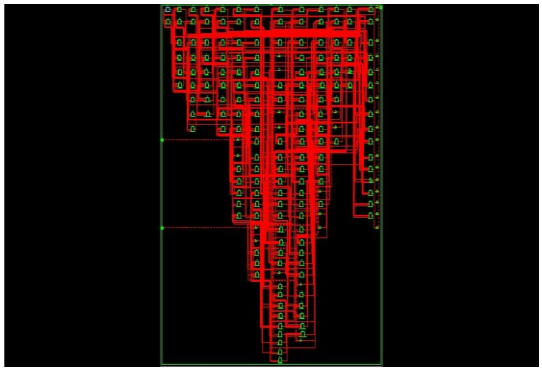
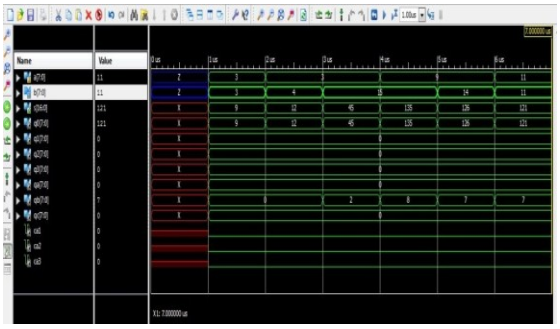
INTERNAL SCHEMATIC FOR REVERSIBLE VEDIC MULTIPLIER FOR 8 BIT:



7.3 TECHNOLOGY SCHEMATIC FOR REVERSIBLE VEDIC MULTIPLIER FOR 8 BIT:



7.4 SIMULATION RESULT:



DEVICE UTILIZATION SUMMARY FOR REVERSABLE VEDIC MUTIPLIER:

7.5 COMPARISON TABLES:

Comparison table for Booth multiplier specification of device xc3s500e-4fg320

Bits	Delay(ns)	Memory	Lut's	Power(mw)
8	36.481	191820	270	2.2036

Comparison table for reversible vedic multiplier specification of device xc3s500e-4fg320

Bits	Delay(ns)	Memory	Lut's	Power(mw)
8	21.72	190796	160	1.305

The above table's shows a comparison between the paper based technique and reversible vedic multiplier based technique in terms of delay in nsec , memory used ,number of lut's used for the design, and power in mw for 256 bits.

CONCLUSION:

The focus of this paper is mainly to design a low power high speed multiplier which is done by constructing the multiplier using reversible logic gates. The procedure is arried ut so as to yield an optimized design as compared to those in the literature. The efficiency of a reversible logic circuit is characterized in terms of parameters such as quantum cost, number of constant inputs,

garbage outputs and number o gates utilized to realize the logic implementations. Lower the value of these parameters more efficient is the design. In parameter called TRLIC had been proposed which is defined as sum of all cost metrics of the given design. The quantum cost is a parameter that directly reflects the delay of the quantum circuit. Also lower TRLIC implicitly means lower the quantuam cost, hence lower is the delay vice versa. Besides imbibing the design criterion that fan-out must be generated within the circuit, he proposed designs also reduce the TRLIC as compared to the previously proposed design. The further optimization of the circuit in terms of the total logical costs is under progress and is taken as future work.

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