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FPGA Implementation of SRAM Memory Testing Technique Using BISR Scheme

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Abstract
As RAM is major component in present day SOC, by Improving the yield of RAM improves the yield of SOC. So the repairable memories play a vital role in improving the yield of chip .Built-in self-repair (BISR) technique has been widely used to repair embedded random access memories (RAMs). If each repairable RAM uses one self contained BISR circuit (Dedicated BISR scheme), then the area cost of BISR circuits in an SOC becomes high. This, results in converse effect in the yield of RAMs. This paper presents a reconfigurable BISR (Re-BISR) scheme for repairing RAMs with different sizes and redundancy organizations. An efficient redundancy analysis algorithm is proposed to allocate redundancies of defective RAMs. In the Re-BISR, a reconfigurable built-in redundancy analysis (Re-BIRA) circuit is designed to perform the redundancy algorithm for various RAMs. A built-in self-repair (BISR) scheme for random access memories (RAMs) with 2-D redundancy has a built-in redundancy analyzer (BIRA) for allocating the redundancy. The BIRA typically has a cache-like element called local bitmap for storing the fault information temporary. The BISR reuses the local bitmap to serve as spare bits such that it can repair more faults. In addition, a row/column/bit redundancy analysis (RCB-RA) algorithm for a RAM with spare rows, spare columns, and spare bits is presented. The Re-BISR structure has been synthesized and found that the area cost when compared with the Dedicated BISR structure is very small. This paper is implemented using Verilog HDL. Simulation and Synthesis is done using ModelSim and Xilinx ISE Tools.

I. INTRODUCTION

The advancement in IC technology increases integration of memories. As SOC size is shrinking, the major area on SOC is occupied by embedded memories. Thus memories in chip will decide the yield of the SOC. Increase in yield of memories in turn increase the yield of SOC. In [1], SOC yield increases from 2% to 10% by improving the memory yield from 5% to 10%. The techniques used for yield improvements in memories are Built-In-Self Test (BIST) and BISR. Many algorithms are proposed for spare allocation for defected memories. The redundancy is of 1D (only spare row or column) [3-4] or 2D (spare row and spare column) [5-7]. Hardware redundancy technique is one effective technique for enhancing the yield of RAM. Memory built-in self-repair (BISR) Techniques have been widely used to execute the fault detection, fault location, and redundancy allocation for RAMs with redundancies in a SoC [3].

A BISR scheme for RAMs with 2-D redundancy, i.e., spare rows and spare columns/IOs, typically consists of a built-in self-test (BIST) circuit, a built-in redundancy analyzer (BIRA), and a reconfiguration mechanism. The BIST is used to detect and locate faulty cells of the RAM under test. The reconfiguration mechanism is used to swap the defective element
with the spare element. The BIRA is used for optimizing the allocation of the 2-D redundancy. The BIRA can collect fault information during the test process and allocate the available redundancies on the fly. Therefore, the BIRA has a heavy impact on the repair efficiency of the BISR scheme. The complexity of the redundancy allocation for RAM with 2-D redundancy is an non-deterministic polynomial-time-hard problem. However, the number of redundancies of a RAM typically is small. Thus, it is still feasible to allocate Redundancies using an exhaustive search algorithm. Many BIRA

schemes for RAMs with 2-D redundancy have been proposed [3]–[9], [11]. They can roughly be divided into two classes: optimal and non-optimal redundancy analysis (RA) schemes. An optimal RA scheme can find a repair solution if the repair solution exists. For example, the BIRA schemes reported in [3]–[8], use different algorithms to achieve an optimal repair rate (RR). However, an optimal RA scheme needs either high area cost or long test time. A heuristic RA scheme attempts to obtain a compromise between the RR and the cost of area and test time. For example, the BIRA schemes reported in [9], [11] and use heuristic RA algorithms to allocate redundancies. A BIRA circuit realizing an optimal or a heuristic RA algorithm typically needs a cache like storage element to store the positions of faulty cells. Since only the positions of faulty cells in a RAM should be stored, a cache-like storage element can be considered as a compressed device image memory. The cache-like element can support the functions of data storing and parallel address comparison. The cache-like element in many BIRA schemes is called a local bitmap [11]. In this paper, therefore, we use the local bitmap to represent the cache-like element. In this paper, we propose a repair efficiency BISR scheme by reusing local bitmap as the bit redundancy. Thus, the available redundancy resource is increased, which can boost the repair efficiency. An RA algorithm for a RAM with 2-D and bit redundancies is proposed to allocate redundancies as well.

In [2], a reconfigurable BIST architecture is proposed by adding some data processing unit and address processing unit. Where the data width and address width of BIST is variable according to the RAM which is being tested. In [3], this scheme uses multiple bank cache like memory for repairs. Remapping scheme and redirecting read/write request from faulty part to spare elements. In [4], Single spare column is used to replace multiple single cell faults by selectively decoding row address bits andsending control signals for multiplexers. This scheme is efficient only for single defects in single. The repair rate and area cost of the Built In Redundancy Analysis (BIRA) is mainly depends on the redundancy organization. The redundancy organization memory is divided into various segments. In which spare row and columns are used differently. Spare rows are used to replace entire row in the memory and the columns are divided in several spare column groups. Here the access time and area cost is induced due to additional multiplexers. However different redundancy organization will lead to different area cost and repair rate. Since most of the memory faults are single cells, spare words are very efficient in reducing area. In this, the spare rows and spare columns are virtually divided into spare row blocks and spare column group blocks.SOC contains different RAMs with different address and data widths. If every RAM in SOC contains different repair circuit, area of the repair circuit increases. In order to reduce the area cost of repair circuit, reconfigurable repair circuit is used in which a single repair circuit is used for repairing multiple memories with different size and redundancies.

II. BLOCK DIAGRAM OF BISR ARCHITECTURE FOR REPAIRABLE RAM

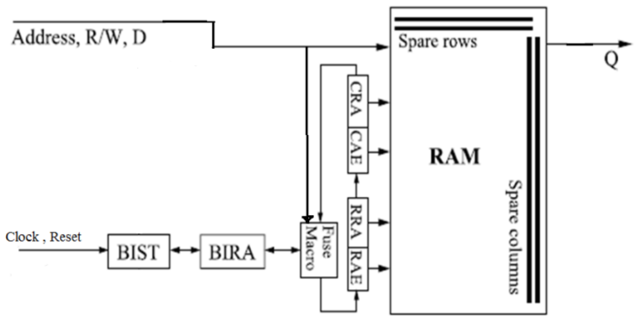

Fig1: BISR block diagram for a repairable RAM

1) Repairable RAM: A RAM with redundancies and Reconfiguration circuit. Fig. 2 depicts an example of an 8*8bit-oriented RAM with 1 spare row and 1 spare column. If a spare row is allocated to replace a defective row, then the row address of the defective row is called row repair address (RRA). Then a decoder decodes the RRA into control signals for switching row multiplexers to skip the defective row if the row address enable (RAE) signal is asserted. There configuration of the defective column and the spare column is performed in a similar way, i.e.,

give a column repair addresses (CRA) and assert the column address enable signal to repair the defective column using the spare column.

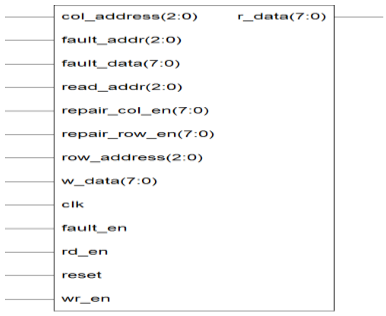

Fig.2: Repairable RAM block diagram

2) Built-in Self-Test (BIST) Circuit. It can generate test patterns for RAMs under test. While a fault in a defective RAM is detected by the BIST circuit, the faulty information is sent to the BIRA circuit.

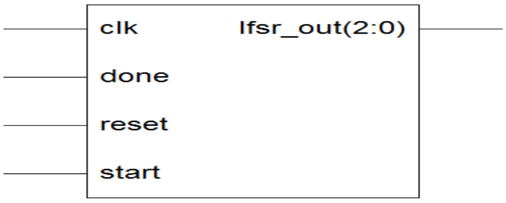

Fig3: BIST LFSR block diagram

3) BIRA Circuit. It collects the faulty information sent from the BIST circuit and allocates redundancies according to the collected faulty information using the implemented redundancy analysis algorithm.

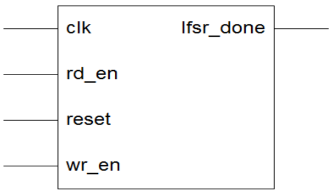

Fig4: BISR block diagram

4) Fuse Macro: It stores repair signatures of RAMs under test. Figure5 shows the conceptual block diagram of a typical implementation of fuse macro. The fuses of the fuse box can be implemented in different technologies, e.g., laser blown fuses, electronic-programmable fuses, etc. The fuse register is the transportation interface between the fuse box and the repair register in the repairable RAM. The fuse macro typically consists of non-volatile storage cells that are used to store the repaired addresses when the power is turned OFF.

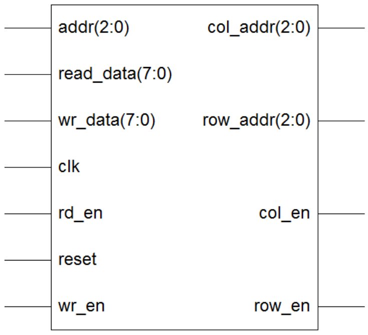

Fig5: Fuse Macro block diagram

The BISR circuit consists of a BIST circuit, a BIRA, and reconfiguration mechanism. The BIST can generate test patterns to test the RAM and locate the faulty cells. The reconfiguration mechanism can swap the defective elements with the spare elements, which is usually realized by multiplexers and storage elements. The control signals of the multiplexers are stored in registers. The registers include row repair address (RRA), column repair address(CRA), row address enable (RAE), and column address enable (CAE) registers. The fuse macro typically consists of non-volatile storage cells that are used to store the repaired addresses when the power is turned OFF. The BIRA can optimize the allocation of 2-D redundancy for replacing the faulty cells in a defective RAM. Typically, a BIRA uses a local bitmap to collect fault information and then allocates redundancy using the implemented RA rules according to the corrected faults. The bit address is used to identify the location of faulty bit in a faulty word. A local bitmap can be considered as a compressed device image memory. The local bitmap is called bitmap for short.

III. MODIFIED BLOCK DIAGRAM OF BIRA

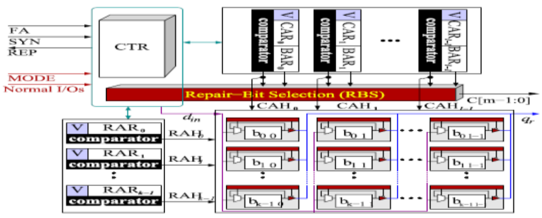

Fig6: modified block diagram of BIRA with $k \times l$-bit bit map

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Some of interaction signals between the BIST and BIRA are shown in the figure6, which are faulty address (FA), syndrome (SYN), and repair (REP). Once the BIST detects a fault, the corresponding FA and Hamming syndrome are sent to the BIRA through the FA and SYN, where Hamming syndrome is defined as the modulo-2 sum of the fault-free data output vector and the output vector from the RAM under test. The signal REP is used to indicate the RA result of the BIRA is repairable or un-repairable. The controller (CTR) handles the faulty address and the encoding of bit address according to Hamming syndrome from the BIST.A mode setting signal MODE is used to set the BIRA to be operated in normal or test mode. Normal IOs of the RAM are connected to the BIRA as well. In test mode, the operation of the modified bitmap is the same as that of the original bitmap.

In normal mode, the operation of the modified bitmap is described as follows. If the RAM is accessed, the applied address is compared with the stored addresses including the row and column addresses. If one of stored row addresses is the same as the row address of the input address, then the corresponding row address hit (RAH) signal is set to 1, i.e., RAHi= 1. Similarly, if one of stored column addresses is the same as the column address of the input address, then the corresponding column address hit (CAH) signal is set to 1, i.e., CAHj= 1. Therefore, when the accessed address is matched with one of the stored addresses, i.e., RAHi= 1 and CAHj= 1, one bit of the addressed word is repaired by the spare bit.

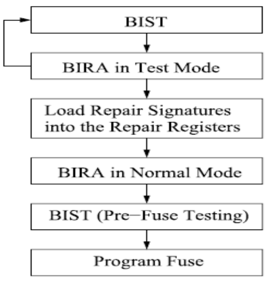
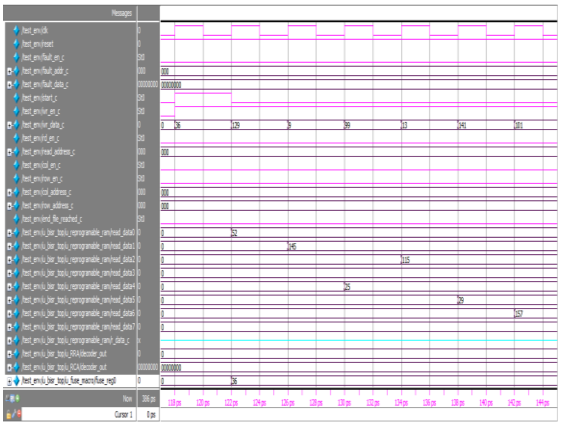


Fig7: Test and redundancy allocation flow.

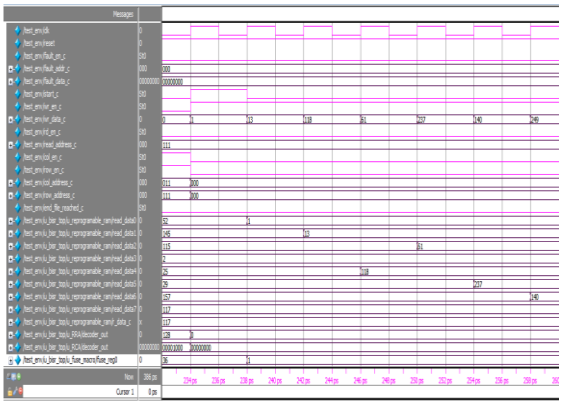
First, the BIST tests the RAM under repair and the BIRA is in test mode. If a fault is detected, the fault information is sent to the BIRA for analysis. This process is iterated until the testing of the RAM is completed. If the RAM is repairable, then the repair signatures are loaded into the repair registers and the BIRA are set to normal mode. Subsequently, the BIST is used to test the repaired RAM again for the prefuse testing. If the prefuse testing is completed and the repaired RAM is fault-free, then the fuses in the fuse macro can be programmed and the test and repair process is completed. Here, we assume that the electrically programmed fuse (e-fuse) is used to realize the fuses in the fuse macro [34]. In addition, the fuse macro has a fuse CTR to handle the programming of e-fuse. The e-fuse enables the function of on-chip self-repair, whereby repair data is programmed into e-fuse when the test and repair process is completed. Therefore, if the BIST and the fuse CTR are asserted by the power on reset signal, on-chip self-repair can be achieved.

IV.EXPERIMENTAL RESULTS

MODEL SIM: Simulation result of BISR in modelsim



Here the input data, write data and output data read are different. Because of fault



By introducing Re-BISR scheme the fault is detected and repaired

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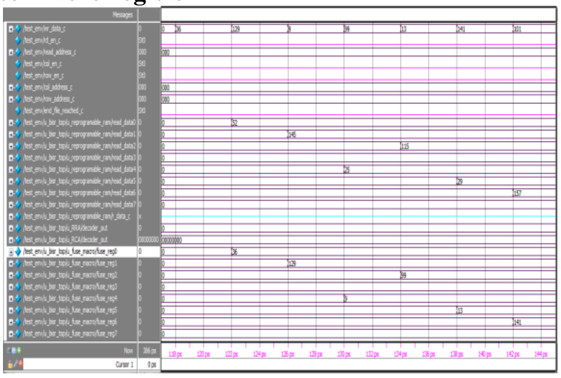
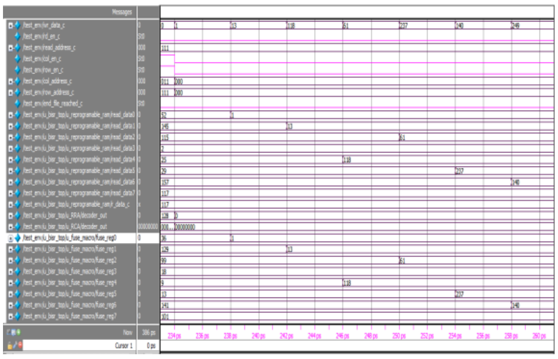
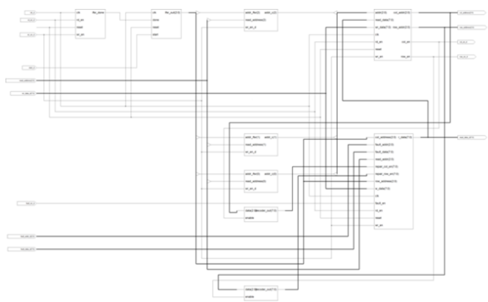
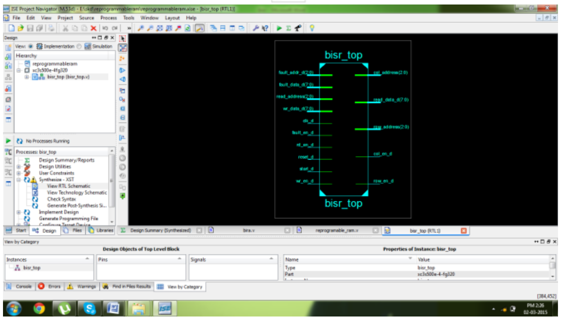
Fuse Macro register



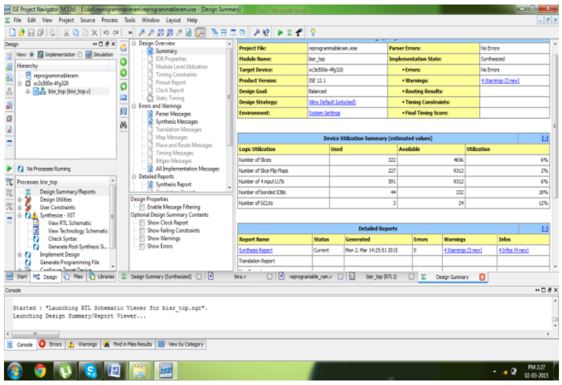


Xilinx synthesis report

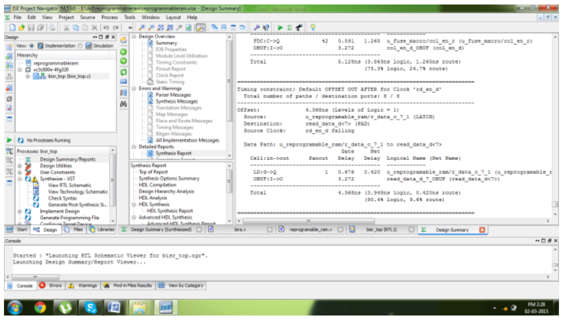




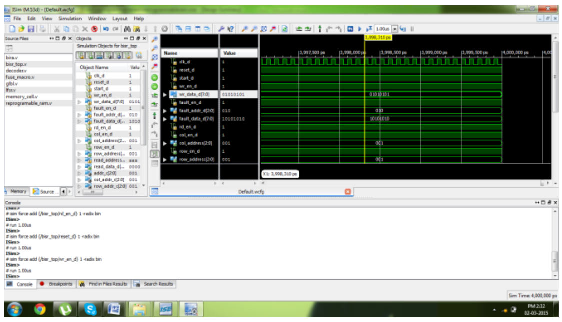
RTL SCHAMATIC



AREA CALCULATION



DELAY CALCULATION



WAVE FORMS

V. CONCLUSION

A reconfigurable BISR(Re-BISR) scheme for repairing RAMs with different sizes and redundancy configurations has been presented in this paper .An efficient BIRA algorithm for 2-D redundancy allocation has also been introduced. The yield of memory plays major role in SOC designs, the proposed Re-BISR effectively increases compare to traditional yield. The Re-BISR scheme can be used for repairing multiple RAMs.

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