International Journal of Research (IJR)
e-ISSN: 2348-6848, p- ISSN: 2348-795X Volume 2, Issue 08, August 2015
Available at http://internationaljournalofresearch.org

A Unique Low-Power Implementation of 4-2 Compressor in High Speed Multiplier

[1] Sowjanya Kanna; [2]A.H.Sharief & [3]S.Neelima

[1]M.Tech (VLSI & Embedded System),
[2]Assoc.Professor,
[3]HOD, Assoc.Proffesor,
Gandhiji Institute of Science & Technology (Gist) – JNTU Kakinada Affiliated,
Gattubhimavaram (Village),Jaggayyapet (Mandal),Krishna (District),Andhra Pradesh, India.

Abstract-

A Multiplier is one of the key hardware elements in most digital and high performance systems such as FIR filters, Digital Signal Processors (DSPs), Microprocessors etc., A low-power high speed 4-2 compressor circuit is used for fast digital arithmetic integrated circuits. The 4-2 compressor has been widely employed for multiplier realizations. A Wallace tree multiplier is an improved version of tree based multiplier architecture. It uses 4:2, 5:2 compressors and a Carry Select Adder (CSA) to reduce the latency and power consumption. Multiplier using 4-2 Compressors produces quick results, especially for use in Digital Signal Processors and in Microprocessors. This multiplier uses a new partial-product reduction format which consecutively reduces the maximum output delay. The 4-2 Compressor used is made from high-speed and low-power XOR-XNOR module and transmission gate based Multiplexer. On using these Compressors in the multiplier, the number of interconnections gets reduced, which further produces quick results, along with consuming lesser power. The concept of these compressors for improving the performance of the multiplier is done on transistor level. The performance of these different designs is compared and the observation is that the usage of compressor makes the process more energy efficient and faster as compared to the traditional methods. The delay and power-delay product (PDP) is compared with earlier Wallace and Dadda Multipliers, implemented with 4-2 Compressors and without compressors, and is proven to have minimum delay and PDP.

Keywords-4-2 compressor; full adder; multiplier; power delay product; XOR-XNOR module

1. INTRODUCTION

In recent years, the focus of VLSI design is mainly on high performance microprocessors. With the emerging need for high speed VLSI devices, there is a continuous demand for high speed multipliers, as they are the core elements in several Computer Arithmetic circuit applications like Image Processing, Digital Signal Processors like in Filters, Convolutors; Multimedia like in Oscillators and Microprocessors like in ALU's. Multipliers are one of the most significant blocks in computer arithmetic and are generally used in different digital signal processors. In most of the VLSI systems, multiplier directly lies in the critical path. So, for these reasons, the designers are now focusing on multipliers of high speed and low power delay product. The performance of multipliers helps in determining the processor's speed of running and performance of several DSP algorithms. Full adder is the basic functional block for most of the arithmetic operations such as compressors, comparators, parity checkers, multipliers, etc. It is the core of many other useful operations such as multiplication, division, subtraction, exponentiation, address calculation and it can significantly influence the overall performances of the system.

Generally there are three stages of multipliers. They are Generation of Partial products, Addition of partial products and final addition stage. In the first stage, both the multiplier and the multiplicand are multiplied bit by bit to generate the partial products. The second stage is the most important, as it is the

International Journal of Research (IJR)
e-ISSN: 2348-6848, p- ISSN: 2348-795X Volume 2, Issue 08, August 2015
Available at http://internationaljournalofresearch.org

most complicated and determines the speed of the overall multiplier. The addition of the partial products contributes most to the overall delay, area and power consumption, due to which the demand for high speed and low power compressors is continuously increasing. The second phase - partial product reduction phase consumes most of the power and is responsible for overall critical path delay. Therefore in order to optimize this stage, Compressors can be used for partial product accumulation. Column Compression (CC) is the technique used to reduce the power consumption and delay in multiplier design, in which the 3-2, 4-2 and 5-2 compressors used in multipliers are accumulated with partial products column–wise. A 3-2 compressor circuit is also known as full adder cell. These compressors are internally made of XOR-XNOR and multiplexer modules and their improved design will contribute a lot towards the overall system performance. Optimized design of these XOR-XNOR gates can improve the performance of multiplier circuit. A new XOR-XNOR module has been proposed and 4-2 compressor has been implemented using this module. A new technique of partial-product reduction using 4-2 Compressors in multipliers have been used based on pre-determined sequence of matrix heights to give minimum number of partial-product reduction stages, with reduces delay and PDP of multiplier and has lesser transistor count.

2. COMPRESSORS

Compressors of type 3-2 and 4-2 are generally used for performing additions. Higher order Compressors can be designed by interconnecting lower order compressors, like a 4-2 compressor can be made from two full adders. In multiplier design, 4-2 Compressor is ideal for constructing regularly structured Wallace tree with less complexity. Usage of compressors will help to have fewer interconnections.

2.1 Framework of Compressors

There are different architectures and designs of 4-2 compressor circuits. These are mainly composed of two types of circuits: XOR-XNOR circuits and multiplexers (MUX). XOR-XNOR gates are also used as building blocks in Parity Checkers, Oscillators, and Comparators etc. Static CMOS based XOR-XNOR uses both pMOS and nMOS consumes many transistors and larger area. Static XNOR-XOR also uses Complementary CMOS style but they both consume large power and not used at low voltages. The XOR-XNOR with feedback transistors can be used at low voltages but input load is doubled, causes slow response if cascaded and area increased. XOR-XNOR shown in Fig 1 uses only 8 transistors and can operate well at low supply voltages. It also provides good driving capability and has high speed performance than the prevailing three XOR-XNOR gates.

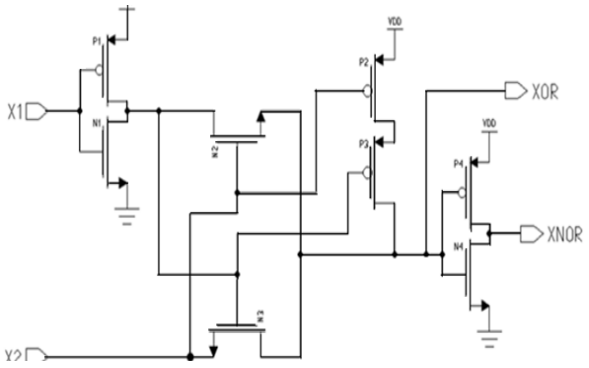

Fig.1. Circuit diagram of XOR-XNOR

The Multiplexer (MUX) module is used in Compressors for Carry generation. The Multiplexer output is based on Select lines (S). If there are 2 data inputs, it is called 2 to 1 MUX. Static MUX using Complementary CMOS style transistors and MUX with transmission gates and output buffer both consume larger area and delay. So, in Compressors, MUX using transmission gates consuming 6 transistors as shown in Fig 2 can be used, in low power cells for faster results within low area.

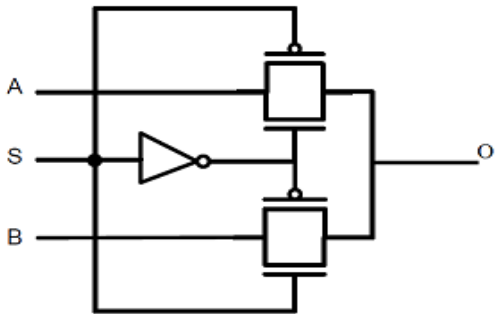

Fig.2. MUX with transmission gates

2.2 Design of a 4-2 Compressor

Mostly 3-2, 4-2 Compressors are generally used. A 3-2 Compressor is also known as a Full Adder Cell with three equal weighted inputs and outputs as Sum,

International Journal of Research (IJR)
e-ISSN: 2348-6848, p- ISSN: 2348-795X Volume 2, Issue 08, August 2015
Available at http://internationaljournalofresearch.org

Carry. 4-2 Compressor can be built from 2 Full-Adders connected serially. It has 5 inputs called X1, X2, X3, X4 and Cin and produces 3 outputs Sum, Carry and Cout, where Carry and Cout have one bit higher weight than others. In this, the Cin and Cout bits are independent to each other. By connecting two full adders serially, a 4-2 Compressor can be implemented. The Block diagram of a 4-2 compressor is shown in Fig. 3

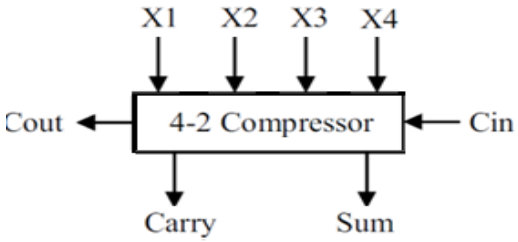

Fig.3. Block diagram of 4-2 Compressor

Different structures of 4-2 compressors are used and these are governing by the basic equation as follows:

$$X1+ X2 + X3 + X4 + Cin = Sum + 2\cdot (Carry + Cout)$$

The 4-2 compressor design has been implemented using following methods:
Conventional method using two full adders as shown in fig 4

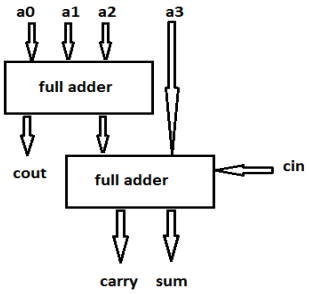

Fig.4 Conventional 4:2 compressor

Using XOR-XNOR and modified MUX that is MUX* as shown in Fig. 5

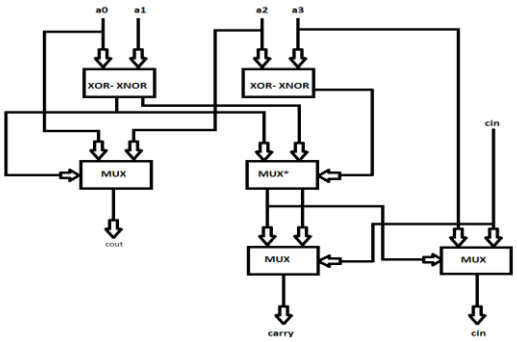

Fig.5 Logic decomposition of 4-2 compressor

3. BASIC TREE MULTIPLIERS

The tree multipliers are also called parallel multipliers. They are performance efficient in general. In these tree multipliers, first phase of partial product generation is implemented by multiplying each multiplicand bit with the multiplier bit by AND operation. Tree multipliers are meant for adding a number of partial products at a time and so further reducing the number of steps needed to reduce the partial products into 2 rows of final intermediate results. The Tree multipliers like Wallace and Dadda differ mainly in the Partial product reduction phase based on the type of reduction algorithm used. The last addition phase performs addition of the reduced bits using Carry Propagate Adder (CPA) to produce the final result.

3.1 Wallace Tree Multiplier

Wallace Tree multiplier is a fast process for multiplying two numbers that was introduced by Wallace. Wallace Tree multiplier accumulates partial products column-wise into three and two bits and gives them to Full-Adders and Half-Adders respectively to reduce as Sum, Carry bits. The bits that do not belong to these adders are bypassed to next stage. Sum bit is given to next stage of same weight and carry is propagated to a column of one-bit higher order in next stage. Wallace accumulates as many bits as possible into adders. At each stage, this process is continued until the stage height is reduced to 2 rows. The Wallace tree 8x8 multiplier along with its reduction stage is totally comprised with five stages. Stage 5 uses Carry Propagate Adder. A total of 47 Full-adders and 17 Half-adders are used for Wallace 8x8 multiplier.

International Journal of Research (IJR)
e-ISSN: 2348-6848, p- ISSN: 2348-795X Volume 2, Issue 08, August 2015
Available at http://internationaljournalofresearch.org

3.2 Dadda Tree Multiplier

Dadda proposed an algorithm with predetermined sequence of matrix (stage) heights for NxN multipliers to have reduced number of reduction stages. It is developed by working back from two row stage. The height of each intermediate stage is limited to floor value of 1.5 times the height of the successor stage i.e., Height of stage i = (3/2) * Height of stage i+1. Then sequence of stage heights are 2,3,4,6,9,13...

The main difference between Wallace and Dadda multipliers is that, Wallace uses adders wherever possible but Dadda uses adders wherever necessary in order to maintain the predetermined stage height. The critical path is varied and so, delay of Dadda is less than that of Wallace as Dadda is intended to save number of adders. The delay and power delay product (PDP) comparison of Wallace and Dadda 6X6 and 8X8 multipliers are shown in below table.

Type of Multiplier	NxN	Delay (nS)	PDP (10-14J)
Wallace	6x6	4.724	73.17
Dadda		1.907	31.83
Wallace	8x8	11.47	512
Dadda		9.242	371.8

Table1. Delay and PDP Comparison in Wallace and Dadda Multipliers

4. WALLACE MULTIPLIER BASED ON 4-2 COMPRESSORS

Compressors when used in partial product reduction phase in multipliers will help in having lesser number of interconnections and adder cells. In high speed multipliers, usage of compressors instead of conventional full and half adders lead to quick output generation and as well the number of reduction stages gets reduced. Compressors of higher order can be used in multiplier design. When compared to two full adders, a 4-2 Compressor has lesser delay and power consumption as the interconnections are reduced. A CC multiplier, with equal size multiplicand and multiplier bits and built with compressors have considerable flexibility in allocating the number of cells to different partial product reduction stages. The 4-2 compressor is well suitable in Multiplier's design as that require fewer transistor count and it also provides better performance.

4.2 Design of Wallace Tree Multiplier using 4-2 Compressors

On using compressors the number of reduction stages in Wallace multiplier gets reduced to 3, instead of 5 stages when only half and full adders are used. On using compressors in partial product reduction, the number of reduction stages gets reduced to 3, rather than 5 stages when only half adders and full adders are used. After stage3, the result is given to a Carry Propagate Adder (CPA). The power, delay and in addition the PDP also gets reduced. The Multiplier uses 31 no. of 4-2 Compressors, 24 full adders and 20 half adders. This Wallace tree has lesser delay compared to the one which does not use 4-2 compressors.

5. CONCLUSION

A low power and high speed Wallace Tree multiplier has been used for having high performance, which uses 4-2 compressors made from an XOR-XNOR gate of good driving capability, high speed and low power and Multiplexer made of transmission gates. This multiplier uses a reduction format with predetermined stage heights for having quick results and further minimum power delay product (PDP). This present Wallace multiplier shows optimal power and performance against normal Wallace multiplier and basic Dadda Tree multiplier implemented without compressors. The reduction format can also be applied to higher order NxN multipliers for high speed results.

6. REFERENCES

[1] Z. Wang, G. A. Jullien, and W. C. Miller, "A new design technique for column compression multipliers," IEEE Trans. Comput., vol. 44, pp. 962–970, Aug. 1995.

[2] Manoj Kumar, Sandeep K. Arya, Sujata Pandey, "Single bit full adder design using 8 transistors with novel 3 transistors XNOR gate," International Journal of VLSI

[3] Riya Garg, Suman Nehra, and B. P. Singh, "Low Power Full Adder using 9T Structure," International Journal on Recent Trends in Engineering and Technology, Vol. 8, Issue No. 2, pp. 52-55, 2013.

[4] N. Sureka, Ms.R.Porselvi, Ms.K.Kumuthapriya, "An Efficient High Speed Wallace Tree Multiplier", Information Communication and Embedded Systems (ICICES), pp. 1023 - 1026, 2013.

[5] S.F. Hsiao, M.R. Jiang, J.S. Yeh, ―Design of high low power 3-2 counter and 4-2 compressor for fast multipliers, Electronic Letters, Vol. 34, No. 4, pp. 341-343, 1998 http://en.wikipedia.org/wiki/Wallace_tree

[6] Naveen Kr. Gahlan, Prabhat Shukla, Jasbir Kaur ―Implementation of Wallace Tree Multiplier using Compressor, Int.J. Computer Technology & Applications, Vol 3 (3), pp.1194-1199, May – June 2012.

[7] P.N.V.K. Hasini, T. Krishna Murthy "A Novel high-speed transistorized 8x8 Multiplier using 4-2 Compressors" International Journal of Engineering Research and General Science Volume 3, Issue 2, Part 2, pp. 359-365, March-April 2015.

[8] S. Veeramachaneni, K. M. Krishna, L. Avinash, S. R. Puppala, and M. Srinivas, "Novel architectures for high-speed and low-power 3-2, 4-2 and 5-2 compressors," in VLSI Design. Held jointly with 6th International Conference on Embedded Systems, 20th Intern. Conference on, pp. 324–329, Jan. 2007.

[9] BaranD.Aktan M., &Oklobdzija, V.G. (2010). Energy Efficient Implementation of Parallel CMOS Multipliers with Improved Compressors.In the proceedings of International Symposium on Low-Power Electronics and Design (ISLPED), ACM/IEEE.

[10] R. Marimuthu, S. Balamurugan, Bala Krishna Tirumala, & P.S. Mallick (2012). FPGA Implementation of High Speed Multiplier using Higher Order Compressors. 2012 International Conference on Radar, Communication and Computing (ICRCC).

[11] Chip-Hong Chang, JiangminGu, &Mingyan Zhang (2004). Ultra Low-Voltage Low-Power CMOS 4-2 and 5-2 Compressors for Fast Arithmetic Circuits. IEEE Transactions on Circuits and Systems—i: regular papers, vol. 51, no. 10.

[12] Kelly Liew Suet Swee, & Lo HaiHiung (2012). Performance Comparison Review of 32-Bit Multiplier Designs. In the proceedings of 4th International Conference on Intelligent and Advanced Systems (ICIAS2012).

[13] M. Margala and N. G. Durdle, "Low-power low-voltage 4-2 compressors for VLSI applications," in Proc. IEEE Alessandro Volta Memorial Workshop Low-Power Design, pp. 84–90, 1999.

[14] D. Radhakrishnan, A.P. Preethy, "Low Power CMOS pass logic 4-2 compressor for high speed multiplication", Proceedings of 43rd IEEE Midwest Symposium on Circuits and Systems, Vol. 3, pp. 1296-1298, 2000.

[15] Pallavi Devi Gopineedi, Himanshu Thapliyal, M.B Srinivas and Hamid R. Arabnia, "Novel and Efficient 4:2 and 5:2 Compressors with Minimum number of Transistors Designed for Low-Power Operations", ESA, pp.160-168, 2006.