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Implementation and Comparison of Effective Area Efficient Architectures for CSLA

[1] Yamarthi Yogananda Prasad; [2] BS.Madhuri & [3]S.Neelima
[1]M.Tech (VLSI & Embedded System),
[2]Asst.Professor,
[3]HOD, Assoc.Proffesor,
Gandhiji Institute of Science & Technology (Gist) – JNTU Kakinada Affiliated,
Gattubhimavaram (Village),Jaggayyapet (Mandal),Krishna (District),Andhra Pradesh, India.

Abstract:

Carry Select Adder (CSLA) is one of the fastest efficient adders which are used in many data-processing processors to perform fast arithmetic functions. CSLA is called efficient adder because of less delay and reduced size. In this paper 16 bit, 32 bit, 64 bit and 128 bit Regular Linear CSLA, Modified Linear CSLA, Regular Square-root CSLA (SQRT CSLA) and Modified SQRT CSLA architectures have been developed and compared. Comparing the Regular Linear CSLA with Regular SQRT CSLA, the Regular SQRT CSLA has reduced area as well as comparing the Modified Linear CSLA with Modified SQRT CSLA The proposed work conveys that it uses a simple and efficient gate-level modification to significantly reduce the area and power of the CSLA. The performance factors of the proposed design are evaluated in terms of delay, area, power and their products by simulation tool and implemented in FPGA kit. The results analysis shows that the proposed modified BEC CSLA structure is better than the regular BEC SQRT CSLA. This paper introduces an unique method that replaces the BEC using common Boolean logic. This paper proposes an efficient method which replaces the BEC using D latch. Experimental results are compared and the result analysis shows that the proposed architecture achieves the three folded advantages in terms of area, delay and power.

Keywords: Carry Select Adder(CSLA); area efficient; Field Programmable gate array(FPGA); Boolean Logic; Square Carry select adder root CSLA(SQRT CSLA)

1. INTRODUCTION

Area and power have major role in the designing of integrated circuit because of the increase in popularity of portable systems as well as the rapid growth of power density in VLSI circuits. Addition usually influences strongly on the overall performance of digital systems and a crucial arithmetic function. Low power and area efficient addition and multiplication have always been a fundamental requirement of high performance processors and systems. Designing efficient adder is the most difficult problem for researchers in VLSI design.

The carry-select adder (CSLA) provides a compromise between small area but longer delay ripple carry adder (RCA) and larger area with shorter delay carry look-ahead adder[1].CSLA uses multiple pairs of ripple carry adder (RCA) to generate partial sum and carry by considering carry input Cin=0 and Cin=1, then the final sum and carry are selected by multiplexers (mux) .Design of area efficient high speed data path logic systems are one of the most essential areas of research in VLSI.

In digital adders, the speed of addition is controlled by the time required to propagate a carry through the adder. The CSLA is used in many computational systems to alleviate the problem of carry propagation delay by independently generating multiple carries and then select a carry to generate the sum [2].The CSLA is not area efficient because it uses multiple pairs of Ripple

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Carry Adders (RCA) to generate partial sum and carry by considering carry input Cin=0 and Cin=1.Then the final sum and carry are selected by the multiplexers (mux).

The basic idea of this work is to use Binary to Excess-1 Converter (BEC) instead of RCA with Cin=1 in the regular CSLA to achieve lower area and power consumption [3]. The main advantage of this BEC logic comes from the lesser number of logic gates than the n-bit Full Adder (FA) structure. In this paper, we proposed the modified BEC SQRT CSLA architecture. Youngwood Kim and Lee Sup Kim introduced a multiplexer based add one circuit was proposed to reduce the area with negligible speed penalty.

The modified CSLA using BEC [4] has reduced area and power consumption with slight increase in delay. The basic idea of the proposed architecture is that which replaces the BEC by D latch with enable signal. The proposed architecture reduces the area, delay and power. The CSLA is not area efficient because it uses multiple pairs of RCA to generate partial sum and carry by considering carry in 0 and carry in 1, then the final sum and carry are selected by the multiplexers (Mux).The basic idea of this work is to use BEC instead of RCA with carry in 1 in the regular CSLA to achieve lower area [2], [3] and [4]. The main benefit of BEC comes from the lesser number of logic gates than the n-bit Full Adder (FA). The details of BEC methodology of the basic adder blocks and presents the detailed structure and the function of the BEC.

The CSLA has been chosen for comparison with the proposed design as it has a lower area. The problem of carry propagation delay is overcome by independently generating multiple radix carries and using this carries to select between simultaneously generated sums. In this adder system, the addend and augends are divided into sub addend and sub augends sections that are added twice to produce two sub sums.

The selection of the correct, or true, sub sum from each of the adder sections depends upon whether or not there actually is a carry into that adder section. an adder is introduced to operates with low power and occupies lower area in comparison to conventional CSLA circuit due to using a first zero finder circuit. Besides by three basic changes in the critical path of adder, speed is improved considerably. First of all we used a high speed compact CSLA as partial adder in each block, then a block carry generator (BCG) circuit is used for faster carry propagation and finally we replaced multiplexer gate with a XNOR gate. For designing a fast CSLA, we used combination of conventional CMOS (C-CMOS) and Transmission Gate(TG) logic styles.

2. AREA EVALUATION METHODOLOGY OF THE BASIC ADDER BLOCKS:

An XOR gate is shown in Fig. 1, which is implemented by using AND, OR and Inverter (NOT). The gates between the dotted lines are performing the operations in parallel. The area evaluation methodology considers all gates to be made up of AND, OR and Inverter (AOI), each having area equal to 1 unit.

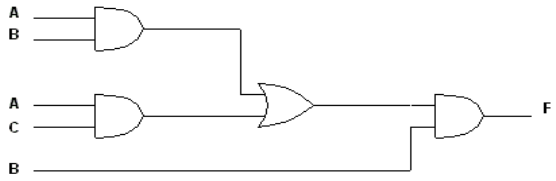

Fig1: Area evaluation of XOR gate

2.1 Binary to Excess -1 Converter (BEC):

To reduce the area and power consumption of regular CSLA, RCA with Cin=1 is replaced with BEC [5]. An n+1 bit BEC replaces the n bit RCA. The function table of a 3-b BEC is shown in Fig. 1 and Table 1 respectively [1]. By the use of BEC logic, we can reduce the significant amount of silicon area reduction in the VLSI design.

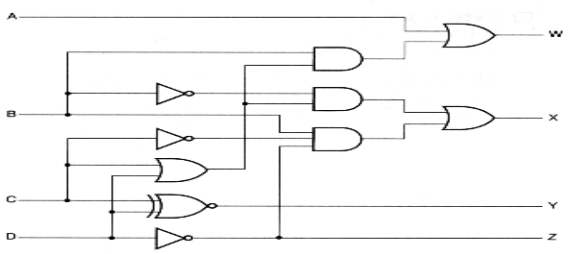

Fig2: 3 Bit Binary to Excess convertor

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3. EXISTING SYSTEM:

In RCA every full adder has to wait for the incoming carry before an outgoing carry is generated. One way to get around this linear dependency is to anticipate both possible values of the carry input i.e. 0 and 1 and evaluate the result in advance. Once the real value of the carry is known the result can be easily selected with the help of a simple multiplexer stage.

The carry out calculated from the last stage i.e. least significant bit stage is used to select the actual calculated values of the output carry and sum. The selection is done by using multiplexer. Internal structure of the group 2 of regular 16-bit CSLA is shown in fig.3 By manually counting the number of gates used for group 2 is 57 (full adder, half adder, and multiplexer). One input to the mux goes from the RCA with Cin=0 and other input from the RCA with Cin=1. The carry out calculated from the last stage i.e. least significant bit stage is used to select the actual calculated values of the output carry and sum. The selection is done by using a multiplexer.

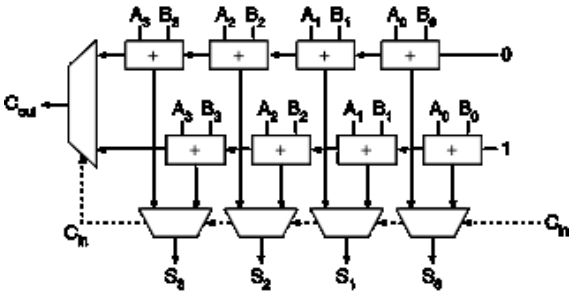

Fig3: Block diagram of carry select adder

A 16-bit CSLA is constructed by dividing into 4 stages i.e. N=16 total number of bits, M=4 number of bits per stage, (N/M = 4) and chaining such four equal length blocks .The existing system uses BEC instead of RCA with carry in 1 in the regular CSLA to achieve lower area. With an efficient design of an add-one circuit, the power and area of CSA can be reduced. But the XOR function in BEC consists of five gates according to the previous design.

4. PROPOSED SYSTEM:

This method replaces the BEC add one circuit by D-latch with enable signal. Latches are used to store one bit information. Their outputs are constantly affected by their inputs as long as the enable signal is asserted. In other words, when they are enabled, their content changes immediately according to their inputs. D-latch[5] and it's waveforms are shown in Fig.4 and Fig.5 respectively.

The Binary to excess one Converter (BEC) replaces the ripple carry adder with Cin=1, in order to reduce the area and power consumption of the regular CSLA. The modified16-bit CSLA using BEC is shown in Fig. 4 The structure is again divided into five groups with different bit size RCA and BEC. The group 2 of the modified 16-bit CSLA is shown Fig. 5. By manually counting the number of gates used for group 2 is 43 (full adder, half adder, multiplexer, BEC).

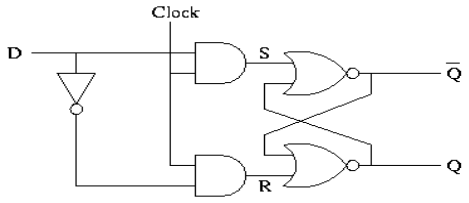

Fig 4: D- Latch

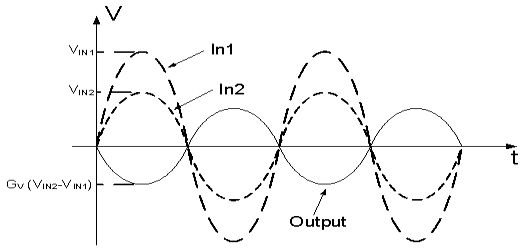

Fig 5: Input and Output Waveforms

The architecture of proposed 16-b CSLA is shown in Fig.6. It has different five groups of different bit size RCA and D-Latch. Instead of using two separate adders in the regular CSLA, in this method only one adder is used to reduce the area, power consumption and delay. Each of the two additions is performed in one clock cycle. When the clock is low a2 and b2 are added with carry is equal to zero. Because of low clock, the D-Latch is not enabled. When the clock is high, the addition is performed with carry is equal to one. All the D-Latches are enabled and store the sum and carry for

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carry is equal to one. According to the value of c1 whether it is 0 or 1, the multiplexer selected the actual sum and carry.

The third input to the full adder FA2 is the clock instead of the carry and the third input to the full adder FA3 is the carry output from FA2. The group 2 structure has three D-Latches in which two are used for store the sum2 and sum3 from FA2 and FA3 respectively and the last one is used to store carry. Multiplexer is used for selecting the actual sum and carry according to the carrry is coming from the previous stage. The 6:3 multiplexer is the combination of 2:1 multiplexer.

4.1 Modified Carry Select Adder

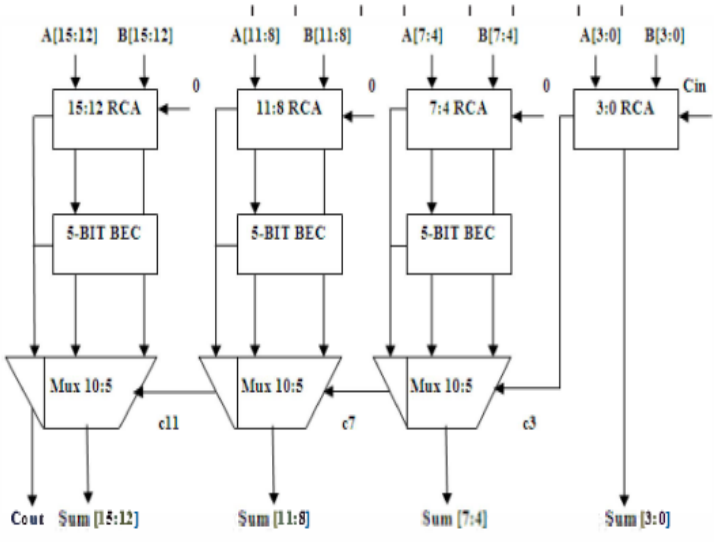

Fig 6: 16 bit Modified Carry Select Adder

A Modified Carry Select-Adder (MCSA) design is proposed, which make use of single RCA and Binary to Excess-1 Converter (BEC) instead of using dual RCAs to reduce area and power consumption with small speed penalty. The reason for area reduction is that, the number of logic gates used to design a BEC is less than the number of logic gates used for a RCA design. This is 16-bit adder in which least significant bit (LSB) [6]adder is ripple carry adder, which is 2 bit wide. The upper half of the adder most significant part is 14-bit wide which works according to the clock. Whenever clock goes high addition for carry input one is performed. When clock goes low then carry input is assumed as zero and sum is stored in adder itself.

5. IMPLEMENTATION RESULTS:

The 8-bit CSLA is done by the same structure of 16-bit CSLA except group 4 and group 5. The 8th bit inputs are directly given to the full adder to complete the 8-bit sum and carry. The 32-bit CSLA is done by cascading two 16-bit CSLA and 64-bit CSLA is done by cascading two 32-bit CSLA. Table exhibits the delay, area and power of regular, modified and proposed CSLA Simulation is carried out using Xilinx simulation tool and Spartan 2E as the target device. The major disadvantage of modified CSLA using BEC[8] is the increasing delay. This disadvantage is overcome in proposed architecture which reduces the delay, area and power than the regular and modified CSLA.

size	Types	Area of count of linear CSLA	Area Count of SQRT CSLA
16 bit	Regular	403	434
	Modified	319	337
32 bit	Regular	871	868
	Modified	675	674
64 bit	Regular	1742	1736
	Modified	1387	1348
128 bit	Regular	3679	3472
	Modified	2811	2696

Table 1: Comparison of CSLA based on Area Count

When compared to regular and modified CSLA the proposed circuit occupies less area. In addition to realization of higher speed and lesser area as discussed above, depicted that the proposed architecture consumes less power when compared to the regular and modified CSLA. The proposed CSLA overweighs both the regular and modified CSLA in terms of area, delay and power.

6. CONCLUSION:

A regular CSLA uses two copies of the carry evaluation blocks, one with block carry input is zero and other one with block carry input is one. Regular CSLA suffers from the disadvantage of occupying more chip area. The modified CSLA reduces the area and power when compared to regular CSLA with increase in delay by the use of Binary to Excess-1 converter. This paper proposes a scheme which reduces the delay, area and power than regular and modified CSLA by the use of D-latches. The Modified CSLA architecture is therefore, low area, simple and efficient for VLSI hardware implementation. Totally from the result analysis the Modified SQRT CSLA has reduced area.

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