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All Optical Implementation of Reversible Multiplexer Design using Mach-Zehnder Interferometer

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Abstract:

Since from couple of years reversible logic has risen as a promising registering model for applications in scattering less optical computing, low power CMOS, quantum processing, and so forth. There exists balanced mapping. i.e (one-to-one) in the middle of inputs and yields in reversible circuits which brings about no loss of information. Reversible processing has been proposed by a few experts as a conceivable different option for location the vitality dispersal issue. A few usage choices for reversible logic circuits have additionally been investigated as of late, as adiabatic logic, atomic attractive reverberation, optical registering, and so on. Focal points of reversible logic frameworks have drawn a huge enthusiasm of analysts to create promising registering standard. The reversible entryways can be effortlessly created at the chip level utilizing optical figuring. The all optical execution of reversible logic gates are in light of semiconductor optical amplifier (SOA) based Mach-Zehnder Interferometer (MZI). The Mach-Zehnder interferometer has focal points, for example, rapid, low power, simple manufacture and quick exchanging time. The all optical reversible gates outline is taking into account optical reversible entryways alluded as Feynman door, Fredkin Gate.Both entryways are proposed alongside systematic assessment of the configuration complexities both as far as postponement and asset necessities. The two gates are contrasted and customary methodologies by utilizing an accessible synthesis tool and after that mapping the reversible gates to MZI switch based usage.

Keywords: Reversible logic; Mach-Zehnder Interferometer (MZI); optical computing; semiconductor optical amplifier (SOA)

1. INTRODUCTION:

Reversible logic is turning into a promising standard among the developing figuring innovations because of is wide applications like optical registering, DNA processing, quantum figuring, quantum speck cell automata and so on. Reversible logic is likewise being examined for its promising applications in power of use nanocomputing. It is additionally considered as another low-power outline approach. Reversible circuits are those circuits that don't lose data amid reckoning and reversible calculation in a framework can be performed just when the framework contains reversible gates. An entryway is reversible if the door's inputs can be produced again from the yield and have a balanced mapping in the middle of inputs and yields, i.e. there is a particular yield task for each unmistakable data. Reversible logic entryways must have same number of inputs and yields. A reversible circuit comprises of a course of reversible entryways with no fan-out or criticism associations, and the quantity of inputs and yields must be equivalent. The steady information in the reversible circuit is known as the ancilla data, while the junk yield alludes to the yield which exists in the circuit. The inputs recovered at the yields are not considered as refuse yields.

Optical usage of reversible entryways can be a

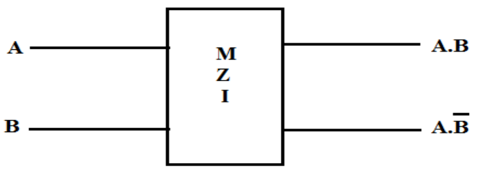


Fig.2. Functional behavior of MZI switch

promising different option for beat the force scattering issue in routine registering. Optical usage of reversible logic gates is picking up. The consideration of specialists as photon can give the unmatched fast and can have the data put away in a sign of zero mass. The all optical usage of reversible logic gates could be helpful to conquer the cutoff points forced by ordinary figuring, and is likewise considered as execution stage for quantum processing. As of late, specialists have likewise executed reversible logic entryways, for example, Feynman door, Toffoli gates, Peres door and Changed Fredkin entryway utilizing semiconductor optical amplifier (SOA)-based Mach-Zehnder Interferometer (MZI) optical switch because of its critical points of interest, for example, rapid, low power, quick exchanging time and simplicity in manufacture. The MZI interferometer comprises of bidirectional couplers and semiconductor optical enhancer in its arms. Interferometer goes about as a fast switch since it doesn't require any optical to electronic discussion and the other way around. Reversible frameworks empower the framework to process in both forward and in reverse course. In other word, for each yield we can create the data furthermore can backpedal to any point in the computational history. The all optical reversible snake configuration is taking into account two new optical reversible gates alluded as optical reversible entryway I (Organization I) and optical reversible entryway II (Organization II) and the current all optical Feynman entryway. The two new reversible entryways Organization I and Organization II can actualize a reversible snake with lessened optical expense which is the measure of number of MZIs switches and the proliferation delay, and with zero overhead as far as number of ancilla inputs and the waste yields.

2. FUNDAMENTALS OF ALL REVERSIBLE LOGIC:

In recent years, the Mach-Zehnder interferometer (MZI) based optical switch is widely used to implement reversible logic gates. A design of all optical MZI switch is shown in Fig. 1.

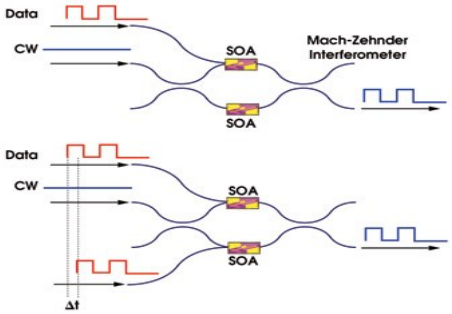


Fig 1: Semiconductor optical amplifier based Mach-Zehnder interferometer

By altering the phase change in one arm of a Mach-Zehnder interferometer, cross-phase modulation can switch the output from one spatial port to the other (top). For higher-speed switching, a delayed signal can be applied to the other arm so that a rapidly saturating gain switches the signal both onto and off the output port of the interferometer (bottom). The change in index is exploited to achieve optical switching by placing the device in an optical interferometer such as the Mach-Zehnder shown on the top of Figure 1. A block diagram of MZI based all optical switch is shown in Fig 2.

CONCEPT OF REVERSIBILTY AND NEED OF REVERSIBLE COUNTING

Reversibility in computing implies that no information about the computational states can ever be lost, so we can recover any past stage by computing backwards. This is called as logical reversibility. Reversible computing provides many advantages like reliability, low power design, high efficiency and fast processing. Reversible circuits conserve information and this improves the performance of the system. It also improves computational efficiency by minimizing power dissipation and increase portability of device, as it reduce the element size to atomic size. Although due to reversibility the hardware cost of the circuit increases as extra inputs and outputs are required to maintain reversibility but power cost and performance are dominant than hardware cost. Hence in this computing era we cannot ignore need of reversible computing.

3. PROPOSED ALL-OPTICAL MULTIPLEXER DESIGN:

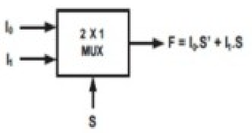
In this section, we present the all-optical implementation of a digital multiplexer using MZI switches, beam splitters and beam couplers. In the following subsections, we discuss the design of a (2×1) non-reversible all-optical multiplexer, followed by its generalization to (2n×1) multiplexer. Then a design extension to make the multiplexer design reversible is suggested, that requires one additional ancilla line.

A.DESIGN OF (2×1) MULTIPLEXER:

The schematic diagram of a (2×1) multiplexer is shown in Figure 4(a), where I0 and I1 are the two inputs, and S is the select line. The function implemented at the output is also shown. The all-optical implementation of the multiplexer is shown in Figure 4(b), which consists of a beam splitter (BS) for splitting the select input S, two MZI switches which generates the sub functions I0.S, I0.S, S.I1 and S.I 1 respectively, and finally a beam coupler (BC) that combines two of the MZI outputs to realize the desired functionality at the final output F. The BC essentially performs the logical OR functions in the digital domain. In the earlier reported works on implementing logic functions using MZI switches, BS and BC [8], [9], the cost of implementation (referred to as optical cost) has been estimated as the number of MZI switches required, as the relative costs of BS and BC are small. Similarly, the delay is measured as the length of the longest cascade of MZI switches. Denoting the units of cost and delay by MZI and Δ, for the implementation as shown in Figure 3(b),

$$
\begin{aligned}
M(1) &= 2\ MZI \\
D(1) &= 1\ \Delta
\end{aligned}
$$

WhereM(x) and D(x) respectively denote the optical cost and delay for a (2x × 1) multiplexer.



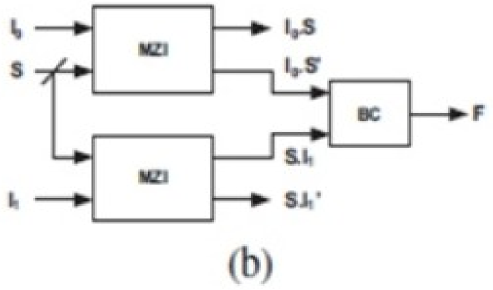


Fig. 3. a) 2-to-1 MUX (a) schematic diagram, (b) all-optical implementation

4. REVERSIBLE LOGIC GATES

The basic reversible gates are Feynman Gate and Fredkin Gate. This basic reversible gate can produce any Boolean functions.

(a) All Optical Feynman Gate

The Feynman gate (FG) is a 2 inputs and 2 outputs reversible gate. It has the mapping (A, B) to (P=A, Q=AXORB) where A, B are the inputs and P, Q are the outputs, respectively. The Feynman is also referred as the Controlled-Not gate (CNOT) as when the input A=1 then the output generated at Q will be complement of input B that is Q=B. A Feynman gate can be implemented using 2 MZI based all optical switch, 2 beam combiner (BC) and 2 beam splitter (BS) in all optical reversible computing. As the beam combiner (BC) simply combines the optical beams while the beam splitter simply splits the beams into two optical beams, hence researchers do not consider them in the optical cost and the delay calculations. Figure 3 shows the block diagram and the all optical implementation of the Feynman gate.

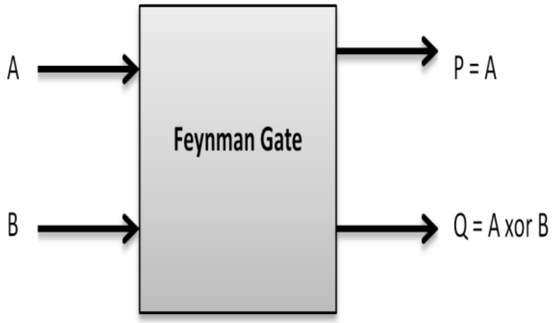


Fig.3. Feynman Gate

Truth table 1.Feynman Gate

Input		Output	
A	B	X	Y
0	0	0	0

(b)All optical Fredkin Gate

Fredkin gate is a 3*3 reversible logic gate having A, B, C as input vector and X, Y, Z as output vector, where X=A, Y=A’B⊕AC, Z=A’C⊕AB

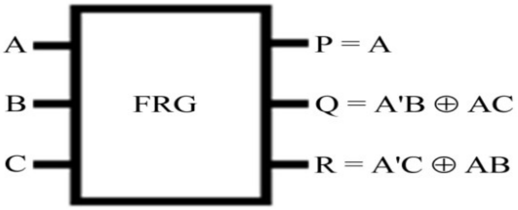


Fig.4. Fredkin Gate

Truth Table 2. Fredkin gate

Input			Output		
A	B	C	X	Y	Z
0	0	0	0	0	0
0	0	1	0	0	1
0	1	0	0	1	0
0	1	1	0	1	1
1	0	0	1	0	0
1	0	1	1	1	0
1	1	0	1	0	1
1	1	1	1	1	1

(c)All optical Peres Gate

The Peres gate is a 3x3 reversible logic gate with the inputs to outputs mapping as (A,B,C) to (P = A, Q = A XOR B, R = A.B XOR C), where A, B, C are the inputs and P, Q, R are the outputs respectively [18]. An all optical Peres gate can be implemented using 4 MZI based switches, 5 beam splitters (BS) and 3 beam combiners (BC). The optical cost of Peres gate is considered as 4 as the all optical implementation of Peres gate requires 4 MZI based switches. The delay of Peres gate is 2Δ as two MZI switches works in parallel with the two other MZI switches.

5. DELAY AND OPTICAL COST ANALYSIS

The delay and optical cost analysis of the proposed adder are performed by analyzing the steps involved in the design of all optical reversible ripple carry adder with input carry. The methodology requires n optical reversible gate that works in series. Thus this step will have the optical cost of 3n and delay of 2nΔ. A CNOT gate that is used to generate the carry out and it contributes the optical cost of 1 and delay of 1Δ. Thus, the Step 1 has the total optical cost of 3n+1 and delay of 2n + 1Δ.

Optical Cost and Delay of All Optical Implementation of Reversible Gates

	Optical cost	Delay
Feynman Gate	2	1Δ
Fredkin Gate	2	1Δ
Peres Gate	4	2Δ

6. CONCLUSION

Reversible logic gates are important for the future optical computing as they have the potential of reducing power consumption dramatically. It has large number of benefits in those areas which require high energy efficiency, speed and performance. The basic reversible logic gates like Fredkin gate, Feynman gate and Peres gate can produce any Boolean function. These gates will provide the efficient results. Although the cost of the circuit increases due to reversibility as extra inputs and outputs are added in the circuit to maintain reversibility, but the power cost and performance dominant than hardware cost. All the optical reversible gates are functionally verified at the logic level. This is done by creating a Verilog library of

Mach-Zehnder interferometer, beam combiner and beam splitter. The state of the art of reversible optical circuits by providing NOR logic based reversible gates.

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