International Journal of Research (IJR)
e-ISSN: 2348-6848, p- ISSN: 2348-795X Volume 2, Issue 09, September 2015
Available at http://internationaljournalofresearch.org

A Review on Various Error Detection and Correction Using HVD Implementation

[1]Shaik Sumera Bhanu; [2]G. Sreenivasulu & [3]Syed Kareemsaheb,
[1]Associate Professor, Department of Eectronics& communication Engineering, Audisankara Institute of Technology(ASIT), Gudur,A.P. India.
[2] M.E ,Associate Professor, Department of Eectronics& communication Engineering, Audisankara Institute of Technology(ASIT), Gudur,A.P. India.
[3]M.tech., (Ph.D),Department of Electronics& communication Engineering, Nagarjuna University, Guntur, A.P.

Abstract

Several EDAC techniques have been proposed and employed to effectively detect and correct errors introduced during data transmission over a communication channel or at the destination domain during storage. Some of these techniques can detect: only single error, all unidirectional errors, only burst errors, any bit in a data packet is change from one to zero or zero to one it means error is occur in same, errors with known locations assume a code is correct if the error location are known or cannot detect errors which appear in the same location in a pair of message codes. Coding techniques that detects and correct errors are more precise at detecting error locations and correcting them, however if more than one error occur, it becomes a challenge to detect all errors in a data frames and converted back its original form . In this paper, an advanced error detection and correction method to protect against errors is proposed. This method is based on 4D parities checking. This method, which is named HVD, provides very high detection coverage rate that can correct up to three flips in a data bit. The performance of HVD is optimizing in comparison with the following coding techniques: CRC, Hamming codes. An independent design platform is utilized for the simulation by Xilinx 8.1 using Model Sim SE-EE 5.4a which shows a significant reduction in uncorrected errors during data transmission. The efficient performance of HVD makes it a more applicable coding technique for communication, data transmission, different protocols and other application.

Keywords: Burst error; CRC (Cyclic Redundancy Check); EDAC (Error Detection and Correction); Hamming Code; HVD (Horizontal Vertical Diagonal); Message bits; Xilinx; Model Sim

I. INTRODUCTION EDAC methods are used to find that the data is error free or is not corrupted, either by noisy channel, by hardware failure or during read-write operation in the memory segment. Various error detection methods exist in the communication system. One method currently utilized to produce reliable memory is the use of Error Correction Codes (ECC) to encode data before it is stored in the memory. Error correction codes take a set of information bits at the producer of the information and create a set of redundant bits based on the information bits. These redundant bits are sent or stored with the original set of information bits. The consumer of the information then uses the redundant bits to determine if any errors have occurred in transmission or storage. In the case of memory, the redundant bits are calculated and stored along with the original bits and then when they are read from the memory they are examined to determine if any errors have occurred between

the time the information was stored and the time it was retrieved. The most common error detecting and correcting scheme being employed are parity bit, CRC, HVD and Hamming codes. All these methods are implemented on the second layer of OSI model at Data link layer. The upper layers work on some generalized view of network architecture and are not aware of actual hardware data processing. Therefore, the upper layers require error-free transmission between two systems. Almost every application did not work if it receiver data with errors. Applications like voice and video may not get that much affected and may still function well with some error.Data-link layer uses some error control mechanism to ensure that data bit streams are transmitted with certain level of accuracy. But to recognize how errors can be controlled, it is important to know what types of errors may occur. A. Hardware Redundancy Vs Software EDAC In order to protect semiconductor memories, software EDAC or redundancy can be used. Redundancy can either be hardware redundancy that is provided by extra components or time redundancy that is provided by extra execution time or by different moment of storage or can be a combination of both the hardware and time redundancies. To allow redundancy to detect permanent faults, the repeated computations are performed differently. TMR (Triple Modular Redundancy) is a suitable technique for SRAM-based FPGAs because of its full hardware redundancy property in the combinational and sequential logic. One solution for the protection of memories is use of hardware redundancy techniques, but they are too costly. When hardware redundancy is not possible, we have to go for software solutions. By using software Error Detection and Correction, transient faults in the combinational logic will never be stored in the storage cells, and bit flips in the storage cells will never occur or will be immediately corrected. For applications where read and write operations are done in blocks of words, such as secondary storage systems made of solid-state memories (RAM discs), software-implemented EDAC could be a better choice than hardware EDAC, because it can be used with a simple memory system and it provides the flexibility of implementing more complex coding schemes. With software EDAC, the data that is read from main memory may be erroneous, if the error occurs after the last scrub operation and before the time of reading. In other words, single-bit errors may cause failures. In contrast, hardware EDAC checks all the data that is read from memory, and corrects single-bit errors. Therefore, hardware EDAC provides improved reliability and when feasible should be the first choice for protecting the main memory. When hardware EDAC is not available or affordable, software EDAC can be used as a low cost solution for enhancing the reliability of systems. For cases where data is read and written in blocks of words rather than individual words, software EDAC may be a better choice than hardware EDAC.

LITERATURE SURVEY Various error detection and correction methods are being used to maintain good level of reliability, to protect memory cells using protection codes. The method used in [3], is based on the hardware and time redundancy, although this technique reduces the number of input and output pins of the combinational logic; it requires additional encoding/decoding circuitry. The reliability issue can be solved, but the hardware redundancy schemes like duplication or triple modular redundancies are expensive. In [5], the encoder and the decoder can use any error detection and correction

code. But the data is only coded in write operations, and decoded in read operations. So, the gathering of upsets is likely to occur and it depends on the reading and writing application request frequency. In order to avoid this accumulation of upsets, it is necessary to use an extra logic which is able to constantly detect and correct upsets in all coded data. The EDAC method given in [11] is again based on TMR, so increases the density as it is a hardware redundancy method. The method given in [4], perform memory error correction code which reduces power consumption in single-error correcting and double error-detecting checker circuits. This method can be employed to solve the non linear power optimization problem but it involves tedious computation of H- matrix. The method in [6], is called HVD, provides eminent detection coverage rate that can correct up to three upsets in a data array. It make use of parity codes in four directions in a data part to satisfy the reliability of memories and it can detect and correct the errors in the actual data bits. If the parity bits are itself erroneous, then those errors are detected by generating the parity bits for parities that is syndrome bits, but this is a complicated process. An easy way to find the errors in parity bits is presented in this paper. For this, we can take data bits and parity bits as a whole word. These words can be viewed as an m x n array. The hamming code will be used for the error detection and correction for this whole codeword containing both the data bits and the parity bits throughout the length of an array. After detecting the error, it can discover whether it is a data bit or a parity bit. The method used in [9], it shows that All of multiple error bit flips can be detected and 3-bit errors can be corrected, based on the experimental results. But it can correct only three bit error in a 8×8 matrix. The method used in[8], it shows that it can detect and correct up to 4 bits. With this method a large combination of multiple faults can be corrected which depend upon the length of the coded word array.

VARIOUS METHODS FOR EDAC

A. Type of Error Control The information of data is transfer from one hop to another hop. In TCP/IP model, the physical layer and the final layer of TCP/IP model transforms the data into stream of bits and transfers them into a signal toward the receiver device. Meanwhile those bits flow from one hop to another, they are exposing to channels interference, for example electrical interference or thermal noise that subject to unpredictable change. These channel interferences can change the shape of the transmitted signal leading into errors in the signal. There are two kinds of error single-bit error and burst error.

B. Parity Check The most common method for detecting bits error with asynchronous character and character- oriented synchronous transmission is parity bit method. There are two types of parity check schemes: even and odd parity checks. With the even parity check, the redundant bit is chosen so that an even number of bits are set to one in the transmitted bit string of N+r bits, where r is the bit that used to be the even parity check and N is the bit that is transmitted by the transmitter of the network. The receiver re-computes the parity of each received bits from the transmitter and discard the strings with the invalid parity. The parity scheme is always used if 7-bits character is exchanged. If there are 7-bits that are transmitted by the transmitter and parity check are used to detect the error and often the eighth bit is the parity bit.

C. Cyclic Redundancy Check (CRC) The second method in error detection in data link layer is cyclic redundancy check. As the parity check which is based on the submission of the

binary the cyclic redundancy check is based on the binary division. In CRC, rather than adding bits to attain a desired parity, a series of redundant bits, called the CRC remainder, is attached to the end of a data unit so that the resulting data unit becomes exactly divisible by a second. On the receiver side, the incoming binary data bits are divided by the same number to be compared on the transmitter side. Implies that, if the remainder of the division is identical to the value that added to CRC when the data was transmitted, the data will be accepted, otherwise the unmatched reminder produced on the destination after the CRC is indicates the data unit has been damage during the transmission of data. The redundancy bits used by CRC are derived by dividing the data unit by a predetermined divisor; the remainder is the CRC. To be valid, a CRC must satisfy two conditions: It must have exactly one less bit than the divisor and appending it to the end of the data string must make the resulting bit sequence exactly divisible by the divisor.

Conclusions In this paper a simple method with smaller calculation is presented. It is a painless method of detecting the errors by amputation of error bits, so it can be remove complexity of the circuit. With the help of method can detect and correct the errors in data bits as well as in the parity bits without any extra calculations. This paper presents an advanced EDAC method which is entitles as HVD code. This kind of detection and correction code uses the parity code in 4D in a message. Any change of bit in a data packet can be detected and two or three bit errors can be corrected, depend on the experimental results

References

[1.] Anlei Wang, Member, IEEE, and NaimaKaabouch, Member, IEEE. "FPGA Based Design of a Novel Enhanced Error Detection and Correction Technique, 25- 29 (2008)

[2.] Behrouz A. Forouzan Data Communication and networking, 2nd edit. Tata McGraw Hill (2011)

[3.] Clarke K.P., Reed-Solomon error correction, Research and development British Broadcasting Corporation, WHP 031 BBC (2002)

[4.] McAuley A.J., Weighted sum codes for error detection and their comparison with existing codes, IEEE/ACM Trans. on Networking, 2(1), 16–22 (1994)

[5.] Feldmeier D.C., Fast Software Implementation of Error Detection Codes, IEEE/ACM Trans. Networking, 3(6), 640-651 (1995)

[6.] Berrou, C., Glavieux A. and Thitimajshima P., Near Shannon limit error-correcting coding and decoding: Turbo-codes International Conference on Communications, 1064-1069 (1993)

[7.] Baicheva T., Dodunekov S. and Kazakov P., On the cyclic redundancy-check codes with 8-bit redundancy, Computer Communications, 21, 1030–1033 (1998)

[8.] Kazakov P., Fast calculation of the number of minimumweight words of CRC codes, IEEE Transactions on Information Theory, 47(3), 1190–1195 (2001)

[9.] Koopman P., 32-bit cyclic redundancy codes for internet applications, in International Conference on Dependable Systems and Networks, June 23–26, 459–468 (2002)

[10.] MostafaKishani, Hamid R. Zarandi, HosseinPedram, AlirezaTajary, Mohsen Raji and BehnamGhavami, HVD: horizontal-vertical-diagonal error detecting and correcting code to protect against with soft errors, (2011)

AUTHOR PROFILE

1. Shaik sumera bhanu, she got her Bacheor degree from Narayana Engineering college(NEC), Nellore, In Department Of Electronics and computer Engineering, JNTU Anantapur. Currently she pursuing M.Tech post graduate of VLSI From Audisankara Institute Of Technology(ASIT), Gudur, In Department of Electronics and Communication Engineering, JNTU Anantapur.

2. **G. SREENIVASULU, M.E.**

He is working as Associate Professor, Department of Eectronics& communication Engineering, Audisankara Institute of Technology(ASIT), Gudur,A.P. India.

3. Syed kareesaheb M.Tech .,(Ph.D), Research scholor,

Department of Electronics& communication Engineering, Nagarjuna University, Guntur, A.P. He is working as Associate. Prof. In Department of Electronics& communication Engineering. Audisankara Institute of Technology (ASIT),Gudur.