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Fast clearing and protection of Power Systems with Fault Current Limiters and PLL-Aided Fault Detection

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Abstract—

In this paper, a new method is proposed that can beused to discriminate faults from switching transients. The methodis primarily intended for use in systems where fast fault detectionand fast fault clearing before the first peak of the fault current arerequired. An industrial system, in which high short-circuit power is desired but in which high short-circuit currents cannot be toleratedis an example of such a system. A phase-locked loop (PLL) is used to perform the discrimination. Computer simulations havebeen performed and it has been demonstrated that the output ofthe PLL is completely different for a fault compared to a switching transient. This difference can be used for discrimination betweena fault and a switching transient.

***Index Terms*—**Fault protection; phase-locked loop (PLL); power system; transients

I. INTRODUCTION

HIGH SHORT-CIRCUIT power is often desired in anindustrial system in order to connect and disconnectloads without causing disturbances to sensitive equipment orprocesses.With the high short-circuit power; a high fault currentdevelops in case there are faults in the system. This high faultcurrent has to be considered when designing the switchgear andother components that build up the power system. This is easilydone in new installations but can be problematic when there is a need for higher short-circuit power in an existing system.In these cases, the installation of a fault current limiter could be an alternative to rebuilding the switchgear. The installationof a fault current limiter can also provide the opportunity tomake connections in the power system that otherwise wouldnot be possible due to fault currents that exceed the rating ofthe switchgear. One of these examples is the paralleling of twotransformers. If a fault current limiter is installed as a sectionalizer between the two transformers, the system will experiencethe benefit of higher short-circuit power and in case of a faultin the system, the fault current limiter is operated and thesystem is sectionalized, thus reducing the fault current to levelswhich the system can handle. In [1], a trend toward increasedshort-circuit power is reported, which is also illustrated by anexperience of more than 2800 installations of fault-currentlimiters throughout the world.And proposal for future work. Furthermore, a short appendixdescribing some methods of estimating power systemsignals is added for convenience.

II. FAULT-CURRENT LIMITERS AND FAULT-CURRENT DIVERTERS

An apparent contradiction regarding the short-circuit powerof a supply network is that whereas there are obvious advantageswith a stronger network (less voltage dips, more and larger loadscan be connected, less switching transients), there are also obviousdisadvantages (high-fault currents in case of short-circuitfaults in the system).

Fault-Current Limiters

One way of solving this contradiction is to use a fault-currentlimiter. A fault-current limiter is a device that during normaloperating conditions allows a strong network but when a faultoccurs, introduces enough impedance in the circuit so that thefault current is limited.

The purpose of a fault-current limiter is to limit the fault currentso that its prospective peak value never is reached. The currentlimiting functionality can be achieved in several ways (e.g.,current limiting reactors [2]; fuses [3]; triggered fuse [1]; superconductivefault–current limiters [4], [5]; and fuses [6] and power electronic-based current limiters [7]–[10].

Fault-Current Diverters

Fault-current diverters can be used as an alternative to faultcurrentlimiters. A current diverter consists of a switch that is inopen position under normal operating conditions. When a faultis detected, the switch closes and short circuits the phases of thepower system to earth at a predetermined location. This predeterminedlocation is preferably chosen as close to the source aspossible. The faults current will still flowfrom the source throughthe current diverter to earth and will continue to do so until themain circuit breaker (CB) clears the fault current. The benefit ofa fault-current diverter is that the load that is connected to thesystem does not see the full short-circuit current once the switchhas been closed. Thus, for the load, the fault-current diverterprovides a limitation of the fault current. A current diverter isan easy solution to provide fault-current limiting functionalityin a power network. The network downstream the current diverterexperiences only a small residual current once the fault current has been commutated to the earth path.

One example of a current diverter is given in [5]. It is a devicethat in case of a short circuit involving an open arc operatesquickly and achieves a short circuit between phases and earth,thus short-circuiting the arc. The voltage drop across the arc becomespractically zero, making the arc extinguish. Another exampleis given in [6], which is a similar device that uses thesame principle.

One common feature of the described fault–current limitersand current diverters is that they must be able to operate withina few milliseconds after fault inception. The fault current mustbe limited before the first peak of the fault current. Taking intoaccount that some of the fault-current limiters described before contain mechanical systems that require a certain time tooperate, it can be concluded that fault detection is an essentialprerequisite for a system containing a fault-current limiter. Some types of fault-current limiters do not depend on externalfault detection—a superconductive fault-current limiter operatesas soon as the superconducting properties of the device arechanged due to the fault current and the fuse operates as soonas the current has increased above the fuse’s designed operatingcurrent. For the other fault-current limiters, the fault detectionhas to be performed by external means.

III. POWER SYSTEM PROTECTION

As concluded in the previous section, power system protectionis another important issue. It is essential for safe operationof the power system that faults are detected and cleared automaticallyin a fast and reliable manner so that the operation of thepower system is not disturbed. A typical fault protection systemis built from circuit breakers (CBs), protection relays, and primarytransducers, such as voltage and current transformers andauxiliary equipment.There are many methods and algorithms available to detectshort-circuit current in a power system. One simple (but yet efficient)method is to estimate the current from measured currentsamples. If the magnitude of the estimated current is larger thana predetermined threshold it is assumed that a fault has occurred(magnitude relay). The accuracyof the

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estimation and the amount of information that is availablefor the estimation are correlated. In general, if more informationis available, the estimation will become more accurate. On theother hand, if faster fault detection is required, the estimation becomesless accurate since less information is available. In an earlierpaper, fast fault detection has been defined to be in the rangeof 1–2 ms after fault inception [9]. This short detection time isneeded for the fault-current limiters as mentioned in the previoussection. Some methods that have been suggested for usein transmission systems have the potential of being fast. Thesemethods could be based on traveling waves, neural networks, wavelet transforms, and fault-generated noise.

Although it is sometimes possible to adapt the mentionedtechniques for fast fault detection in power distribution systems,new techniques have been explored. In the latter reference,a method for fast fault detection is described, which detects thata fault has occurred when five consecutive current samples areabove a predefined threshold (i.e., the measured current samplesare not fitted to a signal model). With proper signal processing(filtering), it was further demonstrated that it was possible todiscriminate between a fault and common switching transients.In this paper, an alternative method to perform the discriminationis proposed.

Even though the detection of faults is the primary concernfor fault protection devices (dependability), the ability to distinguishbetween a fault and a switching transient (security) isalso important. Switching transients can, under certain circumstances,give rise to high currents, which are much larger inmagnitude than normal load currents. In existing relay protection,capacitor energization and transformer energization Thus, the error is zero exactly when the output angle of the PLL is in phase with the current of phase a. When a transient occurs in the system, the error signal will deviate from zero.

Depending on the characteristics of the transient, the deviationwill have different magnitude and frequency. Since a fault is typically an ac fundamental power frequency character, the deviation will be different than for a switching transient that contains no fundamental power frequency components. The behavior of the error signal of the PLL will also depend on the tuning of the PLL.

A current transient caused bya transformer energization typically contains a superimposeddc component and a superimposed second harmonic component.Acurrent transient caused by a capacitor energization typicallycontains higher frequency harmonic components. The harmoniccomponents in the measured current can be identifiedwith Fourier-based methods, but that typically requires moretime. For fast fault detection purposes, other methods have tobe investigated. The method that is proposed in this paper usesa PLL for that purpose.

IV. PROPOSED METHOD

In this section, the proposed method of using a PLL for discriminationbetween faults and switching transients will be described.First, a short description of the basics of a PLL is given.Second, a well-known implementation of a PLL suitable forsimulation purposes is described and the relevant signals thatare used for the actual discrimination between a fault and aswitching transient are identified. Third, the tuning of the parametersof the PLL implementation is discussed and suggestions for a first selection of parameters are given.

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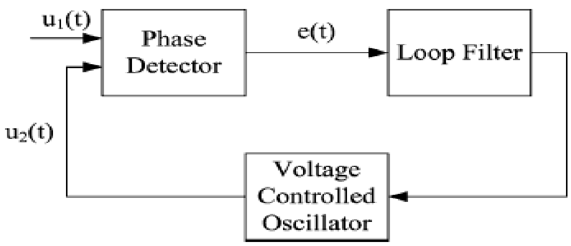

Fig 1: Block diagram of a PLL.

Basics of a PLL

The firstPLLs were analog devices but following the development insolid-state electronics and computer technology, the PLL hasdeveloped from an analog device via digital implementations topure software implementations.

A PLL is a circuit that is used to synchronize an input signalwith a reference signal (an output signal that is generated by thePLL) with respect to phase and frequency. The function of thePLL can be explained from the block diagram of a simple PLL,as shown in Fig.1.

The input signal is compared with the reference signalin the phase detector (PD). The output of the phase detectoris zero as long as the input signal and the output signal areequal in phase and frequency. If the phase or frequency of the input signals changes, the output of the phase detector will deviatefrom zero. The error signal is passed through a low-pass filter (LF) and then to a voltage-controlled oscillator (VCO),which generates a reference signal (the output signal). If theerror signal deviates from zero, the VCO will adjust the frequencyof the reference signal so that the phase error becomeszero and the two signals are in phase. When the input signal isin phase with the reference signal, the PLL is in its locked state;hence the name phase locked.Recent research related to PLLs has been from several researchfields: general descriptions of PLLs, distributed generationapplications, active power-line conditioner applications, servo controllers, as well as protection and control.

Description of a PLL that is Suitable for the Discriminationbetween a Fault and a Switching Transient

A vector implementation, as shown in Fig. 2, of a PLL is describedin this paragraph. Compared to the block diagram ofFig.1, the error signal corresponds to theoutput of thePD, whereas the proportional-integral (PI) regulator and the integratorcorresponds to the loop filter and the voltage-controlledoscillator (VCO). The inputs to the PLL are the three phase-currents, which are first transformed to quantitiesusing Clarke's transformation. Then, the quantitiesare projected onto a reference frame. Depending on theproximity of the quantities to the reference frame, an errorsignal is formed. This error signal is fed through a PI regulatorso that the error is controlled to zero. Once the error is zero, theinput signals are in phase with the reference frame.If it is assumed that the system is in steady state and that thepower system is completely balanced, the phase currents can bewritten as

$$I_a = I \sin wt$$

$$I_b = I \sin (wt-120)$$

$$I_c = I \sin (wt+120)$$

Then, the Clarke's components $I\alpha$ and $I\beta$ equate to

$$I\alpha = I \sin wt$$

$$I\beta = - I \cos wt$$

Now, with reference to Fig. 2, the error signal is given by

$$e(t) = I \sin (wt-\theta)$$

C. Tuning of the PLL

The PLL will be tuned to the power system frequency. PLLshave been used for many years in HVDC transmission in orderto synchronize the firing of the thyristors to the phase angle ofthe connected ac system. It is thus a well-

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known procedure andit is advisable to use parameters from such an installation as astarting point for the tuning.

Fault Detection and Discrimination Using a PLL

The method that is used to detect a fault and discriminatethe fault from a switching transient is described here. Two algorithmsare executed in parallel. The first algorithm is basedon the estimation of the magnitude of the current. If the estimatedmagnitude is higher than a preselected threshold, a flagis set. The second algorithm is as previously mentioned, monitoringthe error signal of a PLL. If this error signal exceeds apreselected threshold, a second flag is set. If both flags are set,it is determined that a fault has occurred.

V. SIMULATION AND RESULT

In order to test the proposed method, a simple test system hasbeen developed and implemented in MATLAB/simulink.

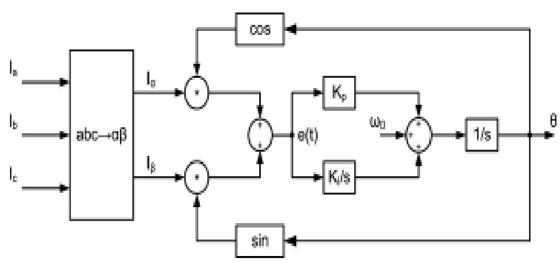

Fig 2: PLL implementation.

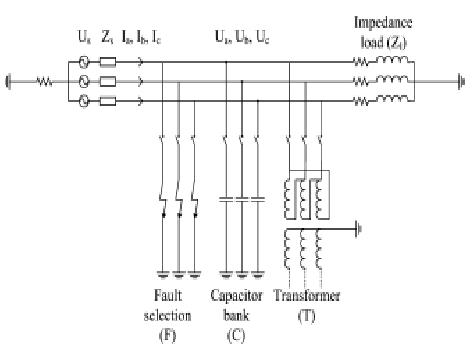

Fig 3: MATLAB test system

The test system, as shown in Fig. 3, consists of an infinitesource, an impedance load, a shunt capacitor (with an associatedcircuit breaker), a transformer (with an associated CB), anda fault selection arrangement. The data of the system are summarizedas follows.

• The infinite source is modeled with a voltage source that isconnected in series with impedance. The supply voltageof the source has been chosen as 12 kV. The seriesimpedance has been chosen so that the power systemwill have a short-circuit power of approximately MVA m 0.55 mH). The supply frequency of the voltage source is selected to 50 Hz. Ashort-circuit power of 831MVA will give a short-circuitcurrent of approximately 40 kA.

• The impedance load is modeled by impedanceconsistingof a resistor and an inductance. Their values arechosen so that the load current is approximately 630 A.

• The shunt capacitor is modeled by a capacitance ofF. The shunt capacitor gives a reactive powersupply of 4.08 MVAr at nominal voltage. The shunt capacitor is connected to the power system by a CB which,at the start of the simulation, is open. The capacitor isuncharged at the start of the simulation.

• The transformer is modeled by a transformer modelavailable in the master library of PSCAD/EMTDC. Withthis transformer model, it is possible to model inrushphenomena and magnetizing properties. The transformeris connected to the power system with a CB which, atthe start of the simulation, is open. The transformer isconnected in delta on the primary side and in Y on thesecondary side. The winding voltages of the transformerare 12 kV at the primary side and 240 V at the secondaryside. The leakage reactance is 0.122 p.u. on a transformerrating of 10.2 MVA. The residual flux in the transformeris also modeled.

• The fault selection arrangement is implemented by usinga component from the PSCAD master library. With thiscomponent, it is possible to simulate different fault resistances,whose phases participate in the fault and differentfault

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inception angles. At the start of the simulation, nofault is applied.

Simulated Events

A large selection of shunt faults, capacitor energizations, andtransformer energizations have been simulated. The faults weresimulated as three-phase faults and phase-to-phase faults withlow impedance. This selection was made because these types offaults are dimensioning for fault-current-limiting applications.Many distribution systems are earthed through impedance,which limits the magnitude of fault currents due to single-phaseearth faults. The capacitor and transformer energizations havebeen simulated by closing the associated CB. All events havebeen simulated to occur at various times with respect to thephase angle of the supply voltage (the phase angle of phase hasbeen selected as a reference). The instant when the event occurswill determine some of the characteristics of the transient currentsuch as, for example, the magnitude and possible dc offset.

Results

A large number of results are available as a result fromthe simulations. A few selected results are presented here.

The figures of this subsection contain plots of power systemsignals—mainly voltages and currents—but also signals of thecontrol system, such as the error signal from the PLL, whichhas been taken as a measure on how much the measured currentdeviates from the prefault load current.

1) ***Faults****:* This section contains plots of signals caused byshunt faults in the power system. Both three-phase and phase-tophasefaults have been analyzed. Typical phase voltages and currentsdue to a three-phase fault are plotted in Fig. 4. The errorsignal of the PLL for this fault is plotted in Fig. 5. As can beseen from that figure, the error signal deviates largely from zero(steady state) shortly after the fault. However, after the fault iscleared, the error signal returns to zero once the PLL has adjustedto the new conditions. Faults have been applied with differentfault inception angles. The magnitude of the error signalof the PLL was well above 10 p.u. for all fault inception angles.Typical phase voltages and phase currents due to a phase-tophasefault are plotted in Fig. 6. The error signal of the PLL forthis fault is plotted in Fig. 7. As can be seen from that figure,the error signal again deviates from zero shortly after the fault.Once the fault is cleared, the error signal returns to zero aftera short transient period. Faults have been applied with differentfault inception angles. The magnitude of the error signal of thePLL was well above 10 p.u. for all fault inception angles.

2) ***Transformer Energization****:* In this section, plots of signals(voltages, currents, and relevant parameters from the controlsystem) caused by transformer energization in the powersystem are presented. Typical phase voltages and phase currentsdue to a transformer energization are plotted in Fig. 8. The errorsignal of the PLL for this event is plotted in Fig. 9. As can beseen from that figure, the error signal deviates from zero shortlyafter the event has occurred but returns to steady state when thePLL has adapted to the new conditions. Different switching instantswere investigated and the magnitude of the error signalwas never above 2 p.u.

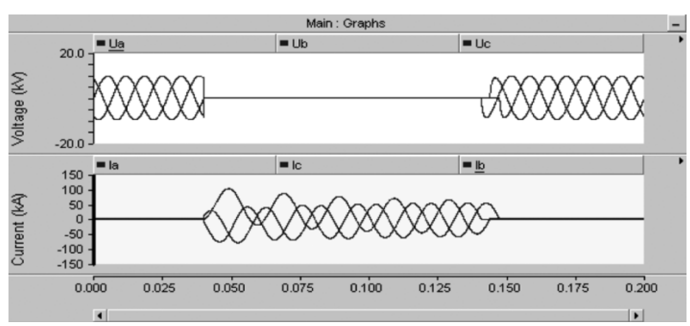

Fig 4: Phase voltages and currents due to a three-phase fault.

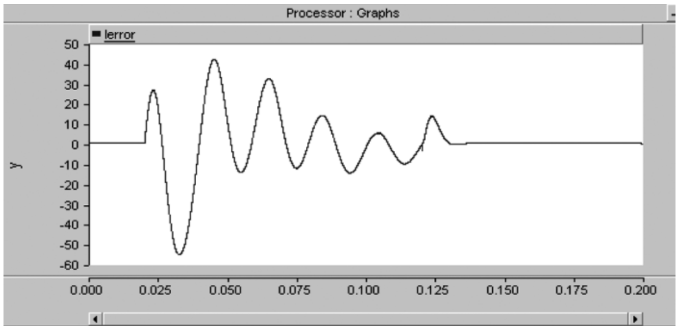

Fig 5: Error signal due to a three-phase fault (in per unit).

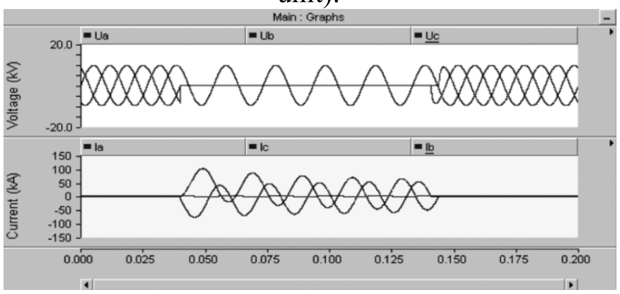

Fig 6: Phase voltages and currents due to a phase-to-phase fault.

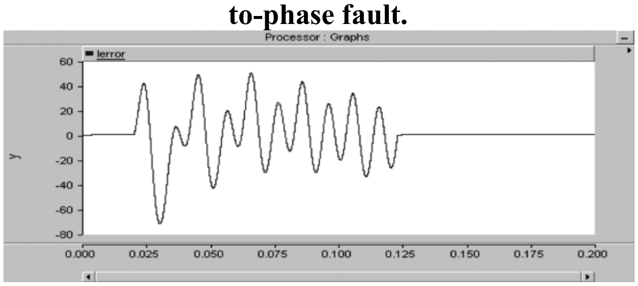

Fig 7: Error signal due to a phase-to-phase fault (in per unit).

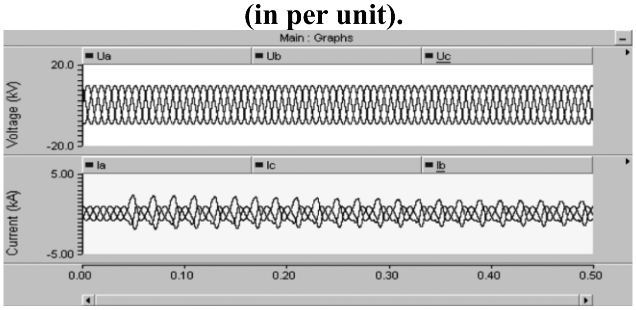

Fig 8: Phase voltages and currents due to transformer energization.

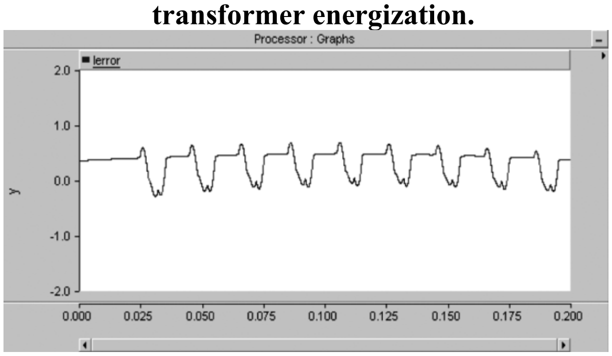

Fig 9: Error signal due to transformer energization (in per unit).

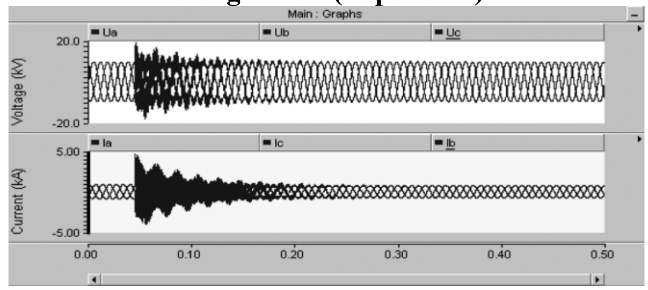

Fig 10: Phase voltages and currents due to capacitor energization.

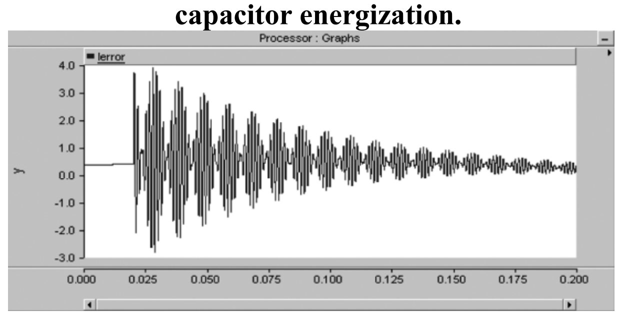

Fig 11: Error signal due to capacitor energization (in per unit.).

3) Capacitor Energization: In this section, plots of signals(voltages, currents, and relevant parameters from the controlsystem) caused by capacitor energization in the power systemare presented. Typical phase voltages and phase currents due tocapacitor energization are plotted in Fig. 10. The error signal ofthe PLL for this event is plotted in Fig. 11. As can be seen fromthat figure, the error signal deviates from zero shortly after theevent has occurred but returns to steady state when the PLL hasadapted to the new conditions. Different switching instants wereinvestigated and the magnitude of the error signal was neverabove 5 p.u.

C. Analysis of the Proposed Method

First, a threshold for the measured current magnitude is selected.In this example, the threshold is selected to three timesthe nominal current, (i.e., 2 kA). Second, a threshold for theerror signal of the PLL is selected. In this example, the thresholdis selected to 10 p.u. The first threshold is reached for all ofthe four transients studied in this section. However, the second threshold is only reached for the two transients that correspondto faults (i.e., the three-phase fault and the phase-to-phase fault).

Thus, it can be concluded that the algorithm is able to discriminatebetween a fault and a switching transient. With a samplingrate of 64 samples/cycle (50 Hz), the first threshold is reached atthe first sample following fault inception (i.e., after 0.3 ms). Thesecond threshold is reached after approximately 2 ms. Thus, thefault detection time is approximately 2 ms.Compared to a magnitude-based protection algorithm, allfour transients would have been considered as faults sincethe first threshold was reached. In order to use a pure magnitude-based protection algorithm, the first threshold would haveto be increased to, for example, 10 kA to provide a good marginbetween a fault and a switching transient. If the magnitude ofthe switching transients is higher, the threshold will have to be increased even more.

VI. CONCLUSION AND FUTURE WORK

In this paper, it has been demonstrated that a PLL can be usedto determine whether a current transient is due to a fault in thesystem or due to a switching transient. Transformer and capacitorswitching have been specifically studied due to the large occurrenceof these switching transients in the power system. Simulationshave been performed using a test system where faultsand switching transients have been simulated. For all of theseevents, a large difference was observed in the error signal ofthe PLL when a fault or a switching transient was applied. Thisdifference can be used to discriminate faults from switchingtransients.

The work presented in this paper is based on simulations andtheoretical investigations. The focus has been on discriminationbetween switching transients and low impedance faults. For futurework, high impedance faults must also be considered. Furthermore,the method could be tested in a real-time digital simulatorwith actual recordings of faults and switching transientsand eventually implemented in a real protection system.

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