

## Implementation of Dynamic Voltage Restorer for FCI in Distribution Systems

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### Abstract—

*This project introduces and evaluates an auxiliary control strategy for downstream fault current interruption in a radial distribution line by means of a dynamic voltage restorer (DVR). The proposed controller supplements the voltage-sag compensation control of the DVR. It does not require phase-locked loop and independently controls the magnitude and phase angle of the injected voltage for each phase. Fast least error squares digital filters are used to estimate the magnitude and phase of the measured voltages and effectively reduce the impacts of noise, harmonics, and disturbances on the estimated phasor parameters, and this enables effective fault current interrupting even under arcing fault conditions. The main drawback of this approach is that the dc-link voltage of the DVR increases due to real power absorption during fault current limiting operation and necessitates overcome the aforementioned limitations, this project proposes an augmented control strategy for the dvr that provides: 1) voltage-sag compensation under balanced and unbalanced conditions and 2) a fault current interruption (FCI) function. A switch to bypass the DVR when the protective relays, depending on the fault conditions, do not rapidly clear the fault. The adopted DVR converter is comprised of three independent H-bridge VSCs that are connected to a common dc-link capacitor. These VSCs are series connected to the supply grid, each through a single-phase transformer. The proposed FCI control system consists of three independent and identical controller's one for each single-phase VSC of the DVR. This paper introduces an auxiliary control mechanism to enable the DVR to interrupt downstream fault currents in a radial distribution feeder. The current ripples can be reduced by using SVPWM technique. This control function is an addition to the voltage-sag compensation control of the DVR. The performance of the proposed controller, under different fault scenarios, including arcing fault conditions, is investigated based on time-domain simulation studies in the MATLAB/SIMULINK environment.*

**Index Terms**—Digital filters; dynamic voltage restorer (DVR); fault current interrupting; multi loop control; Space vector pulse width modulation (SVPWM)

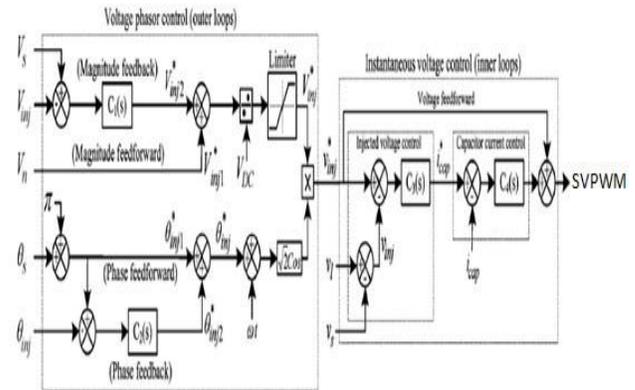
**I. INTRODUCTION** :Voltage sag, voltage swell and harmonics are major power quality problems concern of the industrial and commercial electrical consumers due to enormous loss in terms of time and money. This is due to the advent of a large numbers of sophisticated electrical and electronic equipment, such as computers, programmable logic controllers,

variable speed drives, and so forth. The use of this equipment often requires very high quality power supplies. Some special equipment are sensitive to voltage disturbances, especially if these take up to several periods, the circuit does not work. Therefore, these adverse effects of voltage changes necessitate the existence of effective mitigating devices. There are various solutions to

these problems. One of the most effective solutions is the installation of a Dynamic Voltage Restorer (DVR). DVR is a series custom power device, which has excellent dynamic capabilities. It is well suited to protect sensitive loads from duration voltage sag or swell. A DVR is basically a controlled voltage source installed between the supply and a sensitive load. It injects a voltage on the system in order to compensate any disturbance affecting the load voltage. Basic operating principle of a DVR is as shown in Fig.1. In August 1996, Westinghouse Electric Corporation installed world's first dynamic voltage restorer in Duke Power Company's 12.47 kV substation in Anderson, South Carolina. This was installed to provide protection to an automated rug manufacturing plant. Prior to this connection, the restorer was first installed at the Waltz Mill test facility near Pittsburgh for full power tests. THE dynamic voltage restorer (DVR) is a custom power device utilized to counteract voltage sags [2], [3]. It injects controlled three-phase ac voltages in series with the supply voltage, subsequent to a voltage sag, to enhance voltage quality by adjusting the voltage magnitude, wave shape, and phase angle [4]–[7]. The main components of a DVR (i.e., a series transformer  $T$ , a voltage - source converter (VSC), a harmonic filter, a dc-side capacitor  $CDC$ , and an energy storage device [8], [9]). The line-side harmonic filter [6] consists of the leakage inductance of the series transformer  $L_f$  and the filter capacitor  $C$ .

The DVR is conventionally bypassed during a downstream fault to prevent potential adverse impacts on the fault and to protect the DVR components against the fault current [10]–[12]. A technically elaborate approach to more efficient utilization of the DVR is to equip it with additional controls and enable it also to limit or interrupt the downstream fault currents. A control

approach to enable a DVR to serve as a fault current limiter is provided in [10].



The main drawback of this approach is that the dc-link voltage of the DVR increases due to real power absorption during fault current limiting operation and necessitates a switch to bypass the DVR when the protective relays, depending on the fault conditions, do not rapidly clear the fault. The dc-link voltage increase can be mitigated at the cost of a slow-decaying dc fault current component using the methods introduced in [8] and [13]. To overcome the aforementioned limitations, this paper proposes an augmented control strategy for the dvr that provides: 1) voltage-sag compensation under balanced and unbalanced conditions and 2) a fault current interruption (fci) function. The former function has been presented in [14] and the latter is described in this paper. It should be noted that limiting the fault current by the DVR disables the main and the backup protection (e.g., the distance and the over current relays). This can result in prolonging the fault duration. Thus, the DVR is preferred to reduce the fault current to zero and interrupt it and send a trip signal to the upstream relay or the circuit breaker (CB). It should be noted that the FCI function requires 100% voltage injection capability. Thus, the power ratings of the series transformer and the VSC would be about three times those of a conventional DVR with

about 30%–40% voltage injection capability. This leads to a more expensive DVR system. Economic feasibility of such a DVR system depends on the importance of the sensitive load protected by the DVR and the cost of the DVR itself. The performance of the proposed control scheme is evaluated through various simulation studies in the MATLAB/SIMULINK platform. The study results indicate that the proposed control strategy: 1) limits the fault current to less than the nominal load current and restores the PCC voltage within less than 10 ms, and interrupts the fault current within two cycles; 2) it can be used in four- and three-wired distribution systems, and single-phase configurations; 3) does not require phase-locked loops; 4) is not sensitive to noise, harmonics, and disturbances and provides effective fault current interruption even under arcing fault conditions; and 5) can interrupt the downstream fault

## II. PROPOSED FCI CONTROL STRATEGY :

The adopted DVR converter is comprised of three independent H-bridge VSCs that are connected to a common dc-link capacitor. These VSCs are series connected to the supply grid, each through a single-phase transformer. The proposed FCI control system consists of three independent and identical controller's one for each single-phase VSC of the DVR. Assume the fundamental frequency components of the supply voltage, load voltage, and the injected voltage. The FCI function requires a phasor parameter estimator (digital filter) which attenuates the harmonic contents of the measured signal. To attenuate all harmonics, the filter must have a full-cycle data window length which leads to one cycle delay in the DVR response. Thus, a compromise between the voltage injection speed and disturbance attenuation is made. The designed LES filters

utilize a data window length of 50 samples at the sampling rate of 10 kHz and, hence, estimate the voltage phasor parameters in 5 ms. Fig. 3 depicts the frequency response of the LES filters and indicates significant attenuation of voltage noise, harmonics, and distortions at frequencies higher than 200 Hz and lower than 50 Hz. Reference [13] demonstrates the effectiveness of this filter in attenuating the noise, harmonics, and distortions for the sag compensation mode of operation as well. The next section shows that this filter also performs satisfactorily in the FCI operation mode, even under arcing fault conditions where the measured voltage and current signals are highly distorted. The control system of Fig. 2 utilizes  $v$ ,  $l$ , the dc-link voltage  $V_{DC}$ , and the harmonic filter capacitor current  $i_{cap}$ , as the input signals. The reported studies in this paper are based on the over current fault detection method of [7] and [12]. The fault detection mechanism for each phase is activated when the absolute value of the instantaneous current exceeds twice the rated load current. The proposed multi loop control system [3], [8], [9], [15]–[20] includes an outer control loop (voltage phasor control) and an inner control loop (instantaneous voltage control). The inner loop provides damping for the transients caused by the DVR harmonic filter [18] and [21], and improves the dynamic response and stability of the DVR. The inner loop is shared by the sag compensation and the FCI functions. When a downstream fault is detected, the outer loop controls the injected voltage magnitude and phase angle of the faulty phase(s) and reduces the load-side voltage to zero, to interrupt the fault current and restore the PCC voltage. The DVR —outer| voltage phasor control and —inner| instantaneous voltage control, corresponding to each phase, are described in the following two subsections. A. Voltage Phasor Control System In the FCI

operation mode, the required injected voltage phasor is equal to the source voltage phasor, but in phase opposition [i.e., the injected phasor  $V_{inj} = V_{inj} \angle \theta_{inj}$  is controlled to be  $V_S \angle (\theta_S + \pi)$ ]. Performance of the voltage phasor control, in terms of transient response, speed, and steady-state error, is enhanced by independent control of voltage magnitude and phase, and incorporating feed forward signals to the feedback control system [17], [18], [21]–[27]. Fig. 2 shows two proportional- integral (PI) controllers ( and ) that are used to eliminate the steady-state errors of the magnitude and phase of the injected voltage, respectively. Parameters of each controller are determined to achieve a fast response with zero steady-state error. The output of the phasor control system is a reference phasor denoted by  $V_{inj}^* = V_{inj}^* \angle \theta_{inj}^*$ . To eliminate the effects of the dc-link voltage variations on the injected voltages,  $V_{inj}^*$  is normalized by  $V_d$ . The magnitude and the phase angle of  $V_{inj}^*$  are independently calculated and the magnitude is passed through a limiter (Fig. 1). The resulting phasor magnitude and phase angle are converted to the sinusoidal signal  $V_{inj}^*$ , which is the reference signal for the instantaneous voltage control.

**B. Instantaneous Voltage-Control System**

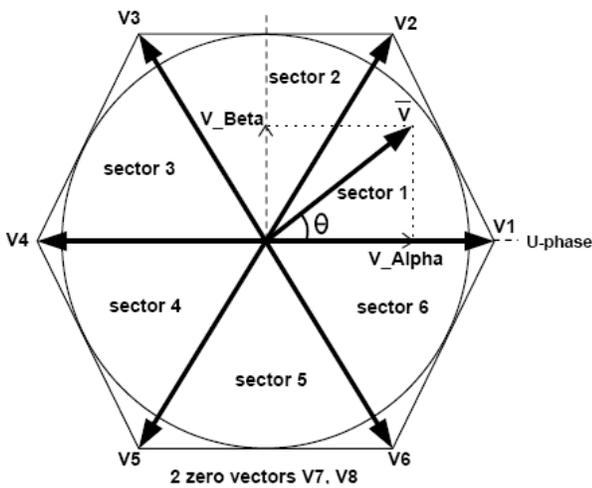
Under ideal conditions, a voltage sag can be effectively compensated if the output of the phasor-based controller  $V_{inj}^*$ , is directly fed to the sinusoidal pulse-width modulation (SPWM) unit. However, resonances of the harmonic filter cannot be eliminated under such conditions. Therefore, to improve the stability and dynamic response of the DVR, an instantaneous injected voltage controller and a harmonic filter capacitor current controller are used to attenuate resonances. The generated reference signal for the injected voltage  $V_{inj}^*$  is compared with the measured injected voltage  $V_{in}$ , and the error is

fed to the voltage controller. As shown in Fig. 2, the output of the voltage controller  $ica^*$  is the reference signal for the filter capacitor current control loop. It is compared with the measured capacitor current  $ica$ , and the error is fed to the current controller. The steady-state error of the proposed control system is fully eliminated by the PI controllers in the outer control loop (i.e.,  $C1$  and  $C2$ ), which track dc signals (magnitude and phase angle). Therefore, there is no need for higher order controllers in the inner control loop which are designed based on sinusoidal references. Thus, in Fig. 2,  $C3$  and  $C4$  are pure gains  $kv$  and  $K$ , respectively. A large  $kv$  result in amplification of the DVR filter resonance and can adversely impact the system stability [18]. Thus, the transient response of the DVR is enhanced by a feed forward loop, and a small proportional gain is utilized as the voltage controller. A large  $Kc$  damps the harmonic filter resonance more effectively, but it is limited by practical considerations (e.g., amplification of capacitor current noise, measurement noise, and dc offset [18]). Therefore, the lowest value of the proportional gain which can effectively damp the resonances is utilized. The output of the current controller is added to the feed forward voltage to derive the signal for the PWM generator.

### III. SPACE VECTOR PWM :

The Space Vector PWM generation module accepts modulation index commands and generates the appropriate gate drive waveforms for each PWM cycle. This section describes the operation and configuration of the SVPWM module. A inverter with dc link configuration can have eight possible switching states, which generates output voltage of the inverter. Each inverter switching state generates a voltage Space Vector ( $V1$  to  $V6$  active vectors,  $V7$  and  $V8$  zero voltage vectors) in the Space Vector plane

(Figure: space vector diagram). The magnitude of each active vector (V1 to V6) is  $\frac{2}{3} V_{dc}$  (dc bus voltage). The Space Vector PWM (SVPWM) module inputs modulation index commands ( $V_{\alpha}$  and  $V_{\beta}$ ) which are orthogonal signals (Alpha and Beta) as shown in Figure. The gain characteristic of the SVPWM module is given in Figure 3. The vertical axis of Figure represents the normalized peak motor phase voltage ( $V/V_{dc}$ ) and the horizontal axis represents the normalized modulation index ( $M$ ).

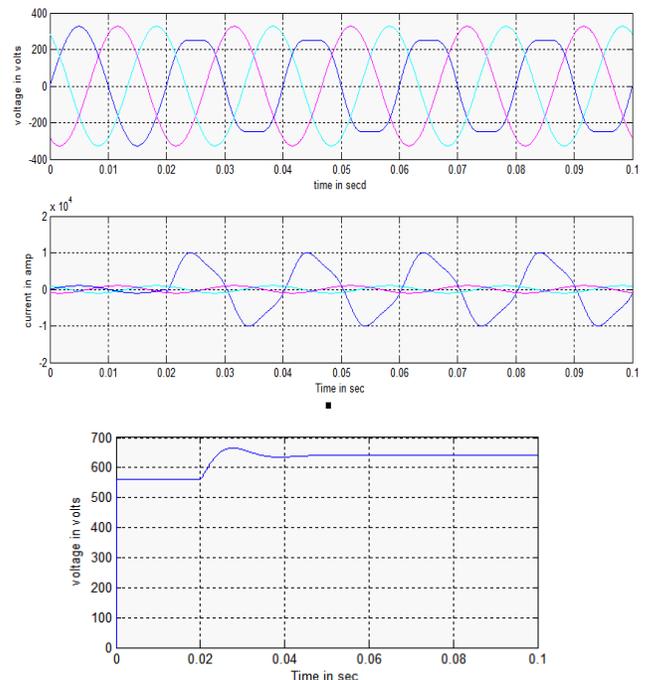


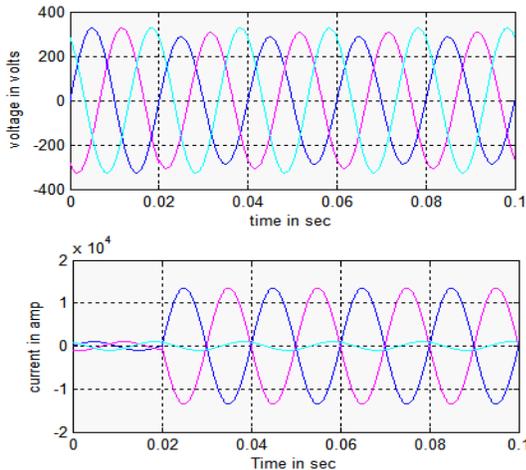
Over modulation occurs when modulation  $U_{mag} > U_{magL}$ . This corresponds to the condition where the voltage vector in (Figure: voltage vector rescaling) increases beyond the hexagon boundary. Under such circumstance, the Space Vector PWM algorithm will rescale the magnitude of the voltage vector to fit within the Hexagon limit. The magnitude of the voltage vector is restricted within the Hexagon; however, the phase angle ( $\theta$ ) is always preserved. The transfer gain (Figure: transfer characteristics) of the PWM modulator reduces and becomes non-linear in the over modulation region

**IV SIMULATION RESULTS:** A depicts a single-line diagram of a power system which is used to evaluate the performance of the proposed

DVR control system under different fault scenarios, in the MATLAB/SIMULINK software environment. A 525-kVA DVR system is installed on the 0.4-kV feeder, to protect a 500-kVA, 0.90 lagging power factor load against voltage sags. Parameters of the simulated power system and the DVR are given in Appendix A. In the reported studies, the base voltage for per-unit values is the nominal phase voltage. Besides, voltage and current waveforms of phases A, B, and C are plotted by solid, dashes, and dotted lines, respectively. Fig. 4. Single-line diagram of the system used for simulation studies.

(a) Voltages at bus3. (b) Fault currents, during downstream threephase fault when the DVR is inactive (bypassed)





**V. CONCLUSION** .The study results conclude that:

- The proposed multiloop control system provides a desirable transient response and steady-state performance effectively.
- The proposed control system detects and effectively interrupts the various downstream fault currents within two cycles (of 50 Hz);
- The proposed fault current interruption strategy limits the DVR dc-link voltage rise, caused by active power absorption, to restore the PCC voltage without interruption; in addition, it interrupts the downstream fault currents even under low dc-link voltage conditions.
- By using SVPWM technique the current ripples can be mitigated.
- The proposed control system also performs satisfactorily under downstream arcing fault conditions.

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