International Journal of Research (IJR)
e-ISSN: 2348-6848, p- ISSN: 2348-795X Volume 2, Issue 10, October 2015
Available at http://internationaljournalofresearch.org

Accomplishment of Dynamic Double-Tail Comparator intended for High Speed Applications

M.Mahesh*[1], R. Murali Krishna*[2], M.Nagesh*[3]
Department of ECE, Swarnandhra College of Engg & Tech.,A.P,India
mmahesh401@gmail.com*[1] muralirapaka@gmail.com*[2] nagesh8320@gmail.com*[3]

ABSTRACT:
In the present scenario, need for ultra low-power, area efficient and high speed analog-to-digital converters (ADCs) is pushing toward the use of dynamic Clocked regenerative comparators to improve the power efficiency and speed. In this work , we modified the structure of the Dynamic Double-Tail Comparator by adding few additional transistors to the existing structure. The proposed modified Double-Tail Dynamic Comparator is used for fast operations even in very small supply voltages. We can implement the proposed structure and existing structures of Dynamic Comparator in Mentor Graphics Tool. From simulation results in 0.18-µm CMOS technology, we find that the proposed design yields less Delay than the existing structures.

Keywords - dynamic clocked comparator; Double-tail comparator; low-power analog design high-speed analog-to-digital converters (ADCs)

1. INTRODUCTION

COMPARATOR is one of the essential building blocks in most of the analog-to-digital converters (ADCs).Many high speeds ADCs, such as flash, pipeline, successive approximation ADCs require low power high-speed comparators with in a small chip area. High-speed comparators in ultra deep sub micrometer (UDSM) CMOS technologies suffer from low supply voltages especially when considering fact that threshold voltages of the devices have not been scaled at the equal pace as the supply voltages of the modern CMOS processes. Hence, designing high-speed comparators is a number of challenges, when the supply voltage is smaller. In other words, in a given technology to achieve high speed, larger transistors are needed to compensate the reduction of supply voltage, which also means that more power and die area is needed. Besides, low-voltage process results in limited common-mode input range, which is very significant in many high-speed analog-to-digital converter architectures, such as flash two-step, folding ADCs. Various techniques, such as supply boosting methods, techniques employ body-driven transistors, current-mode design and those using dual-oxide processes, which can handle very higher supply voltages have been developed to meet up the low-voltage design challenges. Boosting and bootstrapping are the two techniques based on augmenting the clock voltage or supply, reference to address switching problems and input-range. These are effective techniques, but they introduce reliability issues especially in UDSM CMOS technologies. Body-driven technique adopted that remove the threshold voltage requirements such that body driven MOSFET operates as depletion-type device. the body driven transistor's suffers from the smaller trans conductance (equal to the g_{mb} of the transistor) compared to its gate-driven counterpart while special fabrication process, such as a deep n-well is needed to have both PMOS and NMOS transistors are operate in body-driven configuration. Apart from technological modifications, developing novel circuit structures which avoid stacking too many transistors between supply rails is preferable for a low-voltage operation, especially if they don't increase the circuit complexity. In additional circuitry is added to the conventional dynamic comparator to enhance the comparator speed in low supply voltages. The structure of double-tail dynamic comparator first proposed is based on the designing separate input and cross coupled stage.

International Journal of Research (IJR)
e-ISSN: 2348-6848, p- ISSN: 2348-795X Volume 2, Issue 10, October 2015
Available at http://internationaljournalofresearch.org

This separation is enables the fast operation over a wide supply voltage range.

In this paper, we propose a new structure for dynamic comparator. The proposed structure doesn't require stacking of too many transistors or boosted voltages. Merely adding few minimum-size transistors to the conventional double-tail dynamic comparator, latch delay time profoundly reduced. This alteration (modification) also results in considerable Power savings when compared to the conventional dynamic comparator and double-tail dynamic comparator.

II. CLOCKED REGENERATIVE COMPARATORS

The Clocked regenerative comparators have found wide applications, many high-speed analog to-digital converter architectures since they can make high speed decisions due to the strong positive feedback in the regenerative latch. Recently many comprehensive analyses have been presented, which investigate the performance of these comparators from the different aspects such as power dissipation and time delay analysis is presented here, the delay time of two common structures i.e., conventional single-tail dynamic comparator and conventional dynamic double-tail comparator's are analyzed based on which the proposed comparator will be obtainable (presented).

A. Conventional single-tail Dynamic Comparator

The schematic diagram of conventional single-tail dynamic comparator broadly used in analog to -digital converters, with rail-to-rail output swing, high input impedance, and no static power consumption is shown in the Fig. 1 . The operation of the conventional single-tail dynamic comparator is as follows. During the reset phase when the CLK = 0 and *M*tail is off, reset transistors (*M*7–*M*8) pull both output nodes Ouput*N* and Out*putP* to V_{DD}(0.8v) to define a start condition, this is valid logical level during reset phase. In the Comparison phase, when V_{DD} = CLK, transistors *M*7 and *M*8 are off condition , and *M*tail is on state. Output voltages (Ouput*N* and Out*putP*), which had been pre-charged to V_{DD}, start to the discharge with different discharging rates depending on corresponding input voltage (inputN/inputP). Assuming the case where $V_{inputP} > V_{inputN}$, Out*putP* discharges earlier than Ouput*N* hence when Out*putP* (discharged by the transistor *M*2 drain current), falls down to the $V_{DD}-|V_{thp}|$. Before Ouput*N* (discharged by the transistor *M*1 drain current), the corresponding pMOS transistor (*M*5) will turn on initiate the latch regeneration caused by back-to-back inverters (*M*3, *M*5 and *M*4, *M*6). Thus Ouput*N* pulls to V_{DD} and Out*putP* discharges to ground. If $V_{inputp} < V_{inputn}$ the circuits works as vice versa.

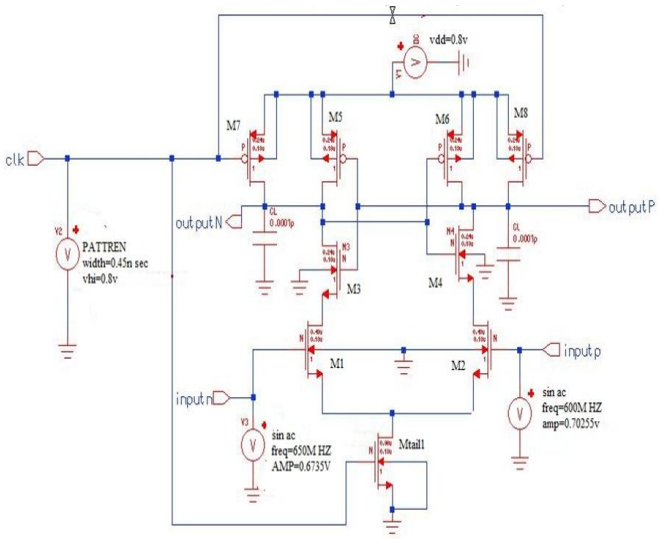

Fig. 1. Schematic diagram of the conventional single-tail dynamic comparator

The simulation result of conventional single-tail dynamic comparator As shown in Fig. 2, the delay of this comparator is obtained from two time delays, that is t_0 and t_{latch}. The delay t_0 denotes the capacitive discharge of the load capacitance (C_L) until the first p-channel transistor (*M*6/*M*5) turns on. In case the voltage at node V_{inputP} is bigger than V_{inputN} (i.e., $V_{inputP} > V_{inputN}$,), the drain current of the transistor *M*2 (I_2) causes faster discharge of the Out*putP* node compared to

International Journal of Research (IJR)
e-ISSN: 2348-6848, p- ISSN: 2348-795X Volume 2, Issue 10, October 2015
Available at http://internationaljournalofresearch.org

the Ouput*N* node, which is driven by M1 with smaller current.

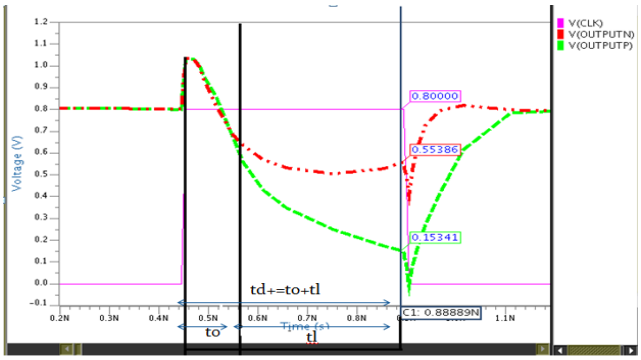

Fig. 2. Transient simulations of the conventional single-tail dynamic comparator at V_{cm} = 0.7 V, and V_{DD} = 0.8 V.

The second term, t_{latch}, is the latching delay of two cross coupled inverters. It is assumed that a voltage swing of $\Delta V_{out} = V_{DD}/2$ has to be obtained from an initial output voltage difference ΔV_0 at the falling output (e.g., Outp). Half of the supply voltage is considered to be the threshold voltage of the comparator following inverter or SR latch.

In principle, this structure has the advantages of high input impedance, rail-to-rail output swing, no static power consumption, and good robustness against noise and mismatch. Due to the fact that parasitic capacitances of input transistors do not directly affect the switching speed of the output nodes, it is possible to design large input transistors to minimize the offset. The disadvantage, on the other hand, is the fact that due to several stacked transistors, a sufficiently high supply voltage is needed for a proper delay time. The reason is that, at the beginning of the decision, only transistors M_3 and M4 of the latch contribute to the positive feedback until the voltage level of one output node has dropped below a level small enough to turn on transistors M5 or M6 to start complete regeneration. At a low supply voltage, this voltage drop only contributes a small gate-source voltage for transistors M3 and M4, where the gate source voltage of M5 and M6 is also small; thus, the delay time of the latch becomes large due to lower transconductances.

Another important drawback of this structure is that there is only one current path, via tail transistor Mtail, which defines the current for both the differential amplifier and the latch (the cross-coupled inverters). While one would like a small tail current to keep the differential pair in weak inversion and obtain a long integration interval and a better G_m/I ratio, a large tail current would be desirable to enable fast regeneration in the latch. Besides, as far as Mtail operates mostly in triode region, the tail current depends on input common-mode voltage, which is not favorable for regeneration.

B. Conventional Double-Tail Dynamic Comparator

The schematic diagram of Conventional double-tail comparator is shown in Fig. 3. This topology has less stacking and therefore can operate small supply voltages compare to the conventional single-tail dynamic comparator. The double tail enables both large currents in the latching stage and wider *M*tail2, for a fast latching is independent of input common-mode voltage , and a lower current in the input stage (small *M*tail1), for low offset voltages. The operation of Conventional double-tail comparator is as follows. During reset period (CLK = 0, and *M*tail2 and *M*tail1off),transistors *M*4-*M*3 pre-charge fp and fn nodes to V_{DD}, which in turn causes transistors *M*R2 and *M*R1 to discharge the output nodes to ground. During decision-making phase (CLK = V_{DD} = 0.8v, *M*tail1 and *M*tail2 turn on), *M*4-*M*3 turn off and voltages at nodes fp and fn start to drop with the rate is defined by $I_{Mtail1}/C_{fn(p)}$ and on top of this, an input-dependent differential voltage $\Delta V_{fn(p)}$ will build up. The intermediate stages formed by *M*R2 and *M*R1 passes $\Delta V_{fn(p)}$ to the cross coupled inverters and also provides good shielding between output's and input's, resulting in reduced value of kickback noise .

International Journal of Research (IJR)
e-ISSN: 2348-6848, p- ISSN: 2348-795X Volume 2, Issue 10, October 2015
Available at http://internationaljournalofresearch.org

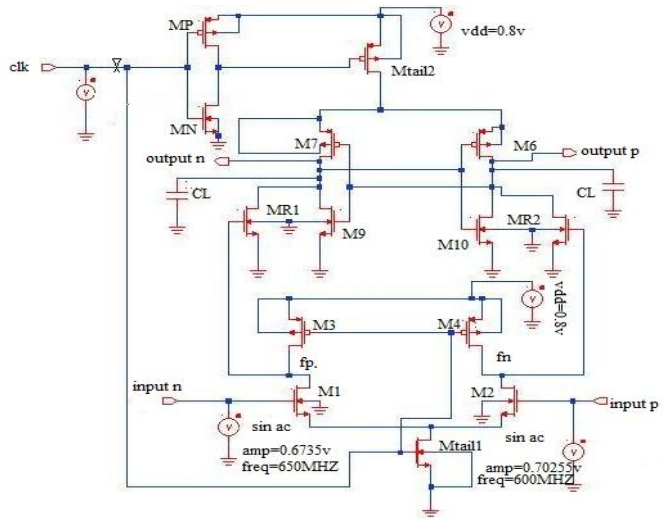

Fig.3. Schematic diagram of the conventional double-tail dynamic comparator

The simulation result of conventional double-tail dynamic comparator as shown in Fig. 4,Similar to the conventional single-tail dynamic comparator, the delay of this Conventional double-tail comparator comprises two main parts, t_{latch} and t_0.The delay t_0 refer to the capacitive charging of the load capacitance (C_{lout}) (at the latch stage output nodes OutputN and Out*putP*) until the first n-channel transistor (*M*10/*M*9) turns on, after which the latch regeneration starts. The regeneration time (t_{latch}) starts after first n-channel transistor of the latch turns on condition(for instance *M*9), the corresponding output will be discharged to the ground, leading front p-channel transistor (e.g., *M*8) to turn on condition, charging another output (Out*putP*) to the supply voltage V_{DD}.

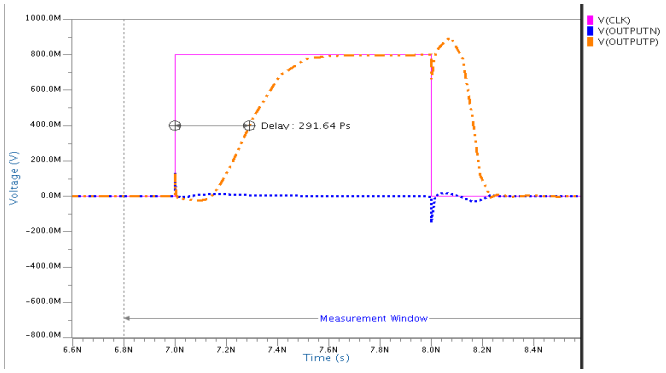

Fig. 4. Transient simulations of the conventional double-tail dynamic comparator for input voltage difference of V_{cm} = 0.7 V, and V_{DD} = 0.8 V.

In this comparator both intermediate stage transistor's will be finally cut-off state, (since fp and fn nodes both are discharge to the ground), hence they do not play any significant role in improving effective transconductance of the latch. Besides, during the reset phase these nodes have to
be charged from ground to V_{DD}, which means power consumption.

III. PROPOSED DOUBLE-TAIL DYNAMIC COMPARATOR

The Fig. 5 demonstrates the schematic diagram of the proposed dynamic double-tail comparator. Due to the better performance of double-tail comparator architecture in low-voltage applications, the proposed comparator is designed based on the double-tail configuration. The main idea of the proposed comparator is to increase $\Delta V_{fn/fp}$ in order to increase latch regeneration speed. For this purpose, we have to add two control transistors (*M*c2 and *M*c1) of first stage in parallel to *M3*/*M*4 transistors but in a cross-coupled manner [see Fig.5].

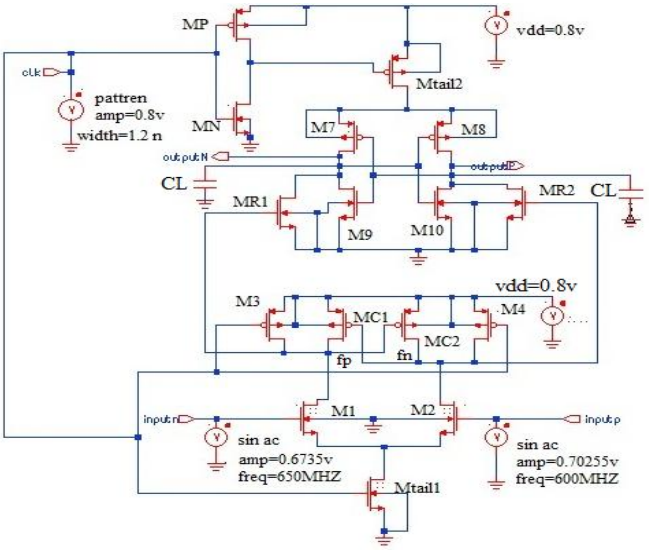

Fig.5. Schematic diagram of the proposed dynamic comparator.

A. Operation of the Proposed Comparator

The operation of proposed comparator is as follows: During reset period (CLK = 0, *M*tail1

International Journal of Research (IJR)
e-ISSN: 2348-6848, p- ISSN: 2348-795X Volume 2, Issue 10, October 2015
Available at http://internationaljournalofresearch.org

and *M*tail2 are off condition, avoiding static power consumption), *M*4 and *M*3 pulls both fp and fn nodes to V_{DD}, hence transistors *M*c1 and *M*c2 are cut off state. Intermediate stage transistors, *M*R1 and *M*R2 are reset both latch outputs to ground. During decision-making phase (CLK = V_{DD}=0.8v, *M*tail2, and *M*tail1 are on state), transistors *M*3 and *M*4 turn off. Furthermore at the beginning of this phase, the control transistors are still off condition (since fp and fn are about V_{DD}). Thus fp and fn start to drop with the different rates according to the input voltages (inputp and inputn).Suppose $V_{inputp} > V_{inputn}$, thus the fn drops faster than fp, (since *M*2 provides more current than *M*1current). As long as fn continues falling, the corresponding pMOS control transistor *M*c1 starts to turn on, pulling fp node back to the V_{DD}, so another control transistor *M*c2 remains off state, allowing fn to be a discharged completely. In other words, unlike conventional double-tail dynamic comparator, in which $\Delta V_{fn/fp}$ is just a function of a input transistor transconductance and input voltage difference, the proposed structure as soon as the comparator detect that for instance node fn discharges faster, a pMOS transistor *M*c1 turns on, pulling other node fp back to the V_{DD}. Therefore by the time passing the difference between fp and fn ($\Delta V_{fn/fp}$) increases in an a exponential manner, leading to the decrease of the latch regeneration time.

The simulation result of proposed double-tail dynamic comparator as shown in Fig. 6, Similar to the conventional double-tail dynamic comparator, the delay of this proposed double-tail comparator comprises two main parts, t_{latch} and t_0.

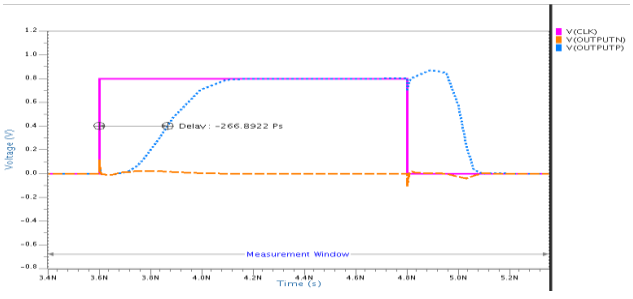

Fig.6. Transient simulations of the proposed double-tail dynamic comparator for *V*DD = 0.8 V.

The below Fig.7 shows the Hand Drawn layout of Proposed Dynamic comparator.

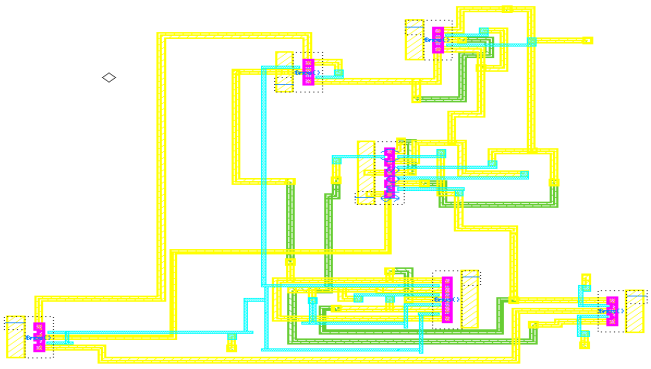

Fig.7. Layout of the proposed double-tail dynamic comparator

IV.PERFORMANCE ANALYSYS

In order to compare the proposed dynamic comparator with the single-tail and conventional double-tail dynamic comparator, all circuits have been simulated in a 0.18-µm CMOS technology with V_{DD} = 0.8 V.

Table I and Fig.8 compares the performance of the proposed comparator with single-tail and the conventional double-tail dynamic comparators. In 0.18-µm CMOS technology, the proposed comparator provides the less delay at 0.8V supply voltage.

Table- I: Performance Comparision of Dynamic Comparators

Comparator structure	Conventional single-tail Dynamic Comparator	Conventional Double-tail Dynamic Comparator	Proposed Dynamic Comparator
CMOS Technology	180 nm	180 nm	180 nm
Supply Voltage	0.8 V	0.8 V	0.8 V
Maximum Sampling Frequency	1 GHz	2 GHz	2.4 GHz
Power Dissipation	5.8606 pw	11.0453 pw	11.0453 pw
Delay	422.23ps	291.64ps	266.66ps
Number of Transistors	9	12	14

International Journal of Research (IJR)
e-ISSN: 2348-6848, p- ISSN: 2348-795X Volume 2, Issue 10, October 2015
Available at http://internationaljournalofresearch.org

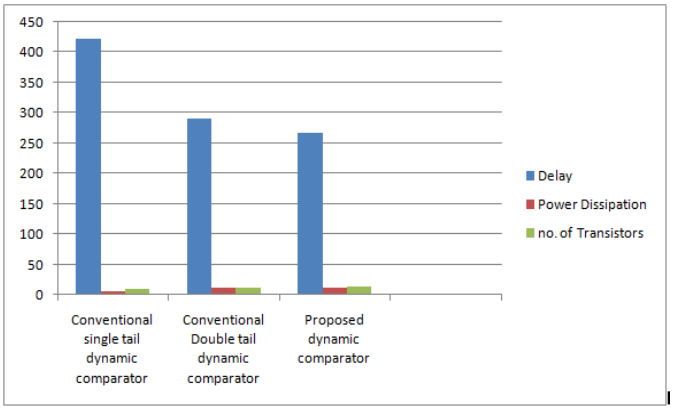

Fig.8.Comparison of Dynamic comparator Architectures

V.CONCLUSION

In this paper, we modifie the structure of the Dynamic Double-Tail Comparator by adding few additional transistors to the existing structure. The proposed modified Double-Tail Dynamic Comparator is used for low-power and fast operations even in very small supply voltages. We were implement the proposed structure and existing structures of Dynamic Comparator in Mentor Graphics Tool.From simulation results in 0.18-µm CMOS technology confirmed that the delay of the proposed comparator is reduced to a great extent in comparison with the single-tail and conventional double-tail dynamic comparator.

REFERENCES

[1] Samaneh Babayan-Mashhadi and Reza Lotfi," Analysis and Design of a Low-Voltage Low-Powe Double-Tail Comparator" IEEE Transactions on Very Large Scale Integration (VLSI) Systems, vol. 22, no. 2, February 2014

[2] Goll and H. Zimmermann, "A comparator with reduced delay time in 65-nm CMOS for supply voltages down to 0.65," *IEEE Trans. Circuits Syst. II, Exp. Briefs*, vol. 56, no. 11, pp. 810–814, Nov. 2009.

[3] S. U. Ay, "A sub-1 volt 10-bit supply boosted SAR ADC design in standard CMOS," *Int. J. Analog Integr. Circuits Signal Process.*, vol. 66, no. 2, pp. 213–221, Feb. 2011.

[4] Mesgarani, M. N. Alam, F. Z. Nelson, and S. U. Ay, "Supply boosting technique for designing very low-voltage mixed-signal circuits in standard CMOS," in *Proc. IEEE Int. Midwest Symp. CircuitsSyst. Dig. Tech. Papers*, Aug. 2010, pp. 893–896.

[5] J. Blalock, "Body-driving as a Low-Voltage Analog Design Techniquefor CMOS technology," in *Proc. IEEE Southwest Symp. MixedSignal*

[6] M. Maymandi-Nejad and M. Sachdev, "1-bit quantiser with rail to rail input range for sub-1V __ modulators," *IEEE Electron. Lett.*, vol. 39, no. 12, pp. 894–895, Jan. 2003.

[7] Y. Okaniwa, H. Tamura, M. Kibune, D. Yamazaki, T.-S. Cheung, J. Ogawa, N. Tzartzanis, W. W. Walker, and T. Kuroda, "A 40Gb/ s CMOS clocked comparator with bandwidth modulation technique," *IEEE J. Solid-State Circuits*, vol. 40, no. 8, pp. 1680–1687, Aug. 2005.

[8] Goll and H. Zimmermann, "A 0.12 μm CMOS comparator requiring 0.5V at 600MHz and 1.5V at 6 GHz," in *Proc. IEEE Int. Solid-State Circuits Conf., Dig. Tech. Papers*, Feb. 2007, pp. 316–317.

[9] B.Goll and H. Zimmermann, "A 65nm CMOS comparator with modified latch to achieve 7GHz/1.3mW at 1.2V and 700MHz/47μW at 0.6V," in *Proc. IEEE Int. Solid-State Circuits Conf. Dig. Tech. Papers*, Feb. 2009, pp. 328–329.

[10] B. Goll and H. Zimmermann, "Low-power 600MHz comparator for 0.5 V supply voltage in 0.12 μm CMOS," *IEEE Electr Lett.*, vol. 43,no. 7, pp. 388–390, Mar. 2007.

[11] D. Shinkel, E. Mensink, E. Klumperink, E. van Tuijl, and B. Nauta, "A double-tail latch-type voltage sense amplifier with 18ps Setup+Hold time," in *Proc. IEEE Int. Solid-State Circuits Conf., Dig. Tech. Papers*, Feb. 2007, pp. 314–315.

[12] P. Nuzzo, F. D. Bernardinis, P. Terreni, and G. Van der Plas, "Noiseanalysis of regenerative comparators for reconfigurable ADC architectures," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 55, no. 6, pp. 1441–1454, Jul. 2008.

[13] Nikoozadeh and B. Murmann, "An analysis of latched comparator of fset due to load capacitor mismatch," *IEEE Trans. Circuits Syst. II, Exp. Briefs*, vol. 53, no. 12, pp. 1398–1402, Dec. 2006.

[14] S. Babayan-Mashhadi and R. Lotfi, "An offset cancellation technique for comparators using body-voltage trimming," *Int. J. Analog Integr Circuits Signal Process.*, vol. 73, no. 3, pp. 673–682, Dec. 2012.

[15] J. He, S. Zhan, D. Chen, and R. J. Geiger, "Analyses of static and dynamic random offset voltages in dynamic comparators," *IEEE Trans.Circuits Syst. I, Reg. Papers*, vol. 56, no. 5, pp. 911–919, May 2009.

[16] J. Kim, B. S. Leibowits, J. Ren, and C. J. Madden, "Simulation and analysis of random decision errors in clocked comparators," *IEEE Trans Circuits Syst. I, Reg. Papers*, vol. 56, no. 8, pp. 1844–1857, Aug. 2009.

[17] P. M. Figueiredo and J. C. Vital, "Kickback noise reduction technique for CMOS latched comapartors," *IEEE Trans. Circuits Syst. II, Exp. Briefs*, vol. 53, no. 7, pp. 541–545, Jul. 2006.

[18] Wicht, T. Nirschl, and D. Schmitt-Landsiedel, "Yield and speed optimization of a latch-type voltage sense amplifier," *IEEE J. Solid-State Circuits*, vol. 39, no. 7, pp. 1148–1158, Jul. 2004.

[19] Johns and K. Martin, *Analog Integrated Circuit Design*, New York, USA: Wiley, 1997.

[20] Kota Kinabalu, Malaysia Low Power CMOS Charge Sharing Dynamic Latch Comparator using 0.18µm CMOS Technology, IEEE-RSM 2011.