Design and Simulation of Digital Carrier Tracking Technique for High Dynamic Spread Spectrum Receiver

1 .Mr. Mahender Gandikota & 2.Miss P.Chandramani

1. M.Tech, Arjun College Of Technology And Sciences, Mount Opera Premises, Batasingaram, Ranga Reddy Dist,Telangana, INDIA.

2. Asst.Professor, Arjun College Of Technology And Sciences, Mount Opera Premises, Batasingaram, Ranga Reddy Dist,Telangana, INDIA

Abstract

The missile to ground telemetry links are designed with spread spectrum techniques to achieve, security and noise immunity. There are various advantages for Spread Spectrum technique such as the ability of strong anti-jamming, low probability of intercept. It is extremely difficult to accomplish the carrier acquisition and tracking in this high dynamic and low signal-to-noise environments, especially in the case of high data rate and long PN code. Carrier synchronization includes acquisition and tracking in Spread Spectrum Systems. The Carrier acquisition also can be seen as rough estimate of the Doppler frequency shift, which is usually included in the process of PN code synchronization and finished by threshold decision for the value of correlation operation.

In this project the digital carrier tracking technique with a structure of frequency-locked loop (FLL) assisted phase-locked loop (PLL) is designed and simulated for high Doppler conditions. The frequency and phase decision are very easy to realize by programmable digital device. Due to the frequency pulling of FLL, the pass-band of the filter in PLL can be made very narrow to suppress the noise, and the PLL can lock the phase of carrier with high accuracy. In the proposed work, the study and simulation of crossproduct auto frequency tracking (CPAFC) and four phase frequency discrimination (atan2), and the improved digital Costas loop to achieve carrier synchronization will be carried out. The performance of the improved digital Costas loop is verified by simulation and this method works well in the environment when input signal changes in a large dynamic range.

MATLAB/GNU OCTAVE simulation tool will be used for simulation. The simulation results, applications, merits and demerits of proposed approach will be analyzed and will be documented.

INTRODUCTION:

A fundamental task of every Global Navigation Satellite System receiver is to synchronize with the visible satellite signals. Since Direct Sequence Spread Spectrum (DS-SS) signals are utilized, code and carrier synchronization is required, but a correlation stage is necessary to despread the signals before the synchronization algorithms can be applied. In real-time receivers the required economy of operations usually precludes the use of complex estimation schemes and tracking loops are preferred. Due to the correlation process these loops are necessarily discrete. The typical trade-off in tracking loop design is bandwidth versus dynamic performance: output noise increases with a larger loop bandwidth, while dynamic tracking error decreases with it [1]. Thus, the loop design becomes particularly challenging when the receivers are subject to high dynamics. To overcome this limitation other receiver structures have been proposed in [1], claiming tracking

capability up to 150 g of acceleration, in contrast with the 5 g regularly assigned to tracking loops. However, the required computational burden is large since several simultaneous correlations and Fast Fourier Transform (FFT) computations are needed. In this paper we show a careful design of the digital loops that can expand their tracking ability to acceleration steps up to 40 g or even more, keeping a low computational load and reasonable tracking threshold values at the same time. The loop structure known as FLL-assisted PLL [2] is very often adopted for GNSS receivers. It consists of a Phase-Locked Loop (PLL) and a Frequency-Locked Loop (FLL) in a coupled mode, with the advantage of reducing locking times and avoiding false locks. This solution is also a legacy of analog loops since the FLL or Automatic Frequency Control (AFC) has been used to reduce frequency errors as a previous stage to phase lock for analog PLL [3]. The advantages of adding the FLL to track spread spectrum signals in dynamic environments were already studied in [4]. For high-dynamics GNSS receivers, the focus is on carrier loops because the carrier shares the same dynamics as the code. Then, the estimation of the carrier frequency can be used to aid the estimation of the code frequency, and a first-order code loop is enough [5]. Usually, implementations of FLL-assisted PLL are not based on optimal digital loop solutions, with each loop designed separately, leaving the analysis of their interactions and possible modifications to the simulation stage [2, 5, 6]. Moreover, schemes adopted to discriminate phase or frequency errors are often justified because of their similarity with well-known analog solutions rather than with an optimality versus implementation complexity criterion. We will show that digital implementations of optimal discriminators are not necessarily more complex and allow designing the FLL-assisted PLL in a coupled way. Nevertheless, the FLL-assisted PLL leads to a more complex design and a computationally more expensive implementation than a single PLL. Moreover, when coupled-loops lose phase lock for a moment, they present cycle slips introducing a phase ambiguity. We will show how to use the same frequency information as that of an FLL to build a nonambiguous phase detector, the Unambiguous Frequency-Aided (UFA) phase discriminator. A PLL with this new phase discriminator, that is, a UFA-PLL, keeps the desirable properties of an FLL without demanding an extra loop and avoiding cycle slips. Other nonambiguous phase discriminators are known for analog PLLs, that is, with analog loop filter, such as the sequential discriminators built with flip-flops presented in [7, 8] or the nonsequential discriminator of [9]. While their goals are quite similar to ours, they increase the PLL implementation complexity, demanding some digital circuitry and a digital-to-analog converter to get the analog phase error. On the contrary, the UFA phase discriminator is easily implemented and naturally suited for a software-based PLL, leading to a less complex implementation than a FLL-assisted PLL. Section 2 introduces the UFA-PLL structure for GNSS tracking loops.

2. Digital Loop Models:

Correlations of the received signal with the locally generated replicas for each visible satellite are the inputs to the discriminator of the carrier tracking loops in a GNSS receiver. The complex correlation for a given satellite with carrier power to noise power spectral density and for the th correlation interval of duration
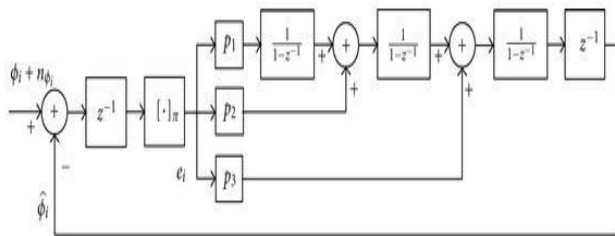
2.1. PLL Model

The phase estimation error is typically obtained using one of several possible discriminators [5], which give the desired phase modified by different memory-less nonlinearities. The optimal one—maximum likelihood estimator—is given bywhere the notation indicates that its argument is kept within the interval by adding or subtracting as many times as needed. The zero-mean noise term has a rather

complicated probability distribution [24], but in high it can be approximated by a Gaussian distribution with zero mean and variance .
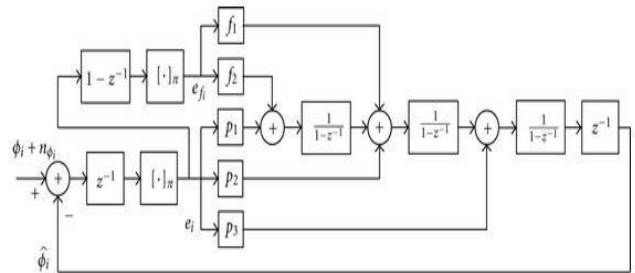
A four-quadrant is not appropriate if there is BPSK data modulation because the discriminator becomes sensitive to the data phase changes. On the contrary, for signals without data the range of the discriminator can be doubled with a four-quadrant . We chose this discriminator because it is not amplitude dependent and the calculation of can be easily implemented with a lookup table, since in practice and are frequently quantized to a few bits.

In order to close the loop in our model, it is of crucial importance to consider the delays present in a real implementation. Failure to account for a delay may turn unstable an optimal loop design. Since ours loops are digital, a single sample delay is expected but in fact there are two. One of them is due to the time spent in and calculations. The other delay appears because the estimated values used in the present correlations have to be known before the calculations begin. That is, the value is obtained with the loop filter output of the th correlation interval, which in turn is calculated with the estimation errors of . Then, with these considerations, the model of a PLL using the classical loop filter structure of type 3, that is, with three accumulators, is shown in Figure 1

2.2. FLL-Assisted PLL Model

To add an FLL to our previous PLL, a frequency discriminator is needed. In a digital loop a frequency error estimate may be obtained as the difference of two successive phase errors, and in fact this is often correct. A problem appears when the discontinuities caused by make that the difference to be wrong in . However, our discrete system cannot distinguish frequencies greater than half of the sample rate, that is, phase changes of between consecutive samples, and so the measured frequency errors must be bounded. In fact, if the phase discriminator is insensitive to BPSK data, the phase changes caused by frequency errors must lie in the interval [25]. Thus, the difference of two consecutive outputs of the phase discriminator can be corrected just using the operation . Therefore, the frequency discriminator for the FLL can be obtained byFigure 2 shows a diagram of the FLL-assisted PLL presented in [2], where the second-order loop filter of the FLL shares the same cascade of accumulators used by the PLL filter.

In the locked condition and are small enough to justify a linear analysis of the loop. The complete loop is seen as an equivalent PLL with filter coefficients , , and , instead of , , and . Thus, the FLL is inserted into the model of the PLL at a design stage. This eliminates the constrain of

using a narrow bandwidth FLL to not significantly perturb the PLL behavior, as in [2, 6]. A wide bandwidth FLL allows the loop to have two regions of operation: "phase-locked'' as it was described before, and "frequency-locked'' when the dynamics unlocks the PLL but the FLL keeps the frequency error within the linear range of its discriminator. In the latter region the loop is governed by the FLL (coefficients and) and the phase error input acts like a zero-mean perturbation [25]. As soon as the dynamics let the loop reduce its frequency error close to zero, the phase lock can be restored.

Conclusion:

This paper gives the research on the digital carrier tracking technology under large Doppler frequency shift. The known structure of FLL-assisted PLL, but with the fully digital conception in [5], led to a carrier loop that operates in phase locked condition normally, and in frequency locked condition if the dynamic becomes too severe. The effect of coupling the FLL to the PLL is considered at the design stage allowing a fine control of effective loop bandwidths. This method can\ accomplish high precision of the carrier tracking under large Doppler shift after the simulation. It can be used in the Rayleigh fading channel with large Doppler shift, thus possessing broad application prospect in the remote sensing and communication area. In conclusion, the PLL has been designed block by block and simulated using PSPICE. It has been shown that the initial design criterion is achieved by generating a clock signal at 120MHz using the reference signal of 200kHz.

References:

[1]   W. J. Hurd, J. I. Statman, and V. A. Vilnrotter, "High dynamic GPS receiver using maximum likelihood estimation and frequency tracking," IEEE Transactions on Aerospace and Electronic Systems, vol. 23, no. 4, pp. 425–437, 1987. View at Google Scholar · View at Scopus

[2]   P.W. Ward, "Performance comparisons between FLL, PLL and a novel FLL-assisted-PLL carrier tracking loop under RF interference conditions," in Proceedings of the 11th International Technical Meeting of The Satellite Division of The Institute of Navigation (ION GPS '98), Nashville, Tenn, USA, September 1998.

[3]   F. M. Gardner, Phaselock Techniques, John Wiley and Sons, New York, NY, USA, 1979.

[4]   C. R. Cahn, D. K. Leimer, C. L. Marsh, F. J. Huntowski, and G. D. Larue, "Software implementation of a PN spread spectrum receiver to accommodate dynamics," IEEE Transactions on Communications, vol. 25, no. 8, pp. 832–840, 1977. View at Google Scholar · View at Scopus

[5]   E. D. Kaplan and C. J. Hegarty, Understanding GPS: Principles and Applications, Artech House, Boston, Mass, USA, 2nd edition, 2006.

[6]   S. B. Son, I. K. Kim, S. H. Oh, S. H. Kim, and Y. B. Kim, "Commercial GPS receiver design for high dymanic launching vehicles," in Proceedings of the International Symposium on GNSS/GPS, Sydney, Australia, December 2004.

[7]   P. V. Brennan, "Performance of phase-locked loop frequency synthesiser using accumulative phase detector," IEE Proceedings

of Circuits, Devices and Systems, vol. 143, no. 5, pp. 249–254, 1996. View at Google Scholar

[8]   R. C. Den Dulk, "Digital fast acquisition method for phase-lock loops," Electronics Letters, vol. 24, no. 17, pp. 1079–1080, 1988. View at Google Scholar · View at Scopus

Authors Profile:

Mr. Mahender Gandikota ,Pursuing Mtech from

Arjun College Of Technology And Sciences,

Mount Opera Premises, Batasingaram, Ranga

Reddy Dist,Telangana, INDIA.

Miss P.Chandramani, i (M.Tech), Asst.Professor,

Arjun College Of Technology And Sciences,

Mount Opera Premises, Batasingaram, Ranga

Reddy Dist,Telangana, INDIA