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Reliable Low Power Multiplier Design Using Reduced Replica Redundancy Block

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Abstract-
We develop a new method for designing a reliable low power multiplier by using algorithmic noise tolerant tecnique. To propose the fixed width RPR to replace the full width RPR block in the ANT design. RPR is a reduced precision replica whose output is taken as the corrected output in case the original system computes error. It reduces the truncation error and then constructs a lower error fixed width Wallace tree multiplier. It is efficient for VLSI implementation. The ANT technique having high accurate, low power consumption and area efficiency. To design the fixed width RPR by using the partial product terms of input correction vector and minor input correction vector to reduce the errors.
Keywords- algorithmic noise tolerant(ANT); reduced precision replica(RPR); fixed width Multiplier

I.INTRODUCTION

The fast growth of portable and wireless computing systems in recent years drives the need for ultralow power systems. Low power consumption and smaller area are some of the most Important criteria in the DSP systems and high performance systems. The low power technique is the voltage overs caling (VOS), was proposed in lower supply voltage beyond critical supply voltage without sacrificing the throughput. A novel algorithmic noise tolerant (ANT) technique combined VOS main block with reduced precision replica (RPR), which combats soft errors effectively while achieving significant energy saving. VOS increase the delay in all paths of a system and may limit high performance required by today complex applications. ANT is the combined VOS block and RPR block, the error is occur. It is a very fast manner but hardware complexity is too difficult.

II. MULTIPLIER

Multipliers are key components of many high performance systems such as FIR filters, microprocessors, digital signal processors, etc. A system's performance is generally determined by the performance of the multiplier because the multiplier is generally the slowest element in the system.

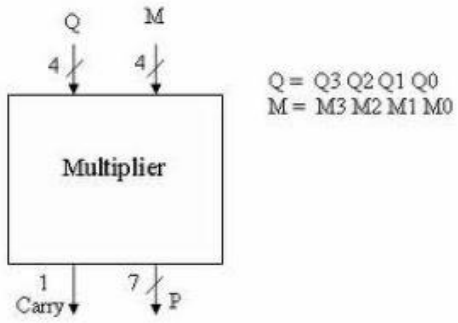

Figure 1. multiplier

The basic algorithm for multiplication of two binary numbers, M (multiplier) and N (multiplicand), makes use of the property of multiplication numbers.

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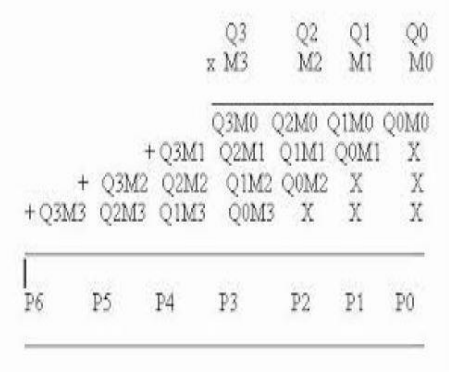

III. RELATED WORK

3.1. FIXED WIDTH MULTIPLIER

The fixed-width multipliers have been widely used in the design of digital signal processor(DSP) due to their smaller area and lower power dissipation. In order to reduce the chip area of channel detector for cognitive radio, many fixed width Booth multipliers have been used. However, they reduce the detection accuracy because of truncated partial products. This method can reduce the truncated error by using variable compensation value. The third categor y is hybrid error compensation, which uses both constant and adaptive QEC techniques together to reduce the truncated error. In order to overcome the disadvantages of has presented a method of dividing the truncated partial products into the major truncated section and the minor truncated section.

3.2. ALGORITHMIC NOISE TOLERANCE

The motivation is to reduce power of the traditional methods for noise tolerance. ANT can be mainly divided into Prediction based ANT and Reduced Precision Redundancy based ANT. Using ANT technique to improve the performance of DSP algorithms in presence of bit error rates. Therefore ANT can produce more effective signals. ANT to compensate for degradation in the system output due to errors from soft computations.

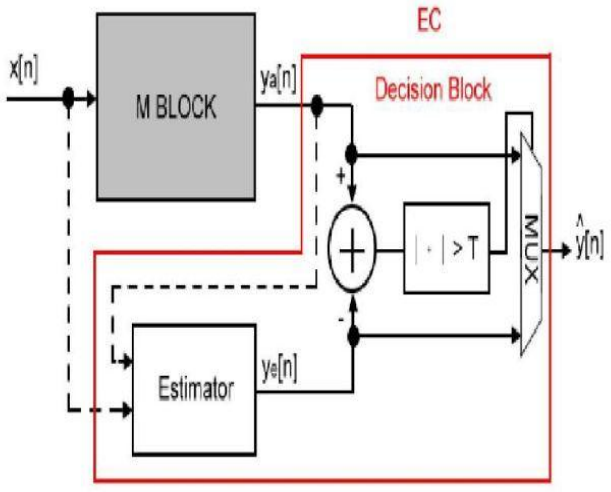

Figure2. algorithmic noise tolerance

3.3. REDUCED PRECISION REDUNDANCY

The MDSP block is subject to VOS, which results in soft errors in its output. When a soft error in MDSP is detected using an error control (EC) block, the RPR output is used as an output. Next, we describe the error characteristics of a system under VOS and then present the proposed error control algorithm.

3.4. SOFT ERROR CHARACTERISTICS

Voltage over scaling introduces input dependent soft errors whenever a path with delay greater than the sample period is excited. Since the arithmetic units employed in DSP systems are based on least significant bit (LSB) first computation, soft errors appear first in the most significant bits (MSBs), resulting in errors of large magnitude. These errors severely degrade the performance but are desirable because they are easy to detect. This fraction depends upon the delay distribution of a system, which in turn depends on the architecture. The path delay distribution for all possible input combinations of an 8× 8 Baugh Wooley multiplier.

IV THE RPR TECHNIQUE

4.1 PROPOSED SYSTEM ANT MULTIPLIER DESIGN USING FIXED WIDTH RPR

To proposed the fixed-width RPR to replace the full width RPR block in the ANT design which can

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not only provide higher computation precision, lower power consumption, and lower area overhead in RPR, but also perform with higher SNR, more area efficient, lower operating supply voltage, and lower power consumption in realizing the ANT architecture. To achieve more precise error compensation, we compensate the truncation error with variable correction value. We construct the error compensation circuit mainly using the product terms with the largest weight in half of the full- length one. However, truncation of LSB part results in rounding error, which needs to be compensated the least significant segment.

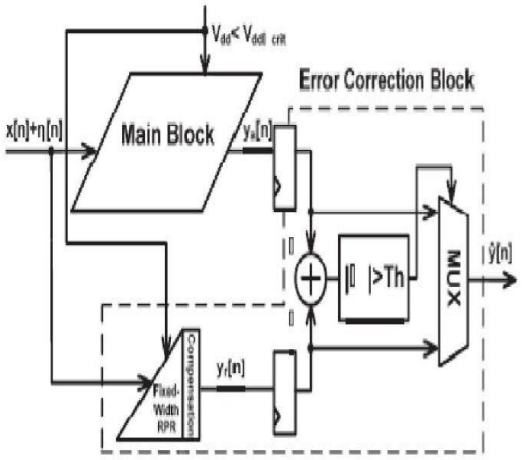

Figure 3. Proposed ant architecture with fixed width rpr

To save hardware complex complexity, the compensation vector in the partial product terms with the largest weight in the least significant segment is directly inject into the fixed-width RPR, which does not need extra compensation logic gates.

The fixed width designs are usually applied in DSP applications to avoid infinite growth of bit width. The hardware complexity and power consumption of a fixed-width DSP is usually about. As compared with the full-width RPR design in the proposed fixed-width RPR multiplier not only performs with higher SNR but also with lower circuitry area and lower power consumption. The error compensation algorithm makes use of probability, statistics ,and linear regression analysis to find the approximate compensation value.

4.2. PROPOSED PRECISE ERROR COMPENSATION VECTOR FOR FIXED WIDTH RPR DESIGN

In the ANT design, the function of RPR is to correct the errors occurring in the output of MDSP and maintain the SNR of whole system while lowering supply voltage. In the case of using fixed width RPR to realize ANT architecture, we not only lower circuit area and power consumption, but also accelerate the computation speed as compared with the conventional full length RPR. However, we need to compensate huge truncation error due to cutting off many hardware elements in the LSB part of MDSP. The source of errors generated in the fixed width RPR is dominated by the bit products of ICV since they have the largest weight.

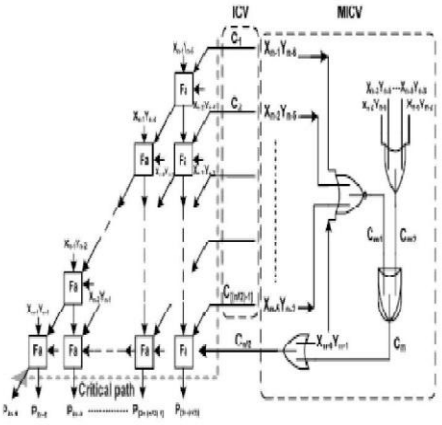

Figure 4 .proposed high-accuracy fixed-width rpr multiplier with compensation constructed by the multiple truncation ec vectors combined icv together with micv.

Before directly injecting the compensation vector β into the fixed width RPR, we go further to double check the weight for the partial product terms in ICV with the same partial product. Therefore, we apply the same weight of unity to each input correction vector element. This conclusion is beneficial for us to inject the compensation vector into the fixed width RPR directly. In this way, no extra compensation logic gates are needed for this part compensation and only wire connections are

needed. compensation vectors are constructed by ICV(β) It implies us that if we adopt the multiple compensation vectors for the average compensation error terms .we can lower the compensation error effectively and no additional compensation error will be generated.

V. CONCLUSION

A low error and area-efficient fixed width RPR based ANT multiplier design is implemented. Noise sources such as cosmic rays and alpha particles can impact the error control blocks as well. We have proposed novel algorithmic noise tolerant technique referred to as reduced precision redundancy(RPR) to combat errors in hardware. ANT is an elegant.

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