International Journal of Research (IJR)
e-ISSN: 2348-6848, p- ISSN: 2348-795X Volume 2, Issue 12, December 2015
Available at http://internationaljournalofresearch.org

A Fuzzy Based Control Strategy for a Cascaded Multi Level Converter

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ABSTRACT

In this paper, Fuzzy based pulse width modulation (PWM) technique specially designed for signle phase (or four wire three-phase) multilevel Cascaded H-Bridge Converters is presented. The main theme of the proposed technique is to reduce the DC-link voltage unbalance independently from the amplitude of the DC-link voltage reference compensate the switching device voltage drops and on-state resistances,and distorted currents in terms of THD. Such type of reduction can be used for increasing the quality of the waveform from the converter. This is widely used in high-power low supply voltage applications where low switching frequency is used. The DC-voltage balance capability of the method removes the requirement of additional control loops to actively balance the DC-link voltage on each H-bridge , simplifying the control strategy. The proposed Fuzzy Based Control strategy is verified in MATLAB/ simulink and results are presented .

Index terms—Multi level converters; Predictive control; and smart grid.

1.INTRODUCTION

The history multilevel converters begin in the mid-1970s, when the first describing a converter topology capable of producing multilevel voltage from various DC voltage sources was published (Baker Bannister, 1975) .The topology was achieved by connecting single phase converter in series .Fig.,1 shows an example of a circuit related to the topology presented by Baker and Bannister. The topology depicted in the figure is a series-connected H-bridge inverter (SCHBI), also known as cascaded H-bridge inverter.

In recent years multilevel converters have been identified as a favoured topology for high power applications as a result of advantages such as high levels of modularity, availability, overall efficiency, and high output waveform quality .this is achieved at the expense of increased number of components and control complexity [1]-[3]. In addition to this functionality ,when the dc side is connected to a set of batteries or other energy storage devices the multilevel converter can be used to maintain the charge balance of the energy storage system [4],[5].]. Multilevel converters have also been applied for power quality improvement and FACTS where, especially in aerospace applications, the reduced filtering requirement needed for multilevel converter represents an advantage in terms of total converter weight and cost [6]–[9]. In the coming years, multilevel converters are likely to be used increasingly in electrical power grids in order to achieve a higher flexibility and reliability and allow smart power management in the presence of different energy sources and utilities connected to the grid. Among all the possible multilevel converter topologies Cascaded H-Bridge converters (CHB) represent an interesting solution in several applications where its reduced number of components when compared to other multilevel converter topologies and high modularity are important features which lend themselves to the improvement of overall system efficiency and reliability. Even though three-phase converters are widely used in high power applications a single-phase configuration is largely employed in Photovoltaic inverters, traction application or in neutral-connected three-phase power distribution systems .

The main issues with the CHB converter is the requirement for isolated DC-Link voltages as well as the significant effect of device voltage drop and on-state resistance in applications with high number of levels and relatively low application ac side voltages.

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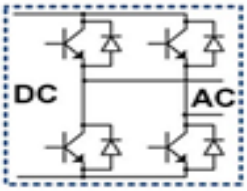
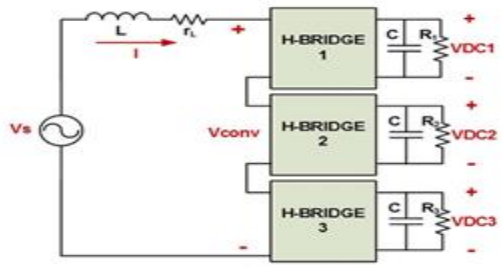
Furthermore, in the active rectifier configuration, balanced DC-Link voltages are required to achieve optimal operation considering a symmetrical (and therefore fully modular) configuration. DC-Link voltage balancing methods have been proposed in literature for CHB active rectifiers and they can be divided into two main groups depending on whether the DC-Link voltage balancing method is integrated in the controller, using additional control loops, or directly into the modulator. In this paper, the latter case is considered and a novel modulation technique, developed for single-phase systems and suitable for high power multilevel CHB converters, is introduced. The proposed modulation strategy is based on the Distributed Commutation Modulator (DCM), described in .DCM is a pulse width modulation (PWM) technique specifically designed for multilevel CHB converters. The aim of DCM is to minimize the commutation frequency of the individual devices, distributing these commutations evenly among the converter HB cells. As a result, the converter losses are equally distributed across the devices, increasing the converter reliability, without compromising the output voltage waveform quality.



(a)

Fig.1 (a) a Single HB Circuit (b) Schematic diagram of a 7-level CHB in a Active Rectifier Configuration



However, the balancing of the DC-Link voltages represents an issue for the DCM strategy as such a technique is able to passively balance the DC Link voltages only when balanced dc currents are demanded. Moreover, in the DCM technique, the devices voltage drops and on-state resistances are not considered. In order to overcome these issues, an active DC-Link voltage balancing algorithm has been designed for DCM which accounts for the device voltage drops and on-state resistances, improving the output voltage waveform quality and maintaining good performances even when unbalanced dc currents are demanded. In the concept of DC-Link voltage balancing algorithm is introduced as well as the device voltage drop and on-state resistance compensation. The main target of the proposed modulation strategy is, in contrast with DCM, to minimize the DC-Link voltage unbalance among the different converter cells in order to maintain the converter modularity and produce high quality waveforms, even if a low switching frequency is considered. Referring to Fig. 1, the DC-Link voltage affects the distribution of the commutations among the devices only for unbalanced loads, i.e., whenR1=R2=R3. When the loads are balanced, i.e., whenR1=R2=R3, the device commutations are equally distributed among the CHB cells. When compared to other DC-Link voltage balancing techniques, the proposed algorithm presents a very fast and accurate response, avoiding the use of additional control loops. The device voltage drops and on state resistances are also compensated, producing higher quality output voltage waveforms, in particular, in applications where a large number of CHB cells are used with a relatively low target ac side waveform magnitude, i.e., automotive applications. The proposed modulator is implemented on a single phase 7-level CHB, comprising three H-Bridges cells and described in Section II, which is widely used in Photovoltaic inverter or in neutral-connected three-phase power distribution systems. Details of the proposed modulation technique are provided in Section III, including examples of the operation of the proposed technique and a brief explanation of the DCM method. The obtained results are described in detail, highlighting the advantages and disadvantages of the proposed modulation

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technique. Simulation results are demonstrated for a single-phase 7-level converter in Section IV, while experimental results from low voltage testing on a laboratory prototype are presented in Section V.

TABLE I
POSSIBLE VOLTAGE LEVELS OF A 3-CELL CONVERTER

V_{CONV}	H-Bridges States
$+3V_{DC}$	(111)
$+2V_{DC}$	(110) (101) (011)
$+V_{DC}$	(100) (010) (001) (11-1) (1-11) (-111)
0	(000) (10-1) (-101) (1-10) (-110) (01-1) (0-11)
$-V_{DC}$	(-100) (0-10) (00-1) (-1-11) (-11-1) (1-1-1)
$-2V_{DC}$	(-1-10) (-10-1) (0-1-1)
$-3V_{DC}$	(-1-1-1)

II.CASCADED H-BRIDGE CONVERTERS

A single-phase configuration of an n-level H-bridge cascaded inverter is depicted in Fig. 2.1. Each separate dc source is connected to a single-phase full-bridge/or H-bridge, inverter. Each inverter can generate three different voltage level outputs, +V dc , 0, and –V dc by connecting the dc source to the ac output by different combinations of the four switches,S 1 , S 2 , S 3 , ands 4 . To obtain voltage level +V dc , switches S 1 and S 4 turned on, where as for voltage level –V dc switches S 2 and S 3 turned on. Zero level voltage can obtained by turning on switches 1 and S 2 ores 3 , and S 4 . AC outputs of each synthesized different full-bridge inverter levels are connected in series for summing up to generate multilevel voltage waveform. The number of outputphase voltage n-levels in a cascade inverter defined by n= 2l+1, wherel is the number Of separate DC sources. As example phase phase voltage waveform for n-level cascaded H-bridge inverter with (n-1)/2 seperate DC sources and (n-1)/2 full bridges. The output phase voltage generalised as v=va1+va2+va3+va4+va5+.....van

The main benefits and drawbacks of cascaded H-bridge multilevel converters are briefly summarized as follows:

Benefits:

* The number of possible output voltage levels are more than twice the number of dcsources (n = 2l+1).

* The series of H-bridges makes for modularized layout and packaging. Enable the manufacturing process to be done more fast and cheap.

Drawbacks:

* Separate dcsources required for each of the H-bridges and could generate oscillating dc source power.

In Fig. 1 the schematic diagram of a single-phase 7-level CHB converter, connected as an active rectifier, is shown. Although the proposed method is equally as effective in the inverter mode configuration, in order to test the capability of a DC-Link voltage balancing algorithm and avoid the necessity of isolated high voltage sources, the rectifier configuration is preferred. Referring to Fig. 1, the HBs are series-connected on the grid side and an inductive filter, with a parasitic resistance rL, is used to facilitate the required connection between the converter and the grid. Each HB cell is connected to a capacitor,C, and a resistor,R, used to represent the loading of the converter, which in reality could potentially be another converter, providing back-to-back operation, or a real load. For a symmetrical converter, the genericith cell is connected to a voltage source and can produce three voltage levels, indicated as−VDCi, 0 and +VDCi. These voltage levels are associated, respectively, to states−1, 0 and 1. As a consequence, an n-cell cascaded converter can produce2n+1voltage levels on the ac side. The output voltage VCONV is composed of seven different voltage levels which can be produced by one or more combinations of H-Bridge states, as indicated in Table I.

III.PROPOSED MODULATION TECHNIQUE

As stated in the introduction, the main goal of the proposed modulation method is to minimize DC-Link voltage imbalances and compensate the device voltage drops and onstate resistances. To achieve such a result, a fast response to any unbalance on the dc loads is required. For this reason the balancing algorithm is fully integrated into the modulation scheme, without using any additional controllers. It is important to note that since one of the targets of the proposed algorithm

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is to equalize the voltages on the capacitors, their average value is considered as the reference voltage for each DC-link capacitor in the algorithm, while the total DC-Link voltage is set to the reference value using a Proportional-Integral action external to the modulator. In order to reduce stress on the power switches and improve their reliability, the commutations are permitted only between adjacent voltage levels i.e., it is possible to switch only one leg of one H-Bridge cell during every sampling interval. The algorithm is modular and applicable to a genericn-level CHB converter; however increasing the number of voltage levels requires an obvious increase in computational effort.

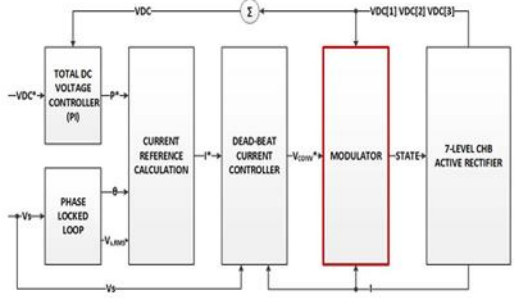

Fig. .2 Overall Control Scheme

A. Control Scheme

Fig. 2, shows the control block diagram implemented for the converter of Fig. 1, where VDC denotes the total DC-Link voltage andVDC∗ is the desired DC-Link voltage. A singlephase Phase-Locked-Loop (PLL) is used in the control scheme to obtain the supply phase angle, θ, and RMS value, Vs,RMS. The PLL scheme is obtained by cascading the orthogonal system generator proposed in [15], based on the Second Order Generalized Integrator, with the three-phase PLL presented in [16], based on a steady-state linear Kalman filter.

The line current is controlled in order to obtain the required DC-Link voltage; to achieve this goal, the current referenceI ∗ is calculated, at every sampling period Tsof the controller, as follows [17]:

$$I^*(t_k + iT_s) = \frac{P^*}{(V_{s,RMS}\sqrt{2})}\sin(\theta + iT_s), i = 1,2 \quad (1)$$

$$V^*_{CONV}(t_k + T_s) = V_s(t_k + T_s) \quad -\frac{L}{2T_s}[I^*(t_k + 2Ts{-}Itk{+}rLI{*}tk{+}Ts \quad (2)$$

The control output represents the desired converter voltage average value during the next sampling interval, applied using the proposed modulation scheme.

B. Distributed Commutation Modulator (DCM)

As mentioned in the introduction, the proposed technique can be seen as an improvement to the DCM technique [30], [31] where the commutations are distributed among the three H-Bridges in order to reduce the device switching frequency, and optimize the converter losses. Under normal operating conditions, the n converter cells are able to commutate sequentially so that each one can perform only one commutation every n sampling periods. Commutations are permitted only between adjacent voltage levels.

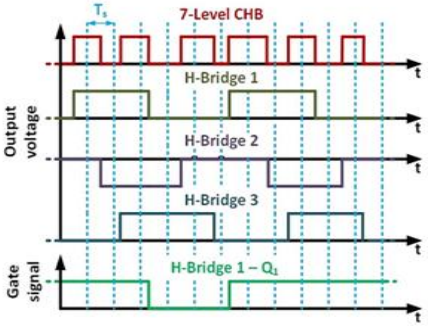

Fig.3 DCM Working Principle

As a consequence, the total switching frequency is half of the sampling frequency, while the device switching frequency of a single cell is approximately1/(n−1) for ann-level CHB. An example of normal operation is given in Fig. 4 where the 7-Level CHB of Fig. 1 is controlled in order to obtain a positive square waveform. As it is possible to see from the first waveform in Fig. 3, given a sampling frequency fs=1/Ts, the waveform produced by the 7 level CHB has a switching frequency fsw=fs. The H-Bridges are forced to commutate sequentially obtaining a switching frequency for a single H-Bridge of fswHB=fsw/3. Taking advantage of the zero vector redundancy, it is possible to obtain, for the device Q1 of the H-Bridge 1, a switching frequency equal tof Q1 sw =fswHB/2. Clearly this

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operation condition is not always feasible when a multi-level waveform is produced and the modulation algorithm attempts to distribute the commutations
among the devices. Two main issues have been identified using this technique. The DC-Link voltage balance is achieved with a symmetrical load on the three HBs and in any other case an additional control is required. The second issue appears in the case of high-power but relatively low voltage applications utilizing a large number of CHB cells, where the device voltage drops and on-state resistances can negatively affect the behavior of the modulator. An additional algorithm, described below, has been implemented to overcome these issues.

C. Device Voltage Drop and on-State Resistance Compensation

The device voltage drop and on-state resistance effect is compensated considering, instead of the measured DC-Link voltages, the effective voltages generated by the converter [43]. For each HB cell, three parasitic voltages, which are dependent on the current direction and amplitude, are defined as

$$V_0 = sign(I) * (V_d + V_q) - I * (R_d + R_q) \quad (3)$$

$$V_+ = -2 * (V_q + |I|R_q) \quad (4)$$

$$V_- = 2 * (V_d + |I|R_d). \quad (5)$$

In (3)–(5) the actual voltages generated by the converter are calculated on the basis of the diode and transistor voltage drops (Vd,Vq), the diode and transistor on state resistances(Rd,Rq), and on the current I flowing through the HB.

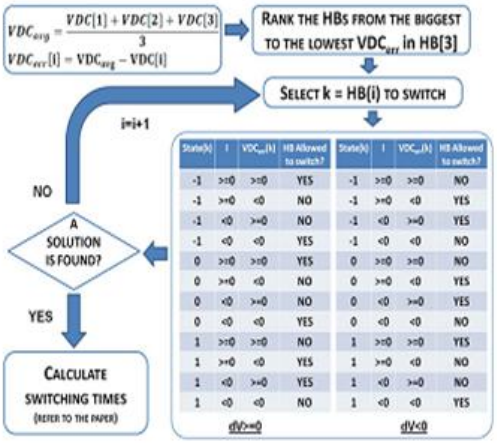

Fig.4 DC Voltage Balancing Principle

In particular, when a zero voltage state is applied, the voltageVDCef f produced at the output of theith cell is defined by the following equation:

$$VDCeff[i] = V_0. \quad (6)$$

On the other hand, in case of positive power flowing through the HB cell (applied voltage and ac current have the same sign) the transistor are on and generate the voltage defined by the following equation:

$$VDCeff[i] = VDC[i] + V_+. \quad (7)$$

Similarly, in case of negative power flow through the HB cell, the transistors are on and generate the voltage defined as follow:

$$VDCeff[i] = VDC[i] + V_-. \quad (8)$$

D. DC Link Voltage Balancing Algorithm

A simplified block diagram of the voltage balancing algorithm is presented in Fig. 4 for a 3-cell converter. The scheme is based on the application of iterative conditions in order to achieve the desired balance of the DC-Link voltages without losing the modularity of the algorithm.

The modulation algorithm begins with an update of the actual order of commutation of the 3 H-Bridges. From the measured DC-Link voltages on each capacitor,VDC[1],VDC[2], VDC[3], the average DC-Link voltage VDCavgis calculated as in (9) and considered as a reference value

$$VDC_{avg} = \frac{(VDC[1] + VDC[2] + VDC[3])}{3}. \quad (9)$$

Then, the DC-Link voltage errorVDCerr is calculated for every HB from

$$VDC_{err}[i] = VDC_{avg} - VDC[i]. \quad (10)$$

The switching order for the HBs is determined by the ranking, from the largest to the smallest, of the VDCerr absolute values. Supposing thatkth HB has been selected for the next switching, it is possible to calculate the normalized voltage error dv that has to be compensated by the selected HB as follows:

$$dv = \frac{V^* - \sum_{i \neq k} state(i) * VDCeff[i]}{VDCeff[k]}, \; state(k) \neq 0 \quad (11)$$

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$$dv = \frac{V^* + V_0 - \sum_{i \neq k} state(i) * VDCeff[i]}{VDC[k]}, \; state(k) = 0 \qquad (12)$$

WhereV ∗ is the voltage reference value andstate(i)the current state of the genericith HB. In other words, dvcorresponds to the normalized voltage that the selectedkth HB has to produce in the next sampling period on the basis of its current voltage level and the subsequent one. Under steady state operation usually|dv| <1; however it is possible, especially during fast transients of the voltage reference, that the absolute value ofdv becomes larger than 1. Before performing any commutation, the modulator checks if the selected kth HB is able to switch, considering its current state, and how the subsequent commutation will affect the DC-Link voltage balancing. The following three cases, valid fordv >0and referred to the selectedkth HB state, are possible.

1) State(k)=−1: the selected HB is not able to generate the required positive voltage with only one commutation, thus the error is reduced applying the 0 voltage level for the whole sampling period. The commutation is permitted only ifVDCerr[k] and the ac currentI have the same sign.

2) State(k)=0: the selected HB is able to generate the required positive voltage with only one commutation, thus the switching instant is calculated as in (13) or in (14), depending on the ac current sign

$$t_x = T_m \left[1 - \left(dv - \frac{V_+}{VDC[k]}\right)\right], \; I \leq 0 \qquad (13)$$

$$t_x = T_m \left[1 - \left(dv - \frac{V_-}{VDC[k]}\right)\right], \; I \geq 0. \qquad (14)$$

If dv >1, it is clear from (13) and (14) that tx<0. In this case tx=0is imposed. The commutation is permitted only ifVDCerr[k]and the ac currentIhave the same sign

3) State(k)=1: the selected HB is not able to not able to generate the required positive voltage. Whendv <1,the voltage error is reduced by applying the 0 voltage level at the switching instant calculated by (15)

$$t_x = T_m \left(dv - \frac{V_0}{VDC[k]}\right). \qquad (15)$$

The commutation is permitted only ifVDCerr[k]and the ac currentIhave different signs.

4) Otherwise: the modulator checks if another HB is able to switch to a higher voltage level without an increase the DC-Link voltage unbalance.

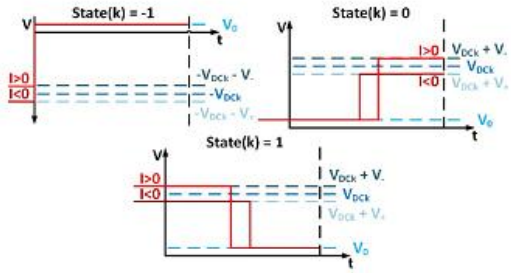

Fig. 5. Possible switching patterns for $0 < dv < 1$.

Fig. 5 a switching pattern example for a positive error is described. As described in (3)–(8) the actual voltage applied by the converter is related to the current sign. Depending on the previously applied state, it is possible to determine three cases for the new commutation where the sign of the current determines the switching instant, as described in (13)–(15). Clearly such a commutation is allowed only if it does not increase the DC-Link voltage error as described in section II-D.

In case ofdv <0, the following three cases for the selected kth HB state are possible.

1) State(k)=1: the selected HB is not able to generate the required negative voltage with only one commutation, thus the error is reduced applying the 0 voltage level for the whole sampling period. The commutation is permitted only ifVDCerr[k] and the ac currentI have different signs.

2) State(k)=0: the selected HB is able to generate the required negative voltage with only one commutation, thus the switching instant is calculated as follows:

$$t_x = T_m \left[1 + \left(dv - \frac{V_-}{VDC[k]}\right)\right], \; I \leq 0 \qquad (16)$$

$$t_x = T_m \left[1 + \left(dv - \frac{V_+}{VDC[k]}\right)\right], \; I \geq 0. \qquad (17)$$

Ifdv <−1, by considering (16) and (17) it is clear that tx<0. In this case tx=0is imposed. The commutation is permitted only ifVDCerr[k]and the ac currentIhave different signs.

3) State(k)=−1: the selected HB is not able to generate the required negative voltage. For the case where dv > −1, the voltage error is reduced

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applying the 0 voltage level at the switching instant calculated by (18)

$$t_x = -T_m \left(dv - \frac{V_0}{V\,DC[k]} \right). \qquad (18)$$

The commutation is permitted only ifVDCerr[k]and the ac currentIhave the same sign.

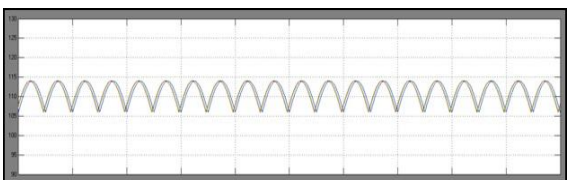
4) Otherwise: the modulator checks if another HB is able to switch to a higher voltage level without an increase the DC-Link voltage unbalance.

TABLE II
SIMULATION PARAMETERS

Symbol	Description	Value	Unit
V_d	Diode voltage drop	3	[V]
V_q	Transistor voltage drop	5	[V]
R_d	Diode on-state resistance	0.5	[mΩ]
R_q	Transistor on-state resistance	1	[mΩ]
r_L	Leakage resistance	1	[Ω]
L	Inductance	11	[mH]
C	Capacitance	3300	[μF]
R	Load resistance	20	[Ω]
f_s	Sampling frequency	2500	[Hz]

SIMULATION RESULTS

Simulations have been carried out in order to compare the performance of the proposed modulation strategy. The power rating of the converter considered in simulation match the power rating used in the experimental tests (3 kW). Operation in rectifier mode has been used to avoid the requirement of isolated high voltage sources. The proposed method, however, is equally as effective in the inverter mode configuration. A Dead-Beat current control, described in [23], [42], is used to impose the desired voltage reference. The complete control scheme is shown in Fig. 3 while the simulation parameters are shown in Table II. In order to highlight the effect of parasitic components, large values of Vd and Vq are considered during simulations. In this paper, the proposed modulator is compared with the DCM technique illustrated in [31].



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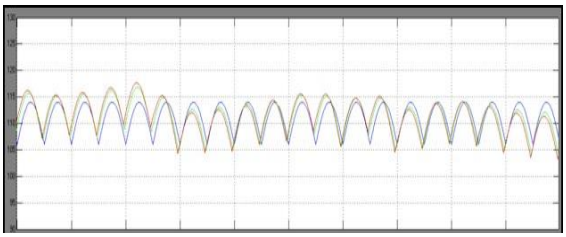

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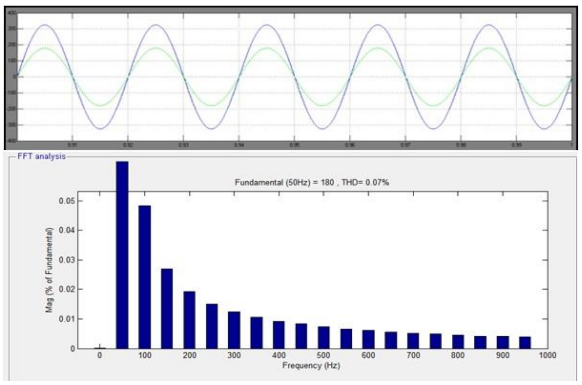

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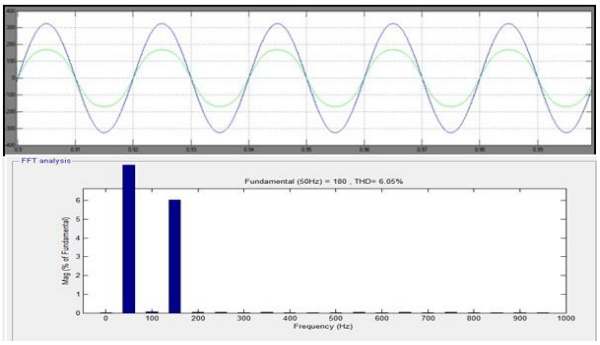

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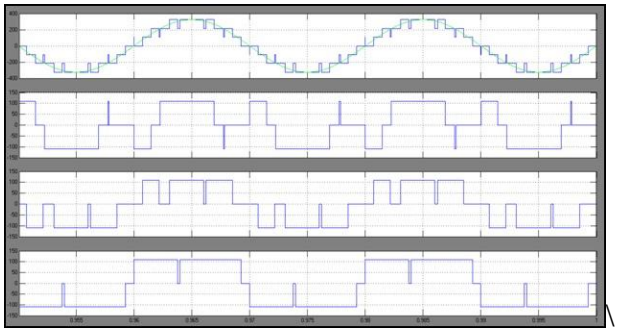

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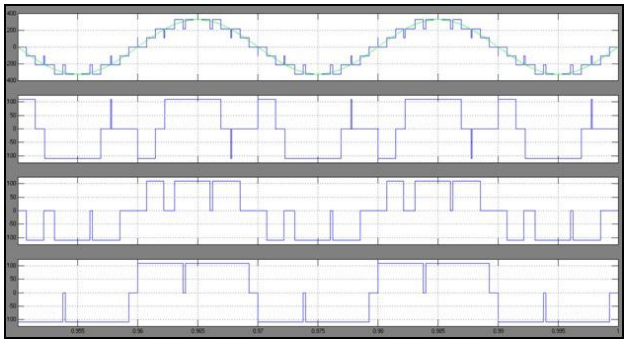
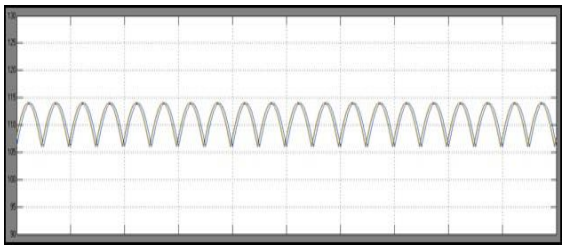


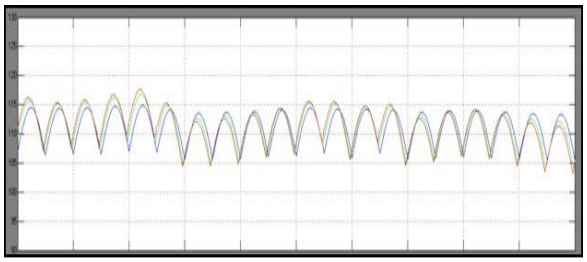
(f)

Fig. 6.2. (a), (c), (e) Simulation results with dc Link voltage balancing algorithm, devices voltage drops and on-state resistances compensation and

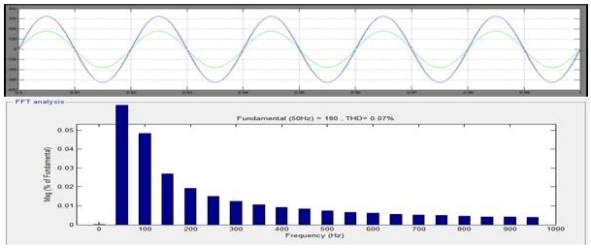
(b), (d), (f)DCM for balanced dc loads; DC-Link voltages; ac current and voltages; converter voltage and coverter voltage reference; single H-Bridges voltages



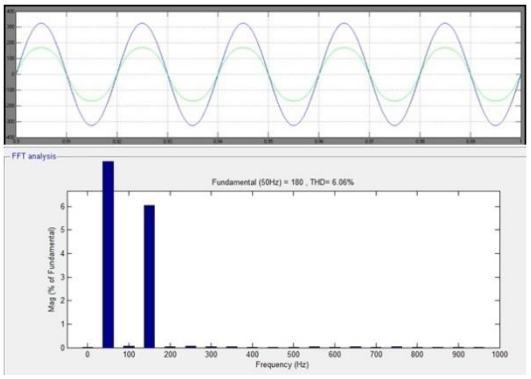
(a)



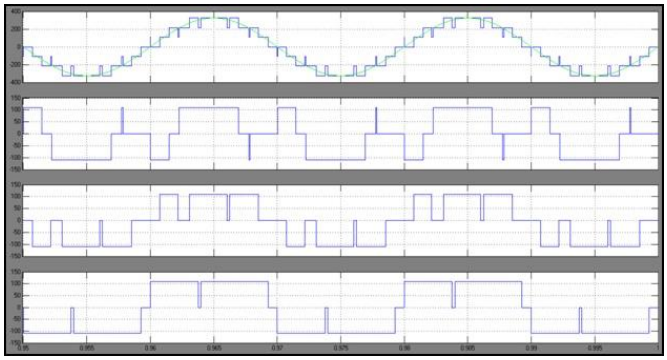
(b)



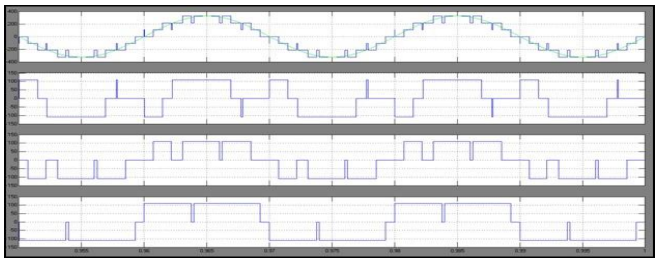
(c)



(d)



(e)



(f)

Fig.6.3 (a), (c), (e) Simulation results with dc Link voltage balancing algorithm, devices voltage drops and on-state resistances compensation and (b), (d), (f) DCM for unbalanced dc loads; DC-Link voltages; ac current and voltages; converter voltage and converter voltage reference; single H-Bridges voltages.

A comparison between the DCM technique and other well-known modulation techniques for CHB converters has already been carried out in [30]. In Fig. 6.2(a) and (b) it is possible to appreciate that the total DC-Link voltage is correctly regulated at the reference

International Journal of Research (IJR)
e-ISSN: 2348-6848, p- ISSN: 2348-795X Volume 2, Issue 12, December 2015
Available at http://internationaljournalofresearch.org

value with an optimal DC-Link voltage balance. However, with the proposed modulation strategy the DC-Link voltage oscillations are reduced, when compared to those observed with DCM. In Fig. 6.3 (c) and (d) the line current and the grid voltage are shown for a switching frequency of 1.25 kHz. For the proposed technique the current is correctly regulated with the required phase alignment between grid voltage and current. The proposed modulation strategy also produces a lower total harmonic distortion (THD) value, compared with DCM, due to the active compensation of device voltage drops and on-state resistances which reduces the line current distortion.

Fig. 6.2 (e) and (f) illustrate, for both techniques, the converter output voltage versus the converter voltage reference and the voltages produced by the single HBs. The commutations are equally distributed among the HBs for both modulation strategies. In order to appreciate the superior capability of the DC-Link voltage balancing of the proposed modulation strategy, three unbalanced dc loads of 10 Ω–20Ω–30Ω are implemented in the simulation. Such operating conditions frequently occur in solid state transformers [23] as well as in battery supplied inverters [36]. From Fig. 6.3 (a) and (b), which illustrate the DC-Link voltages, it is possible to observe that for the proposed modulation strategy the total DC-Link voltage is correctly regulated and the single DC-Link voltages are well balanced. When using the DCM technique under the same conditions, an unbalance of the DC-Link voltages is clear.

Experimental parameters for 3kw prototype

Symbol	Description	Value	Unit
V_d	Diode voltage drop	1.3	$[V]$
V_q	Transistor voltage drop	2.1	$[V]$
R_d	Diode on resistance	32	$[m\Omega]$
R_q	Transistor on resistance	52	$[m\Omega]$
r_L	Leakage resistance	0.5 t0 75	$[\Omega]$
L	inductance	11.15	$[mH]$
C	capacitance	33(k)	[□F]
R	Load resistance	variable	$[\Omega]$
f_s	Sampling frequency	25(k)	$[Hz]$

evident. In Fig. 6.3 (c) and (d) the line current and grid voltage are shown for a switching frequency of 1.25 kHz: using the proposed technique the current is correctly regulated with the required phase alignment between grid voltage and current. On the contrary, the DCM technique produces a significant distortion on the line current. The proposed modulation strategy clearly generates a lower THD value, compared with DCM. Fig. 6.3 (e) and (f) illustrate, for both techniques, the converter output voltage versus the converter voltage reference as well as the voltages produced by the single HBs. Using the proposed strategy the commutations are not evenly distributed among the HBs anymore. Conversely, using the DCM technique, the even commutation distribution is maintained but the significant harmonic content affects the Dead-Beat controller, producing a distorted voltage reference.

CONCLUSION:

PI, PD and PID controllers are conventional, most popular controllers and widely used in most power system appliances. But, in the recent times there are many researchers who reported and successfully adopted Fuzzy Logic Controller (FLC) termed as intelligent controllers to their appliances. A high-power H-_bridge converter with DCM techniques and Dc Voltage Balancing technique is proposed with Fuzzy logic controller .One stands to be with the DCM & the

other being the DC Voltage by Fuzzy Logic Controller (FLC) or the intelligence controller. Simpler layout of switches, reduced component count, and reduced capacitance requirement are among the best features of this scheme over the diode clamped and the cascaded multilevel converters.

In the proposed topology, minimize the unbalance of the DC link voltages, for any amplitude of the voltage reference, in order to obtain high quality waveforms while maintaining the modularity of the converter. In order to obtain a quick response to unbalance on the dc loads, the balancing algorithm is fully integrated into the modulation scheme without using any additional controllers. As a consequence, a high bandwidth response for the balancing algorithm is achieved even for extremely unbalanced load conditions. Moreover, device voltage drop and on-state resistance are compensated in order to extend the range of applications of the presented method to those cases where the parasitic effects of the devices may have a considerable effect, as for example automotive applications.

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