International Journal of Research (IJR)
e-ISSN: 2348-6848, p- ISSN: 2348-795X Volume 2, Issue 12, December 2015
Available at http://internationaljournalofresearch.org

A Hybrid Fuzzy Based Modular Multilevel Cascade Converters for Back-To-Back System without Dc-Link Capacitor

Kurri Rajasekhar Reddy & Mr.A.Suryanarayana Babu

[1]PG Scholar Nova College Of Engineering And Technology Jangareddy Gudem Department Of Electrical And Electronics Engineering ,JNTUK Andhra Pradesh, India.

[2]Nova College Of Engineering And Technology Jangareddy Gudem Department Of Electrical And Electronics Engineering ,JNTUK Andhra Pradesh, India

Abstract:

This paper presents a Hybrid-Fuzzy application of the modular multilevel cascade converter based on double-star chopper-cells (MMCC-DSCC) to a back-to-back (BTB) system for installation on power distribution systems. The DSCC is characterized by a cascade connection of multiple chopper-cells per leg, leading to flexible circuit design, low voltage steps, low EMI emission, and low harmonic voltage and current. The DSCC-based BTB system is equipped with neither dc capacitor nor voltage sensor on the common dc link. The paper designs, constructs, and tests a three-phase, 200-V, and 10-kW downscaled system to verify and justify its operating principles and performance. Experimental and simulated results agree well with each other, showing a promising possibility of the DSCC-based BTB system.

Keywords— Hybrid-Fuzzy; Asynchronous intertie; back-to-back (BTB) systems; grid-connected power converters; modular multilevel cascade converters (MMCCs)

I INTRODUCTION

THE modular multilevel cascade converter (MMCC) family consists of several members with different given names. These members have the common family name "MMCC" because they are characterized by cascade connections of either single-phase full-bridge (H-bridge) ac/dc converters called simply as "bridge-cells" or no isolated bidirectional dc/dc choppers called just as "chopper cells." These family members have different characters from a practical point of view [1]. Among them, attention has been paid to the specific family member with the given name, "double-star chopper cells (DSCCs)" for grid connections and motor drives. Although the full name is "MMCC-DSCC," this paper calls it simply as a "DSCC" for the sake of simplicity. The DSCC is the same in circuit configuration as a specific modular multilevel converter (MMC) presented in [2]–[4]. A difference exists in dc-link voltage between a long-distance DSCC-based HVDC system and a DSCC-based BT system. The HVDC system has, or will have, a dc-voltage range of 250 to 500 kV or higher to reduce the conducting power loss of overhead transmission lines and underground or undersea cables. On the other hand, the BTB system is more flexible in dc-link voltage design than the HVDC system because theft system can be considered as a "zero-meter-long" HVDC system. Therefore, it would be reasonable and acceptable forth BTB system to have a dc-link voltage as low as 66 kV or132 kV. Another difference exists in control strategy between the HVDC and BTB systems. It lies in whether "real-time communications" between the two DSCCs are available or not. Theft system can detect actual voltages and currents in the two DSCCs and can send the detected signals to a unified digital controller because the two DSCCs are installed at the same site. In other words, the two DSCCs can be considered as a single power conversion system with the unified digital controller. On the other hand, the HVDC system has a digital controller for each DSCC, in which the two digital controllers are operated independent of each other because one DSCC is too far away from the other to bring the unified digital controller to the HVDC system. In other words, the two DSCCs can be considered as two separate power conversion systems. As a result, the two DSCCs forming the BTB system can take the equal responsibility for regulating the dc-link voltage and controlling the dc-link current, whereas the two DSCCs forming the HVDC system should take different responsibilities [5]–[7]. Research scientists and engineers in power electronics and power systems have presented or published technical papers on DSCC-based

International Journal of Research (IJR)
e-ISSN: 2348-6848, p- ISSN: 2348-795X Volume 2, Issue 12, December 2015
Available at http://internationaljournalofresearch.org

power conversion systems with focus on control, modeling, analysis, design, and/or operation [2]–[18]. Some papers have included experimental waveforms obtained from single DSCC [8]–[12], [14]–[16]. However, neither paper nor article has disclosed actual waveforms obtained from a downscaled or commercially operating system consisting of two DSCCs connected back-to-back directly or with long cables. In addition, no careful comparison has been made among experiment, simulation, and analysis for the purpose of guaranteeing and enhancing their reliability.

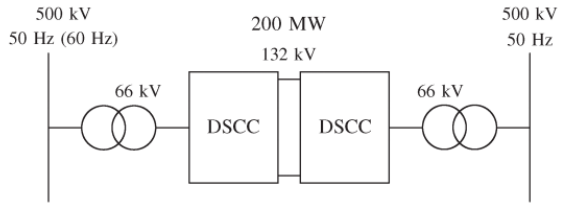


Fig. 1. Circuit configuration of the 200-MW DSCC-based BTB (FC) system.

This paper describes the design, construction, and evaluation of a three-phase 200-V, 10-kW, 50-Hz DSCC-based BT system without dc-link capacitor. The so-called "phase-shifted PWM" with the same triangular-carrier frequency as 450 His applied to the two DSCCs that are the same in circuit and control. Experimental waveforms obtained from the BT system are compared with simulated waveforms obtained from the software package "PSCAD/EMTDC" under the same operating conditions, circuit parameters, and control gains. Both waveforms agree well with each other not only in steady states but also in transient states. This means that both experiment and simulation are reliable enough to look into more practical systems and fault-ride-through (FRT) performance. Modeling and analysis are done for the single power conversion system unifying the two DSCCs that take the equal responsibility for regulating the dc-link voltage and controlling the dc-link current. A transient dc-link current to a small step change in the reference of active-power transfer from 8 to10 kW exhibits a first-order response with a time constant of about 0.9 ms in both experiment and simulation. This time constant agrees well with a theoretical time constant of 0.94 ms. Moreover, this paper presents experimental and simulated waveforms in another transient state, where it takes 20 ms (one cycle at the line frequency) to reverse power flow direction at

aerated power of 10 kW. Such an extremely fast response enables to enhance transient system stability as well as frequency regulation capability in some contingency situations. Finally, this paper presents experimental waveforms during a self-start from the initial state, and those during a self restart from the so-called "sleeping" or "gate-blocked" state in which two circuit breakers at both ac sides of the two DSCCs remain switched on, and all the power switching devices remain turned off.

II SYSTEM CONFIGURATION

High-power BTB and long-distance HVDC systems have the capability of executing asynchronous interties between two power transmission grids with the same line frequency as 50 Hz or 60 Hz. The aim of introducing the asynchronous intertie tithe two grids is to make bidirectional power-flow control independent of a phase difference between the sending grid voltage and the receiving grid voltage. When the line frequencies of the two grids are different, that is, 50 Hz and 60 Hz, the BT system is referred to as a frequency changer (FC). Fig. 1 shows a feasible circuit configuration of a Deceased BTB system for power transmission grids. The power capacity of the BTB system is rated at 200 MW. The secondary line-to-line voltage of each line-frequency transformers designed as 66 kV, and the dc-link voltage between the two DSCCs is set to 132 kV, as shown in Fig. 1. As an example, the BTB system is assumed to adopt the 6-kV GCTs (gate commutated thrusters) that are commercially available on the market, and the dc-capacitor reference voltage of each chopper cell is assumed to be 3 kV. When the count of chopper cells per leg results in88 (= 2×132kV/3kV), the BTB system has the following advantages.

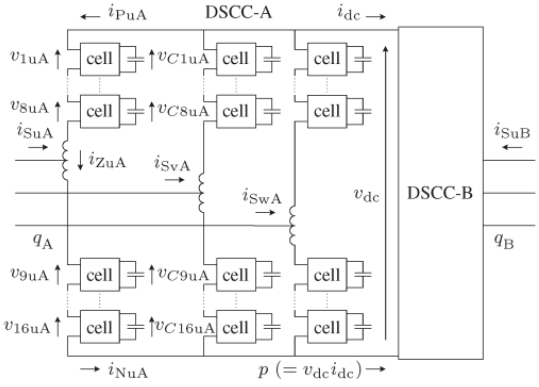
1) Each chopper cell is equipped with a floating dc capacitor and a dc voltage sensor, but without auxiliary dc-voltage balancing circuit or start-up circuit.
2) Since multilevel waveforms with low voltage steps can be considered almost sinusoidal, the line current gets purely sinusoidal at unity power factor or with any power factor controllable. As a result, the BTB system requires neither harmonic filter nor capacitor for power factor correction, unlike a conventional current-source BTB system using line-commutated thrusters.

International Journal of Research (IJR)
e-ISSN: 2348-6848, p- ISSN: 2348-795X Volume 2, Issue 12, December 2015
Available at http://internationaljournalofresearch.org

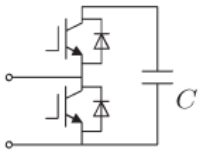
3) The sinusoidal voltage and current allow the BTB system to use a three-phase conventional and simple line frequency transformer for voltage matching and galvanic isolation between 500 kV and 66 kV.
4) No ac-link inductor is required because it can be replaced by the intentionally increased leakage inductance of the transformer.
5) No dc-link high-voltage capacitor is required between the two DSCCs because the floating dc capacitor of each chopper cell acts as an energy buffer. Therefore, neither additional cost nor volume is required for installing theca-link high-voltage capacitor.
6) No dc-link voltage sensor is required because an indirect feedback control loop makes it possible to indirectly regulate the mean dc-link voltage to its reference. This control loop is based on the signals obtained from the dc voltage sensors installed across the floating dc capacitors of all the chopper cells.

III CIRCUITCONFIGURATION

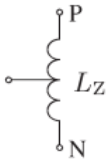
Fig. 2(a) shows the power circuit configuration of the Deceased BTB system with a per-leg chopper-cell count of 16.A couple of identical DSCCs, "DSCC-A" and "DSCC-B" are connected back-to-back without any common dc-link capacitor. Each DSCC consists of 48 chopper cells1depicted in Fig. 2(b), and three center-tapped inductors in Fig. 2(c). Here, LZ is not the inductance between the center tap and another node P or Nut the inductance between two nodes P and N. In Fig. 2(a), pica and inquire the positive and negative arm currents, i_{SuA} is the supply current, and i_{ZuA} is the circulating current



(a)



(b)



(c)

Fig 2Circuit configuration of the DSCC-based BTB system with 16 chopper cells per leg. (a) Main circuit. (b) Chopper cell. (c) Center-tapped inductor.

Along the u-phase leg of DSCC-A. Reference [8] has made the definition of i_{ZuA} as follows:

$$i_{ZuA} = \frac{1}{2}(i_{PuA} + i_{NuA}) \quad (1)$$

The count of independent variables out of the three branch currents i_{PuA}, inlay, and issue is not three but two because Kirchhoff's current law comes into existence at the u-phase a terminal of DSCC-A or at the center tap of the u-phase center tapped inductor. Following [8], this paper selects the supply current and the circulating current as two independent variables. As a result, the positive and negative arm currents are expressed as dependent variables as follows:

$$i_{PuA} = -\frac{i_{SuA}}{2} + i_{ZuA} \quad (2)$$

$$i_{NuA} = \frac{i_{SuA}}{2} + i_{ZuA} \quad (3)$$

The first terms of the right-hand sides in (2) and (3) are related to the supply current. They are out of phase by 180◦witheach other. As a result, the magnetic fluxes formed by the supply current cancel out each other inside the magnetic core of the center-tapped inductor. Therefore, the inductor presents no inductance to the supply current, whereas it renders the inductance LZ to the circulating current. Connected in parallel to make this experimental system effective as a downscaled BTB system. Fig. 3 shows the overview of the three-phase 200-V, 10-kW, and 50-Hz BTB system designed, constructed, and tested. Each a terminal of the two DSCCs is connected to the secondary side of a line-frequency transformer through an ac-link inductor Lac and a starting circuit. Each of the two line-frequency transformers with unity turns ratio is rated at 200 V, 15 kava, and 50 Hz. The leakage inductance of each transformer is much smaller tanoak, thus resulting in

International Journal of Research (IJR)
e-ISSN: 2348-6848, p- ISSN: 2348-795X Volume 2, Issue 12, December 2015
Available at http://internationaljournalofresearch.org

neglecting the effect of the leakage inductance. Each arm of the chopper cell consists of four power MOSFETs. The positive directions of idc and p are defined as the direction from DSCC-A to DSCC-B (left to right), as shown in Fig. 3.Moreover, qA and qB are three-phase instantaneous reactive (imaginary) powers with an engineering unit of [via] 2[19], [20] at the secondary sides of the two transformers. The values of qA and qB are defined as the positive (or negative) value when the DSCC acts as an inductor (or a capacitor).

Fig. 4 is a photo of the three-phase 200-V, 10-kW, and 50-HzBTB system designed and constructed for experiment.

Table I summarizes the circuit parameters of Figs. 2 and 3, which are used in experiment and simulation. Each DSCC has16 chopper cells per leg. The dc reference voltage of each floating capacitor is set tov∗C=50V, so that the dc-link reference voltage should be set tov∗dc= 400V because of the existence of (21) in Section V-B. The reason why the BT system adopts the phase-shifted PWM technique presented in [8] will be described in Section IV-A. Each triangular-carrier frequency is set aft= 450Hz, and a dead or blanking times 8μs. Note that 16 triangular-carrier signals phase-shifted one another by22.5◦ (= 360◦/16).

As described in Section II, the practical DSCC-based BT system rated at 200 MW has 88 chopper cells per leg. However, it would be unreasonable to construct a downscaled Deceased BTB system with a per-leg chopper-cell count of 88 forth purpose of confirming the reliability of experiment, simulation, and analysis. Therefore, the authors have intentionally increased each triangular-carrier frequency of the downscaled system to 450 Hz (slightly higher than that of the practical system), instead of decreasing the cascade count to 16. As result, the downscaled system is almost the same in equivalent triangular-carrier frequency as the practical system. Three phase nominal line-to-line rams voltages of 66 kV and 200 V in the practical and downscaled systems are typical high-voltage transmission and low-voltage distribution voltages in Japan, respectively.

The unit capacitance constant of the dc capacitors in Table I, His defined by

$$H_c = \frac{3nCV_c^2}{2P} \qquad (4)$$

The energy stored in all the dc capacitors, to which the rated voltage is applied, is divided by the rated power of the converter [21]. An SI unit offices [J]/ [W] = [s]. The unit capacitance constant is useful and effective in designing dc capacitors and in comparing dc capacitors in one BTB system to another one with different voltage and current ratings. The reason is that the unit capacitance constant can be considered as a kind of per-unit value although per-unit values have no physical unit.

IV CONTROLSYSTEM

A. Phase-Shifted PWM Technique

A few different PWM techniques to create multilevel voltage waveforms would be applicable to a DSCC-based BTB system from a theoretical point of view [8], [22]–[25]. Among them,

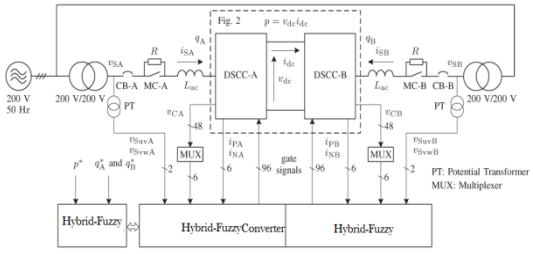


Fig. 3. Overview of the three-phase 200-V, 10-kW, and 50-Hz downscaled BTB system with a unified digital controller.

TABLE I
CIRCUIT PARAMETERS OF FIGS. 2 AND 3

Rated power	P	10kw
Nominal line to line rms voltage	V_s	200v
Nominal line frequency	f_s	50Hz
Per-leg chopper cell count	n	16
Ac link inductor	L_{ac}	2mH (16%)
Center-tapped inductor	L_Z	3mH (24%)
Starting resistor	R	20
DC-link reference voltage	V_{dC}^*	400v
DC-capacitance reference voltage	V_C^*	50v
Dc capacitor	C	6.6mF

International Journal of Research (IJR)
e-ISSN: 2348-6848, p- ISSN: 2348-795X Volume 2, Issue 12, December 2015
Available at http://internationaljournalofresearch.org

Unit capacitance constant	H_c	40ms at 50v
PWM carrier frequency	f_c	450Hz
Equivalent carrier frequency	nf_c	7.2kHz
Dead or blanking time		8μs

On three-phase, 200v, 10kw, 50Hz base

The paper prefer a phase-shifted PWM technique presented in [8] to the others. The reason is that these of the phase-shifted technique makes the actual switching frequency of each chopper cell exactly equal the triangular carrier frequency of the controller in the BTB system, independent of operating conditions, modulation indices, and tolerances of circuit components and parameters. This results in producing equal switching and conduction power losses in the individual chopper cells, making it simple and easy to design the heat-sink and/or cooling equipment of actual chopper cells. The phase-shifted PWM technique does not require the capacitor-voltage sorting and chopper-cell selecting processes presented in [2] but require the individual reference voltages of all the chopper cells for the individual balancing control inspection IV-C.

A. Three Sub controls

The control system for the DSCC-based BTB system shown in Figs. 2 and 3 can be classified into the following three sub controls based on feedback control:

1) Control of the active power and the reactive powers qA and qB at the secondary sides of the two transformers;

2) Control of the dc-link voltage and current (active power p, at the dc link);

3) Voltage control of all the floating dc capacitors. The power control is achieved on the−q synchronous reference frames in combination with decoupled current control [26]. The dc-link voltage and current control will be described in Section V.

C. Voltage Control of All the DC Capacitors

The voltage control of all the floating dc capacitors is characterized by hierarchical control consisting of three layers [26].It is classified into the following three blocks:

1) Overall capacitor-voltage control;

2) arm-balancing control;

3) Individual balancing control.

The overall capacitor-voltage control in the top layer takes the responsibility for regulating the arithmetical

average voltage of all the dc capacitors to its reference. Adjusting a small amount of active power supplied from the ac mains makes it

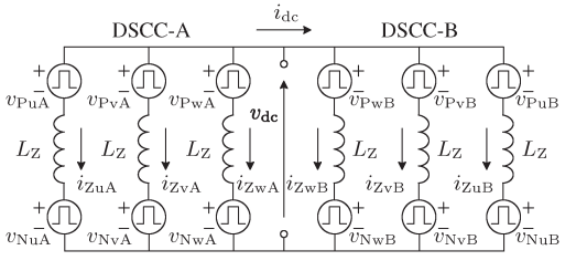


Fig. 5. Equivalent circuit for the DSCC-based BTB system in Fig. 2 with focus on the dc-link voltage and current.

Possible to regulate the arithmetical average voltage of all the capacitors to its reference. Note that the adjusted active power corresponds to the whole power loss of the two DSCCs. This control results in producing a slight difference in active power between each ac side and the dc link.

The arm-balancing control in the middle layer plays an important role in balancing 12 arithmetical average voltages, each of which is the arithmetical average voltage of eight dc capacitors per arm. The dc component of the circulating current in each leg is adjusted to exchange a small amount of active power active-power difference between the positive and negative arms. This sophisticated controls the same in function as the cluster-balancing control used inane SSBC (single-star bridge cells)-based STATCOM [27] and to the clustered SOC (state of charge)-balancing control used in an SSBC-based battery energy storage system (BESS) [28].However, the following essential difference exists: No circulating current flows in the SSBC whereas the circulating currents flowing in the DSCC can be controlled independently [1]. The

International Journal of Research (IJR)
e-ISSN: 2348-6848, p- ISSN: 2348-795X Volume 2, Issue 12, December 2015
Available at http://internationaljournalofresearch.org

individual balancing control in the bottom layer takes charge of regulating each dc-capacitor voltage to the arithmetical average voltage of eight dc capacitors per arm. This straightforward control adjusts the active power formed byte low-voltage-side voltage of each chopper cell and the arm current. The combination of the phase-shifted PWM technique with the voltage control of all the dc capacitors imposes no limitation on the number of cascaded chopper cells per leg theoretically.

V CONTROL OFDC-LINK VOLTAGE ANDCURRENT

This section provides an exclusive discussion on the dc-link voltage and current control, considering the two DSCCs as a unified power conversion system.

A. Equivalent Circuit and Basic Equations

Fig. 5 depicts an equivalent circuit for the DSCC-based BT system shown in Fig. 2, with focus on the dc-link voltage and current. A couple of three-phase ac circuits at the ac sides of the two DSCCs are removed from the equivalent circuit. The reasons are summarized as follows:

1) The supply current in each phase iS produces no effect on the voltage appearing between nodes P and N in the center-tapped inductor. This means that no magnetic flux is generated by the supply current because of the occurrence of cancellation as evident from (2) and (3), although a magnetic flux is generated by the circulating current.

2) The supply current in each phase produces no effect on the dc-link current because no zero-sequence current exists in a set of three-phase supply currents.

3) The chopped voltage at the low-voltage side of each chopper cell is determined by the duty factor and dc capacitor voltage of each chopper cell.

In addition, the stray inductance and resistance existing in each leg are neglected, and each center-tapped inductor is assumed as an ideal one without magnetic saturation or winding resistance.

Each arm of the two DSCCs in Fig. 2(a) is represented by the voltage source corresponding to the sum of the low-voltage-side voltages of the cascaded chopper cells per arm. For example,

The u-phase "collective" positive-arm and negative-arm voltages in DSCC-A, v_{puA} and v_{NuA}, are given by

$$v_{puA} = \sum_{j=1}^{\frac{n}{2}} v_{juA} \qquad (5)$$

$$v_{puA} = \sum_{j=1+n/2}^{n} v_{juA} \qquad (6)$$

Where in the count of the chopper cells per leg. The following relation exists between the dc-link current and the circulating currents:

$$i_{dc} = -\sum_{x=u,v,w} i_{ZxA} = \sum_{x=u,v,w} i_{ZxB} \qquad (7)$$

The u-phase collective leg voltage v_{PNuA} is given by

$$v_{PNuA} = \sum_{j=1}^{n} v_{juA} = v_{NuA} + v_{NuA} \qquad (8)$$

Kirchhoff's voltage law is applicable to each leg, thus leading to the following equation:

$$v_{dc} = v_{PNuA} + L_Z \frac{d}{dt} i_{ZuA} \qquad (9)$$

Equations similar to (9) are valid for the other five legs. The following equations are obtained by adding the right-hand and left-hand sides of the equations related to all the three legs in the individual DSCCs and manipulating the resultant equations, along with (7)

$$v_{dc} = \frac{1}{3} \sum_{x=u,v,w} v_{PNxA} - \frac{1}{3} L_Z \frac{d}{dt} i_{dc} \qquad (10)$$

$$v_{dc} = \frac{1}{3} \sum_{x=u,v,w} v_{PNxB} + \frac{1}{3} L_Z \frac{d}{dt} i_{dc} \qquad (11)$$

From (10) and (11), v_{dc} and i_{dc} are given by

$$v_{dc} = \frac{1}{6} \sum_{x=u,v,w} (v_{PNxA} + v_{PNxB}) \qquad (12)$$

$$\frac{d}{dt} i_{dc} = \frac{1}{2L_Z} \sum_{x=u,v,w} (v_{PNxA} - v_{PNxB}) \qquad (13)$$

Equation (12) means that v_{dc} is independent of L_Z, and that v_{dc} is equal to the arithmetical average of the six low-voltage side collective leg voltages in the BTB system. Equation (13) indicates that dice can be

International Journal of Research (IJR)
e-ISSN: 2348-6848, p- ISSN: 2348-795X Volume 2, Issue 12, December 2015
Available at http://internationaljournalofresearch.org

controlled by the voltage difference between the sum of the three collective leg voltages in DSCC-A and that in DSCC-B.

B. Control of DC-Link Voltage

Attention is paid to the u-phase leg in DSCC-A because of circuit symmetry in the three-phase circuit. The reference voltage at the low-voltage side of each chopper cell, v_{juA}^{*} can be divided into the following three terms:

$$v_{juA}^{*} = v_{juA}^{*}(ac) + v_{ju\,A}^{*}(dc) + v_{ZuA}^{*} \quad (14)$$

Here, v_{juA}^{*}(ac) is the ac (50-Hz) reference voltage; v_{juA}^{*}(dc) is the dc reference voltage, andv_{ZuA}^{*} is the control voltage of theca circulating current. Since the ac reference voltages in the positive arm are out of phase by 180◦with those in the negative arm, the following equation exists in $v_{juA}^{*}(ac)$:

$$\sum_{j=1}^{n} v_{juA}^{*}(ac) = 0 \quad (15)$$

Out of the three terms at the left-hand side of (14), $v_{juA}^{*}(ac)$ cannot be used to regulate the dc-link voltage or to control the dc-link current because it is the ac-terminal line-to-neutral reference voltage and devotes itself to controlling the supply current. On the other hand, $v_{juA}^{*}(dc)$can be used to regulate theca-link voltage, as described in this subsection, while v_{ZuA}^{*} can be used to control the dc-link current, as discussed in the next subsection.

Equation (12) indicates that the following relation should exist between the references of the u-phase collective leg voltage, v_{PNuA}^{*} and the reference of the dc-link voltage, Vedic:

$$v_{PNuA}^{*} = v_{dc}^{*} \quad (16)$$

Hence, the dc reference voltage at the low-voltage side of each chopper cell, v_{juA}^{*} (dc) is given by

$$v_{juA}^{*}(dc) = \frac{v_{dc}^{*}}{n} \quad (17)$$

When v_{ZuA}^{*} = 0, the use of (5), (6), (8), and (14) together with (15) yields the following relation:

$$v_{PNuA}^{*} = \sum_{j=1}^{n} v_{juA}^{*}(dc) \quad (18)$$

The arithmetical average voltage of the96 (= 16×6) dc capacitors in the BTB system, v_C is given by

$$v_C = \frac{1}{6n} \sum_{x=u,v,w} \sum_{j=1}^{n} (v_{CjxA} + v_{CjxB}). \quad (19)$$

Note that v_C does not contain the fundamental and second order harmonics because these harmonic components are cancelled out in each three-phase DSCC. The overall capacitor voltage control [26] adjusts the active powers delivered from the three-phase ac-mains voltages v_{SA} and v_{SB} to DSCC-An ands-B so that $v_C$follows its reference V_C^{*}. The application of the decoupled control presented in [26] to the control system can avoid mutual interferences among the supply currents, theca current, the circulating currents, and the mean dc voltages of all the floating dc capacitors.

Since$v_{juA}^{*}(dc)$ is considered as a dc-biased voltage to $v_{juA}^{*}(ac)$, (17) can be slightly modified into

$$v_{juA}^{*}(dc) = \frac{v_C}{2} \quad (20)$$

This equation relates the actual or detected high-voltage-side voltages of all the chopper cells in (19) to the actual clink voltage in (12), through the low-voltage-side dc reference voltages in (18). Then, taking (17) and (20) into consideration, the voltage reference of each dc capacitor, V_C^{*} should be set as follows:

$$V_C^{*} = \frac{2V_{dC}^{*}}{n} \quad (21)$$

The same equation as (21) exists in the other five legs. The detected and calculated dc voltage given by (19), vices regulated to its reference Vicky means of feedback control. As result, the dc-link voltage v_{dc} can be indirectly regulated to its reference V_{dC}^{*} without sensing the dc-link voltage as long as (20) is satisfied.3

In addition, the following advantage exists in the dc-link voltage control: The two DSCCs take the equal responsibility for regulating the dc-link voltage to its reference. To do it, each DSCC uses the common arithmetical-average voltage given by (19). Note that

International Journal of Research (IJR)
e-ISSN: 2348-6848, p- ISSN: 2348-795X Volume 2, Issue 12, December 2015
Available at http://internationaljournalofresearch.org

the average voltage is obtained from the two DSCCs with real-time communications.

C. Control of DC-Link Current

Controlling the dc-link current i_{dC} can is realized by controlling the circulating current flowing inside each

leg. The reference of the dc-link current, i_{dc}^{*} is given by

$$i_{dc}^{*} = \frac{p^{*}}{nvc/2} \qquad (22)$$

Here, p^{*} is the reference active power flowing from DSCCA to DSCC-B. The value of $\frac{nvc}{2}$ means the calculated clink voltage corresponding to the actual one. Similar to theca-link voltage control, this active power control does not require the actual dc-link voltage, and each DSCC uses the common arithmetical-average voltage given by (19). Because of circuit symmetry, the u-phase reference circulating currents in DSCC-A and DSCC-B, i_{ZuA}^{*} and i_{ZuB}^{*} are assumed to be

$$i_{ZuA}^{*} = -i_{ZuB}^{*} = -\frac{i_{dc}^{*}}{3} \qquad (23)$$

Equations similar to (23) are valid for the other v-phase and w-phase.

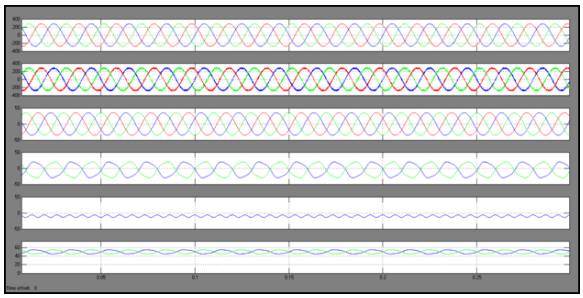


Fig.6. Experimental waveforms operating as a rectifier at p^{*}= 8.7 kW and q_{A}^{*} =−5.0 kvai.

The following control voltage ∗Zia plays the leading role in constituting feedback control of the dc circulating current:

$$v_{ZuA}^{*} = -\frac{K_Z}{n}(i_{ZuA}^{*} - i_{ZuA}) \qquad (24)$$

Where K_Z is the feedback gain. From (8), (14), (15) and (17), the reference of the u-phase collective leg voltage, v_{PNuA}^{*} is given by

$$v_{PNuA}^{*} = v_{dc}^{*} + nv_{ZuA}^{*} \qquad (25)$$

$$\sum_{x=u,v,w} v_{ZxA}^{*} = -\sum_{x=u,v,w} v_{ZxB}^{*} = \frac{K_Z}{n}(i_{dc}^{*} - i_{dC}) \quad (26)$$

Equations similar to (24) and (25) are valid for the other five legs. Note that the six reference circulating currents, included in (24) and its similar five equations, meet Kirchhoff's current law because of the existence of (23). Moreover, it is clear that the six actual circulating currents also meet Kirchhoff's current law. Equations (7) and (23) make it possible to change the control Voltage given by (24) into

$$\frac{d}{dt}i_{dC} = \frac{n}{2L_Z}\sum_{x=u,v,w}(v_{ZxA}^{*} - v_{ZxB}^{*}) = \frac{K_Z}{L_Z}(i_{dc}^{*} - i_{dC}) \qquad (27)$$

A differential equation similar to (27) is valid for the circulating current in each leg. The two DSCCs take the equal responsibility for controlling the dc-link current to its reference. Equation (27) leads to the following conclusions.

1) the actual dc-link current i_{dC} exhibits a first-order response to a step change in its reference i_{dc}^{*} with a time constant owls/KZ.

2) Controlling i_{dC} is independent of regulating vice.

D. Maximum DC-Link Ripple Voltage

This subsection assumes that the mean dc voltage of each chopper-cell capacitor is regulated toucan that the ac components of each capacitor are neglected. The use of a phase-shifted PWM technique makes voltage steps of v_{PuA} and v_{NuA} equal V∗C [10]. As a result, the instantaneous value of v_{PNuA} takes one out of v_{dc}^{*}, $v_{dc}^{*}+v_{c}^{*}$, and $v_{dc}^{*}-v_{c}^{*}$. This is valid for the other five legs. Equation (12), therefore, gives the following relation:

$$v_{dc}^{*} - v_{c}^{*} \le v_{dC} \le v_{dc}^{*} + v_{c}^{*} \qquad (28)$$

Theoretically, the possible maximum ripples voltage appearing across the dc link is2V∗Cin peak-to-peak.

International Journal of Research (IJR)
e-ISSN: 2348-6848, p- ISSN: 2348-795X Volume 2, Issue 12, December 2015
Available at http://internationaljournalofresearch.org

Actually, the maximum ripple voltage would be lower than, or equal to, 2V∗C.

VI SIMULATION RESULTS

A. UNIFIED DIGITAL CONTROLLER AND SIMULATION TOOL

Fig. 3 shows the overview of a unified fully digital controller based on a DSP and two FPGAs. The unified digital controller takes in a total of 112 voltage/current signals detected, and sends out 192 gate signals to the gate-drive circuits of the power MOSFETs. The experimental waveforms were taken by

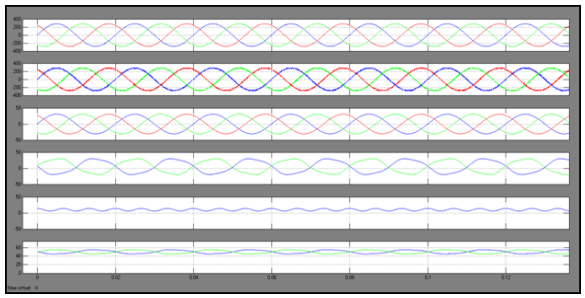


Fig.7. Experimental waveforms operating as an inverter at p^*=8.7kW and q_B^*=5.0kvai.

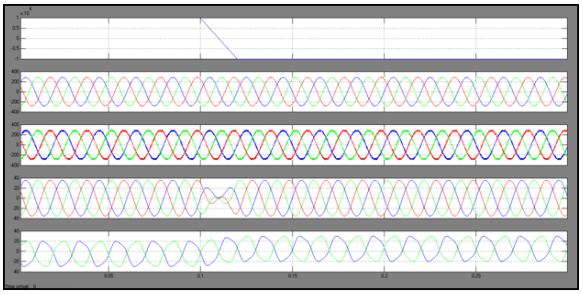
Using a personal computer via the PC-based data acquisition system, "Yokogawa WE7000." The sampling frequency is set to100 kHz.
The software package, "PSCAD/EMTDC" is used for simulation. All the circuit parameters and control gains used in the simulation are the same as those used in the experiment.
Moreover, the following items are considered:
1) A delay time of140μs (= 1/ (450 Hz×16)), which is inherent in the digital control system;
2) A dead or blanking time of 8μs;
3) Each chopper cell using ideal power switches.

B. OPERATING PERFORMANCE UNDER STEADY STATES

Figs. 6 and 7 show the experimental and simulated waveforms in which DSCC-An acts as a rectifier. Similarly, Figs. 8 and 9 are the waveforms in which DSCC-B acts as an inverter. The active-power reference is set top∗=8.7kW, and there active-power references are set to q_A^*=−5.0kvai for DSCCA and q_B^*=5.0kvai for DSCC-B. The apparent power results in 10 kava for both DSCCs. Each supply current in DSCC-A leads the corresponding supply line-to-neutral voltage by 30◦, whereas each supply current in DSCC-B lags the corresponding supply line-to neutral voltage by 150◦. This means that each supply current indict-A is in phase with the corresponding supply line-to-line voltage (e.g., i_{SuA} and v_{SuVA}). On the other hand, each supply current in DSCC-B is out of phase against the corresponding supply line-to-line voltage by 180◦ (e.g., i_{SuB} and v_{SuVB}). The ac terminal line-to-line voltage vuv is a multilevel PWM waveform containing much less harmonic voltage than that of a traditional two-level voltage-source PWM converter. As each triangular-carrier frequency is face= 450Hz, the equivalent carrier frequency is as high as7.2kHz (= 450Hz×16).The waveform of i_{Su} looks purely sinusoidal because its total harmonic distortion (THD) is less than 1.0%. The arm currents i_{pu} and i_{Nu} contain not only dc and 50-Hz components but also a 100-Hz component originated from the dc-capacitor voltage fluctuation and a 3.6-kHz (= 450Hz×8) switching-ripple component. However, the 100-Hz and 3.6-kHz ripple currents disappear from the waveform of fish because these currents circulate inside the two DSCCs. The dc current included in the circulating currentiZuis−7.3A (=−8.7kW/ (3×400V)) indict-A, and 7.3 An in DSCC-B. This is related to the power flow from the u-phase leg to the dc link.

C. Operating Performance under Transient States

Figs. 10 and 11 show the experimental and simulated waveforms in DSCC-A, where the active-power reference p^* was changing from 10 kW to−10 kW with a ramp function in20 ms (one cycle at the line frequency). Here, q_A^* and q_B^* were set to zero. This means that DSCC-A changes its operation from the rated rectification to the rated inversion whereas DSCC-Bodes it from the rated inversion to the rated rectification. Such an extremely fast response makes a significant contribution to



International Journal of Research (IJR)
e-ISSN: 2348-6848, p- ISSN: 2348-795X Volume 2, Issue 12, December 2015
Available at http://internationaljournalofresearch.org

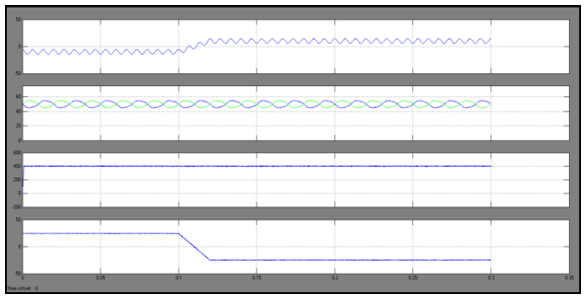
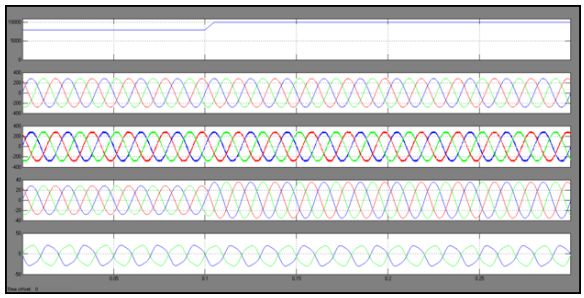


Fig. 8. Experimental waveforms to a ramp change in $p^*$from 10-kW (rated) rectification to 10-kW inversion where q_A^*=q_B^*=0.

Enhancing transient system stability and frequency-regulation capability in contingency situations such as emergency disconnections of large-capacity synchronous generators in thermal power plants from either power system. However, the fast response is not required during normal operation. No over current occurs in the supply currents, the arm currents, the circulating current, and the dc-link current. The clink current is changing from25A (= 10kW/400V) to−25 A. Moreover, the mean dc-capacitor voltages and the mean dc-link voltage are well regulated to their references even during the transient period. The experimental and simulated waveforms agree well with each other even under such a transient-state condition. Figs. 12 and 13 show the experimental and simulated waveforms to a small step change in p∗ from 8 to 10 kW, where q_A^*=q_B^*=0. The experimental and simulated waveforms agree well with each other. The theoretical analysis in Section V-C derives that the transient performance of the dc-link current exhibits a First-order response with a time constant owls/KZ=0.94ms, where LZ=3mH adz=3.2V/A in both experiment and, simulation.



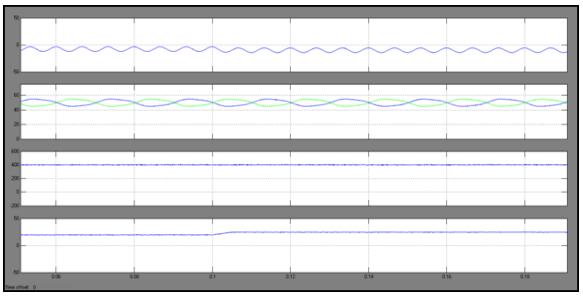


Fig. 9. Experimental waveforms to a small step change in active-power reference from p^*=8to 10 kW where q_A^*=q_B^*=0.

CONCLUSION

PI, PD and PID controllers are conventional, most popular controllers and widely used in most power system appliances. But, in the recent times there are many researchers who reported and successfully adopted Fuzzy Logic Controller (FLC) termed as intelligent controllers to their appliances. This paper has described an application of a modular multilevel cascade converter based on double-star choppercells (MMCC) to a back-to-back (BTB) system, by Hybrid Fuzzy intended for installation on 6.6-kV power distribution systems. The derived circuit equations of the BTB system has shown that the dc-link voltage and current can be controlled independently without any mutual inference. Moreover, an indirect control of the dclink voltage developed in this paper has eliminated neither a voltage sensor nor dc-link capacitors from the dc link.

REFERENCES

[1] H. Adage, "Classification, terminology, and application of the Modular Multilevel Cascade Converter (MMCC),"IEEE Trans. Power Electron., vol. 26, no. 11, pp. 3119–3130, Nov. 2011.

[2] R. Marquardt and A. Legnica, "A new modular voltage source inverter topology," import. EPE, 2003, pp. 2–4.

[3] S. Allegro, R. Hammers, and R. Marquardt, "New transformer less, scalable modular multilevel converters for HVDC-transmission," in Proc.IEEE PESC, 2008, pp. 174–179.

[4] R. Marquardt, "Modular multilevel converter: A universal concept for HVDC-networks and extended

dc-bus-applications," in Proc. IPEC, 2010, pp. 502–507.

[5] J. Qin and M. Saeedifard, "Predictive control of a modular multilevel Converter for a back-to-back HVDC system,"IEEE Trans. Power Del.,vol. 27, no. 3, pp. 1538–1547, Jul. 2012.

[6] M. Guan and Z. CSU, "Modeling and control of a modular multilevel Converter-based HVDC system under unbalanced grid conditions,"IEEE Trans. Power Electron. vol. 27, no. 12, pp. 4858–4867, Dec. 2012.

[7] G. Bergner et al., "An energy-based controller for HVDC modular multilevel converter in decoupled double synchronous reference frame for Voltage oscillation reduction,"IEEE Trans. Ind. Electron., vol. 60, no. 6, pp. 2360–2371, Jun. 2013.

[8] M. Hagiwara and H. Adage, "Control and experiment of pulsewidthmodulated modular multilevel converters,"IEEE Trans. Power Electron. vol. 24, no. 7, pp. 1737–1746, Jul. 2009.

[9] M. Hagiwara, K. Nishimura, and H. Adage, "A medium-voltage motorDrive with a modular multilevel PWM inverter,"IEEE Trans. Power Electron., vol. 25, no. 7, pp. 1786–1799, Jul. 2010.

[10] H. Pang, M. Hagiwara, and H. Adage, "Modeling and analysis of Switching-ripple voltage on the dc link between a diode rectifier and a Modular multilevel cascade inverter (MMCI),"IEEE Trans. Power Electron., vol. 28, no. 1, pp. 75–84, Jan. 2013.