

A new implementation of network fault tolerant voltage source converter for HVDC transmission system

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Abstract—this paper presents Fault Tolerant Voltage Source Converter for HVDC transmission system based on a hybrid multilevel voltage source converter with ac-side cascaded H-bridge cells. The proposed converter offers a unique feature of dc fault blocking capability (ability to block power exchange between the ac and dc sides during the dc side faults, hence no current flows in converter switches), operational flexibility in terms of active and reactive power control, black start capability, in addition to improve ac fault ride through capability. In this paper,fourquadrantoperationandvoltagesupport,thea canddc fault ride-through capabilities of the proposed converter will be demonstrated.

Index Terms—AC and DC fault ride through capabilities; DC fault reverse blocking capability; hybrid multilevel converter with ac side cascaded H bridgecells

I. INTRODUCTION

In the past decade, VSC-HVDC transmission systems have evolved from simple two level converters to neutral point clamped converters and then to true multilevel converters such as modular This converters. results to lower semiconductorlossesandincreasepowerhandlingcapab ility of VSC-HVDC transmission systems in comparison to conventional HVDC systems based on current source converters topology. However, the inability to withstand the effects of the HVDC network to dc side fault and the capability to operate at high voltage to isolate the dc fault current in absence of dc circuit breakers makes an issue towards the evolution of the dc grid. The main issues of the HVDC network during dc side faultsare:

- Over-current on converter switches during dc side faults, and after the fault cleared, inrush current as the dc link voltage buildsup.
- Dc side fault exposes the dc circuit breakers to high let-through current to tolerate the discharge of high fault current flowing at the dc side. It must be capable of operating at high voltage and isolates temporary or permanent dcfaults.

A new generation of converter using H-bridge cells has been implemented to eliminate the drawbacks for VSCs know as the Hybrid multilevel converter with H-bridge cells in the ac side. These converters inherently provide dc fault reverse blocking capability, which can be used to improve VSC-HVDCresiliencytodcsidefaults.Thefollowingofthis paper is organized asfollows.

Section II describes the operating principle of Hybrid multilevel converter with H-bridge cells in the ac side. Section III describes the control strategy for an HVDC transmission system based on a hybrid multilevel VSC with ac-side cascaded H-bridge cells. Section IV presents test network and simulations of a hybrid multilevel converter

HVDC transmission system. Section V gives conclusion.

II. HYBRIDMULTILEVELCONVERTERWIT H H-BRIDGECELLSINTHEACSIDE

Fig .1 shows single phase of a hybrid multilevel converter with N, H-bridge cells per phase. It can generate 4N+1

voltagelevelsatconverterterminal"a"withrespecttosuppl y

midpoint"0". Therefore, with large number of cells perphas e, the converter will produce pure sinusoidal voltage at the converter transformer. The H-bridge cells between "M" and "a" are operated as a series active filter to attenuate the

 $\label{eq:harmonics} \begin{array}{ll} \mbox{harmonics} involtage produced by two level converter bridg \\ e. In order to minimize the conversion losses in the H- \\ bridge cells, the requirement of number of cells has \\ been reduced to produce a voltage of V_{dc}/2 \mbox{ across the} \\ H-bridge & floating \end{array}$

capacitor.AsaresultofusinglessnumberofH-

bridgecells, a small converter station is required than modular multilevel converter. Here a seven cell topology is used which provides 29levelvoltageatconverterterminal. The effectives witchi ng frequency is less than 150 Hz per device. However the operation of hybrid multilevel VSC requires a voltage balancing scheme which ensures that the voltage across the H-bridge cells are maintained at International Journal of Research (IJR) e-ISSN: 2348-6848, p- ISSN: 2348-795X Volume 2, Issue 12, December 2015 Available at http://internationaljournalofresearch.org

Vdc/N under all operating conditions, where the Vdc is the total dc link voltage. By usingthisfeaturethefollowingbenefitsareachieved:

- Theriskoffailureofconverterswitchesduringdcsid e fault is reduced due to DC fault reverse blocking capability.
- Reduces the current rating of dc circuit breaker that will be required to isolate dc sidefaults.
- It allows recovery without interruption from temporary dc side faults. It also simplifies the recoverystrategyfromdcsidefaultsasthecurrenti n the dc side will decay tozero.



Fig.1.HybridmultilevelconverterwithH-bridgecellsintheacside

III. CONTROL STRATEGY FOR AN HVDCTRANSMISSION SYSTEM BASED ON A HYBRID MULTILEVELVSC

A HVDC transmission system based on a hybrid multilevel VSC with ac-side cascaded H-bridge cells requires three control system layers. The inner control layer represents the modulator and capacitor voltage-balancing mechanism that generates the gating signals for the converter switches and maintainsvoltagebalanceoftheH-bridgecellcapacitors. The intermediatecontrollayerrepresentsthecurrentcontroller thatregulatestheactiveandreactivecurrentcomponentsover the full operating range. The outer control layer is the dc voltage (or active power) and ac voltage (or reactive power) controller that provide set points to the current controllers. The current, power, and dc link voltage controller gains are selected using root locus analysis, based on the applicable transferfunctions.Fig.2summarizesthecontrollayersofthe hybrid multilevel VSC.





Fig.2.Schematicdiagramrepresentsthecontrollayerofthehybridmultilevelconverterwith ac side cascaded H-bridgecells





IV. TEST SYSTEM ANDSIMULATIONS

Fig.3showsthetestsystemwherethe687MVAVSCbased onthetopologyshowninFig.1, are operated as two converter stations of the VSC-HVDC transmission system. The VSC control system is designed for active power control and voltage magnitude at the PCC₂. In order to minimize the dc link voltage rise, when the VSC active power transfer collapsesasthevoltageatPCC2collapsesduringacfaults,the activepowerloopismodifiedsoastomaintainpowerbalance between the ac and dc sides and to eliminate the trapped energy in the dc link. G₂ represents a strong grid of 400kV, 1000MVA and X/R=3. In order to demonstrate the ac fault ridethroughcapabilityoftheconverter,thesysteminFig.3is subjected to three phase fault with fault duration of 140 msec. Fordcfaultcapability,thesysteminFig.3issubjectedtopole to pole with fault duration of140msec.

A. Four Quadrant Operation and VoltageSupport

For four quadrant operation and voltage support to the system in Fig.3, converter station 1 is commanded to

increase its output power from G_1 to G_2 from 0 to 0.5pu at 2.5pu/sec. At time t=1sec it is recommended to reverse the activepowerflowinordertoimportthepowerfromgridG₂, at - 2.5pu/sec. At t=2sec a load of 120+j90MVA is introduced at PCC₂. Fig.4 shows the system is able to meet steady state requirements, such as provision of voltage supportandfourquadrantoperation without compromising thevoltage and currentstresson the converters witches.





International Journal of Research (IJR)

e-ISSN: 2348-6848, p- ISSN: 2348-795X Volume 2, Issue 12, December 2015 Available at http://internationaljournalofresearch.org





(b) Active and reactive power converter station2 exchanges withPCC₂



International Journal of Research (IJR)

e-ISSN: 2348-6848, p- ISSN: 2348-795X Volume 2, Issue 12, December 2015 Available at http://internationaljournalofresearch.org



(g) Voltage across the dc link of converter station2 Fig.4 Waveforms demonstrating the steady state operation of HVDCsystem.

B. AC fault ride-throughcapability

Fig.5 shows the result obtained when the test system is subjected to a 140msec three phase fault to ground at the location shown in Fig.3. During the fault period, converter active power output is reduced to zero to minimize the trapped energy in the dc side thus minimizing the dc link voltage rise. The converter station recovers from the three-phase fault with the current controller limiting the current contribution to the fault during the entire fault period even the voltage magnitude at PCC₂ collapsing to zero. Also the voltage across the converter switches is controlled as the voltage across the cell capacitors remains at the desired set point.



(a) Active and Reactive power converter 1 exchanges withPCC₁



(b) Active and Reactive power converter 2 injects into PCC₂



(g) Voltage across H-bridge cells of the converter2



International Journal of Research (IJR)

e-ISSN: 2348-6848, p- ISSN: 2348-795X Volume 2, Issue 12, December 2015 Available at http://internationaljournalofresearch.org



 (h) Line to line voltage waveform at the terminalof converter1
Fig.5 Waveforms when the system in Fig.3 is subjected to a three phase to ground fault ,at time t=1sec with a fault duration of140msec

C. Dc fault ride-throughcapability

Fig.6showtheresultsobtainedduringpoletopoledcfaultsas shown in Fig.3 at time t=1sec with a duration of 140msec. During the fault period the converter station output active power is reduced to zero and converter reverse blocking capability is achieved by inhibiting the gating signals to the converterswitches.Thegatesignalstoconverterswitchesare restored when the fault is cleared at t=1.4sec and is followed by a gradual increase in converter output active power as shown in Fig.6. During the entire fault period, the active and reactivepowerexchangewiththegridareblocked,resultingin zero current in the converter switches. This confirms the ability of the H-bridge multilevel converter to eliminate the gridcontributiontothedcfaultcurrent,hencereducestherisk of over current inthe converter switches.



PCC₁



(b) Active and Reactive power converter 2 exchanges withPCC₂









International Journal of Research (IJR) e-ISSN: 2348-6848, p- ISSN: 2348-795X Volume 2, Issue 12, December 2015 Available at http://internationaljournalofresearch.org



(i)Voltage across the H-bridge cell capacitorsof converter1



(j)Voltage across the H bridge cell capacitorsof converter2

Fig.6 Waveforms during pole-to-pole dc fault at t=1sec with a duration of140msec

V. CONCLUSION

Based on the developed control strategy for the VSC-based HVDC power transmission i.e. the design of the current controller, the DC voltage controller, the active and reactive power controllers and the AC voltage controllers, the VSC-HVDC transmission system based on a hybrid multilevel converter with ac-side cascaded H-bridge cells is implemented. The behavior of the four-quadrant operation, voltage support capability and the ac fault ride-through capability of the HVDC system are simulated in the MATLABSimulinkandresultsareobtained.

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