



An Improved Single-Phase Transformer less Inverter for Grid-Connected PV System with Fuzzy Controller

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Abstract-

This paper presents a high-reliability single-phase transformerless grid-connected electrical converter that utilizes super junction MOSFETs to attain high potency for electrical phenomenon applications. The planned device utilizes 2 split ac-coupled inductors that operate on an individual basis for positive and negative 0.5 grid cycles. This eliminates the shoot-through issue that's encountered by ancient voltage supply inverters, resulting in increased system dependability. Dead time isn't needed at each the high-frequency pulsewidth modulation change commutation and also the grid zero crossing instants, up the standard of the output ac-current and increasing the device potency. The split structure of the planned electrical converter doesn't lead itself to the reverse-recovery problems for the most power switches and per se super junction MOSFETs is utilised with none dependability or potency penalties. Since MOSFETs area unit utilised within the planned device high potency is achieved even at lightweight load operations achieving a high CA energy commission (CEC) or Europe potency of the device system. It additionally has the power to work at higher change frequencies whereas maintaining high potency the upper operational frequencies with high potency allows reduced cooling necessities and ends up in system price savings by shrinking passive elements. With 2 extra ac-side switches conducting the currents throughout the freewheeling phases, the electrical phenomenon array is decoupled from the grid. This reduces the high-frequency common-mode voltage resulting in decreased mischance discharge current. The operation principle, common-mode characteristic and style issues of the planned transformerless electrical converter area unit illustrated. the entire losses of the ability semiconductor devices of many existing transformerless inverters that utilize MOSFETs as main switches area unit evaluated and compared. The experimental results with a five kW

example circuit show ninety nine.0% CEC potency and ninety nine.3% peak potency with a twenty kilohertz change frequency. The high dependability and potency of the planned device makes it terribly engaging for single-phase transformerless electrical phenomenon electrical converter applications with fuzzy logic controller.

Index Terms—California energy commission (CEC) efficiency; European union (EU) efficiency; MOSFET inverters; high efficiency; high reliability; transformer less grid-connected photo voltaic inverter

INTRODUCTION

Transformerless photovoltaic (PV) grid-connected inverters have the advantages of higher efficiency, lower cost, less complexity, and smaller volume compared to their counterparts with transformer galvanic isolation [1]–[27]. High frequency common-mode (CM) voltages must be avoided for a transformerless PV grid-connected inverter because it will lead to a large charge/discharge current partially flowing through the inverter to the ground. This CM ground current will cause an increase in the current harmonics, higher losses, safety problems, and electromagnetic interference (EMI) issues [28]–[31]. For a grid-connected PV system, energy yield and payback time are greatly dependant on the inverter's reliability and efficiency, which are regarded as two of the most significant characteristics for PV inverters. In order to minimize the ground leakage current and improve the efficiency of the converter system, transformerless PV inverters utilizing unipolar PWM control have been presented [8]–[27]. The weighted California Energy Commission (CEC) or European Union (EU) efficiencies of most commercially available and literature-reported single-phase PV transformerless

inverters are in the range of 96–98% [18]. Recently, several transformerless inverter topologies have been presented that use super junction MOSFETs devices [11]–[13] as main switches to avoid the fixed voltage-drop and the tail-current induced turn-off losses of IGBTs to achieve ultra high efficiency (over 98% weighted efficiency). One commercialized unipolar inverter topology, H5, as shown in Fig. 1(a), solves the ground leakage current issue and uses hybrid MOSFET and IGBT devices to achieve high efficiency [11]. The reported system peak and CEC efficiencies with an 8-kW converter system from the product datasheet is 98.3% and 98%, respectively, with 345-V dc input voltage and a 16-kHz switching frequency. However, this topology has high conduction losses due to the fact that the current must conduct through three switches in series during the active phase. Another disadvantage of the H5 is that the line-frequency switches S1 and S2 cannot utilize MOSFET devices because of the MOSFET body diode's slow reverse recovery. The slow reverse recovery of the MOSFET body diode can induce large turn-on losses, has a higher possibility of damage to the devices and leads to EMI problems. Shoot-through issues associated with traditional full bridge PWM inverters remain in the H5 topology due to the fact that the three active switches are series-connected to the dc bus.

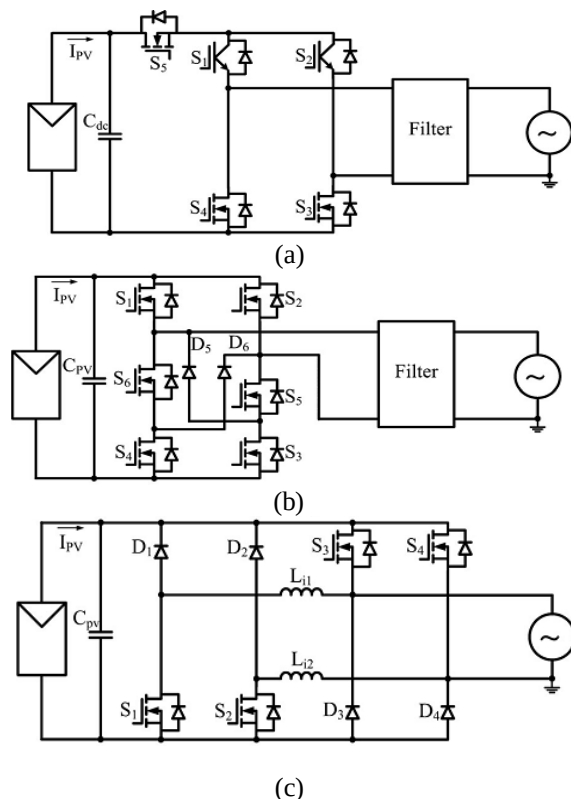


Fig 1 Single-phase transformerless PV inverters using super junction MOSFETs: (a) H5, (b) H6, and (c) dual-paralleled-buck inverters

Replacing the switch S5 of the H5 inverter with two split switches S5 and S6 into two phase legs and adding two freewheeling diodes D5 and D6 for freewheeling current flows, the H6 topology was proposed in [12]. The H6 inverter can be implemented using MOSFETs for the line frequency switching devices, eliminating the use of less efficient IGBTs. The reported peak efficiency and EU efficiency of a 300 W proto type circuit were 98.3% and 98.1%, respectively, with 180 V dc input voltage and 30 kHz switching frequency. The fixed voltage conduction losses of the IGBTs used in the H5 inverter are avoided in the H6 inverter topology improving efficiency; however, there are higher conduction losses due to the three series-connected switches in the current path during active phases. The shoot-through issues due to three active switches series connected to the dc-bus still remain in the H6 topology. Another disadvantage to the H6 inverter is that when the inverter output voltage and current has a phase shift the MOSFET body diodes may be activated. This can cause body diode reverse-recovery issues and decrease the reliability of the system. Another high-efficiency transformerless MOSFET inverter topology is the dual-paralleled-buck converter, as shown in Fig. 1(c). The dual-parallel-buck converter was inversely derived from the dual-boost bridgeless power-factor correction (PFC) circuit in [13]. The dual-paralleled-buck inverter eliminates the problem of high conduction losses in the H5 and H6 inverter topologies because there are only two active switches in series with the current path during active phases. The reported maximum and EU efficiencies of the dual-paralleled-buck inverter using Cool MOS switches and SiC diodes tested on a 4.5 kW prototype circuit were 99% and 98.8%, respectively, with an input voltage of 375 V and a switching frequency at 16 kHz. The main issue of this topology is that the grid is directly connected by two active switches S3 and S4, which may cause a grid short-circuit problem, reducing the reliability of the topology. A dead time of 500 μ s between the line-frequency switches S3 and S4 at the zero-crossing instants needed to be added to avoid grid shoot-through. This adjustment to improve the system reliability comes at the cost of high zero-crossing distortion for the output grid current. One key issue for a high efficiency and reliability transformerless PV

inverter is that in order to achieve high efficiency over a wide load range it is necessary to utilize MOSFETs for all switching devices. Another key issue is that the inverter should not have any shoot-through issues for higher reliability. In order to address these two key issues, a new inverter topology is proposed for single-phase transformerless PV grid-connected systems in this paper. The proposed transformerless PV inverter features: 1) high reliability because there are no shoot-through issues, 2) low output ac current distortion as a result of no dead-time requirements at every PWM switching commutation instant as well as at grid zero-crossing instants, 3) minimized CM leakage current because there are two additional ac-side switches that decouple the PV array from the grid during the freewheeling phases, and 4) all the active switches of the proposed converter can reliably employ super junction MOSFETs since it never has the chance to induce MOSFET body diode reverse recovery. As a result of the low conduction and switching losses of the super junction MOSFETs, the proposed converter can be designed to operate at higher switching frequencies while maintaining high system efficiency. Higher switching frequencies reduce the ac-current ripple and the size of passive components. Detailed power stage operation principle, PWM scheme, and CM leakage current analysis are described in this paper. The total losses of power devices for several existing MOS FET inverters are comparatively evaluated. The loss reduction by replacing IGBTs with super junction MOSFETs as power switches for the proposed transformerless inverter is analyzed. To verify the effectiveness and demonstrate the performance of the proposed transformerless inverter, a 5 kW prototype circuit was built and tested using two different switching frequencies, 20 and 40 kHz. Experimental results show that the proposed inverter topology not only eliminates the issues of MOSFET body diode reverse recovery, ground leakage current, and shoot-through; it also achieves 99.3% maximum efficiency and 99.0% CEC efficiency with high-quality output current waveforms.

PROPOSED TOPOLOGY AND OPERATION ANALYSIS

Fig. 2 shows the circuit diagram of the proposed transformerless PV inverter, which is composed of six MOSFETs

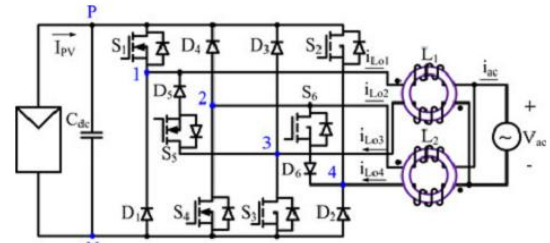


Fig. 2. Proposed high efficiency and reliability PV transformerless inverter topology

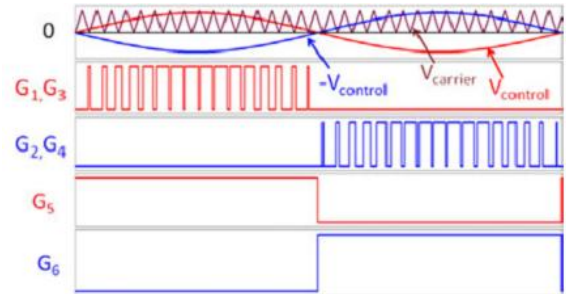
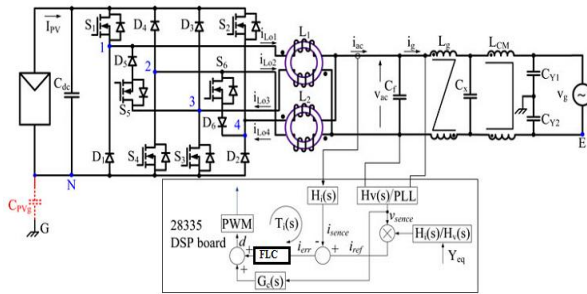


Fig. 3. Gating signals of the proposed transformerless PV inverter.

switches (S1 –S6), six diodes (D1 –D6), and two split ac-coupled inductors L1 and L2 . The diodes D1 –D4 perform voltage clamping functions for active switches S1 –S4. The ac-side switch pairs are composed of S5 , D5 and S6 , D6 , respectively, which provide unidirectional current flow branches during the freewheeling phases decoupling the grid from the PV array and minimizing the CM leakage current. Compared to the HERIC topology [9] the proposed inverter topology divides the ac side into two independent units for positive and negative half cycle. In addition to the high efficiency and low leakage current features, the proposed transformerless inverter avoids shoot-through enhancing the reliability of the inverter. The inherent structure of the proposed inverter does not lead itself to the reverse recovery issues for the main power switches and as such superjunction MOSFETs can be utilized without any reliability or efficiency penalties. Fig. 3 illustrates the PWM scheme for the proposed inverter. When the reference signal $V_{control}$ is higher than zero, MOSFETs S1 and S3 are switched simultaneously in the PWM mode and S5 is kept on as a polarity selection switch in the half grid cycle; the gating signals G2 , G4, and G6 are low and S2 , S4, and S6 are inactive. Similarly, if the reference signal $-V_{control}$ is higher than zero, MOSFETs S2 and S4 are switched simultaneously in the PWM mode and S6 is on as a



Block diagram of the complete inverter test system

GROUND LOOP LEAKAGE CURRENT ANALYSIS AND POWER DEVICES LOSSES CALCULATION AND EVALUATION

A. GROUND LOOP LEAKAGE CURRENT ANALYSIS FOR THE PROPOSED TRANSFORMERLESS INVERTER.

A galvanic connection between the ground of the grid and the PV array exists in transformerless grid-connected PV systems. Large ground leakage currents may appear due to the high stray capacitance between the PV array and the ground [28]–[31]. In order to analyze the ground loop leakage current, Fig. 5 shows a model with the phase output points 1, 2, 3, and 4 modeled as controlled voltage sources connected to the negative terminal of the dc bus (N point). Fig. 5 clearly illustrates the stray elements influencing the ground leakage current, which include: 1) the stray capacitance between PV array and ground CPVg; 2) stray capacitances between the inverter devices and the ground Cg1 – Cg4; and 3) the series impedance between the ground connection points of the inverter and the grid Zg. The differential-mode (DM) filter capacitor Cx and the CM filter components LCM, CY1, and CY2 are also shown in the model. The value of the stray capacitances Cg1, Cg2, Cg3, and Cg4 of MOSFETs is very low compared with that of CPVg, therefore the influence of these capacitors on the leakage current can be neglected. It is also noticed that the DM capacitor Cx does not affect the CM leakage current. Moreover, during the positive half-line cycle, switches S2, S4, and S6 are kept deactivated; hence the controlled voltage sources V2N and V4N are equal to zero and can be removed. Consequently, a simplified CM leakage current model for the positive half-line cycle is derived as shown in Fig. 6.

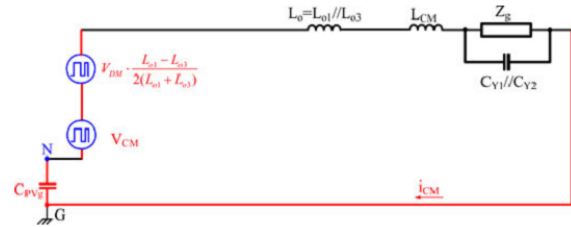


Fig. 7. Simplified single-loop CM model for positive half-line cycle.

With the help of the CM and DM concepts and by introducing the equivalent circuits between N and E, a single-loop mode applicable to the CM leakage current analysis for the positive half-line cycle of the proposed transformerless inverter is obtained, as shown in Fig. 7, with

$$V_{CM} = \frac{V_{IN} + V_{3N}}{2} \quad (1)$$

$$V_{DM} = V_{IN} - V_{3N} \quad (2)$$

A total CM voltage VtCM [31] is defined as

$$V_{tCM} = V_{CM} + V_{DM} \cdot \frac{L_{o1} - L_{o3}}{2(L_{o1} + L_{o3})} = \frac{V_{IN} + V_{3N}}{2} + (V_{IN} - V_{3N}) \cdot \frac{L_{o1} - L_{o3}}{2(L_{o1} + L_{o3})} \quad (3)$$

It is clear that if the total CM voltage VtCM keeps constant, no CM current flows through the converter. For a well-designed circuit with symmetrically structured magnetic, normally Lo1 is equal to Lo3. During the active stage of the positive half-line cycle, V1N is equal to Vdc, while V3N is equal to 0. Hence, the total CM voltage can be calculated as

$$V_{tCM} = \frac{V_{IN} + V_{3N}}{2} + (V_{IN} - V_{3N}) \cdot \frac{L_{o1} - L_{o3}}{2(L_{o1} + L_{o3})} = \frac{V_{dc}}{2} \quad (4)$$

During the freewheeling stage of the positive half-line cycle, under the condition that S1 and S3 share the dc-link voltage equally when they are simultaneously turned OFF, one can obtain

$$V_{IN} = V_{3N} = \frac{V_{dc}}{2} \quad (5)$$

Therefore, the total CM voltage during the freewheeling stage is calculated as

$$V_{tCM} = \frac{V_{IN} + V_{3N}}{2} + (V_{IN} - V_{3N}) \cdot \frac{L_{o1} - L_{o3}}{2(L_{o1} + L_{o3})}$$

$$= \frac{V_{dc}}{2} \quad (6)$$

Equations (4) and (6) indicate that the total CM voltage keeps constant in the whole positive half-line cycle. As a result, no CM current is excited. Similarly, during the whole negative half-line cycle, the CM leakage current mode is exactly the same as the one during the positive half-line cycle; the only difference is the activation of different devices. The total CM voltage in the negative half-line cycle is also equal to $V_{dc}/2$. Therefore,

TABLE I
SPECIFICATIONS AND POWER DEVICES FOR
EFFICIENCY EVALUATION

Nominal input voltage	380V
Grid voltage	240Vac
Nominal frequency	60Hz
Nominal output power	5 kW
Nominal AC current	21A
Switching frequency	20kHz
MOSFETs	IPW60R041C6
IGBTs	IRGB4063D
Diodes	APT30DQ60B

in the whole grid cycle the total CM voltage keeps constant, minimizing CM ground leakage current.

B. Calculation and Comparison of the Power Semiconductor Device Losses for Several Existing MOSFET Transformerless Inverters

Since the efficiency of PV transformerless inverters is normally compared by using weighted efficiency concepts, such as “CEC Efficiency” and “EU Efficiency,” it is critical to evaluate power semiconductor device losses at different load conditions rather than at nominal load condition when evaluating the efficiency of MOSFET transformerless PV inverters. The specifications and power devices for efficiency evaluation of several existing MOSFET transformerless PV inverters [11]–[13] and the proposed

inverter are listed in Table I. The first-order conduction voltage drop models of semiconductor devices can be given by

$$MOSFET : v_{ds}(t) = i(t) \cdot R_{ds} \quad (7)$$

$$IGBT : v_{ce}(t) = V_t + i(t) \cdot R_{ce} \quad (8)$$

$$Diode : v_{ak}(t) = V_f + i(t) \cdot R_{ak} \quad (9)$$

where v_{ds} is the MOSFET drain–source voltage drop, R_{ds} is the MOSFET drain–source on resistance, v_{ce} is the IGBT collector–emitter voltage drop, V_t is the IGBT equivalent voltage drop under zero current condition, R_{ce} is the IGBT on resistance, v_{ak} is the diode anode–cathode voltage drop, V_f is the diode equivalent voltage drop under zero current condition, and R_{ak} is diode on resistance; $i(t)$ is the inverter output current and expressed as

$$i(t) = I_m \cdot \sin(\omega t) \quad (10)$$

where I_m is the peak inverter output current and ω is the angular frequency of the inverter output current. The duty ratios for active-stage devices and zero-stage devices of unipolar grid connected PWM inverters are expressed as (11) and (12), respectively

$$d_{active}(t) = M \sin(\omega t) \quad (11)$$

$$d_{zero}(t) = 1 - M \sin(\omega t) \quad (12)$$

The conduction losses for active-stage MOSFET switches, active-stage IGBT switches, zero-stage MOSFET switches, zero-stage IGBT switches, and zero-stage diodes can be calculated, respectively, from (13) to (17)

$$P_{con_active_MOSFET} = \frac{1}{2\pi} \int_0^\pi i(t) v_{ds}(t) d_{active}(t) d\omega t$$

$$= I_m^2 R_{ds} \frac{2M}{3\pi} \quad (13)$$

$$P_{con_active_IGBT} = \frac{1}{2\pi} \int_0^\pi i(t) v_{ce}(t) d_{active}(t) d\omega t$$

$$= I_m V_t \frac{M}{4} I_m^2 R_{ce} \frac{2M}{3\pi} \quad (14)$$

$$P_{con_zer o_MOSFET} = \frac{1}{2\pi} \int_0^\pi i(t) v_{ds}(t) d_{zero}(t) d\omega t$$

$$= I_m^2 R_{ds} \left(\frac{M}{4} - \frac{2M}{3\pi} \right) \quad (15)$$

$$P_{con_zer o_IGBT} = \frac{1}{2\pi} \int_0^\pi i(t) v_{IGBT}(t) d_{zero}(t) d\omega t$$

$$= I_m V_t \left(\frac{1}{\pi} - \frac{M}{4} \right) I_m^2 R_{ce} \left(\frac{M}{4} - \frac{2M}{3\pi} \right) \quad (16)$$

$$P_{con_zero_Diode} = \frac{1}{2\pi} \int_0^\pi i(t) v_{ak}(t) (1 - M \sin(\omega t)) d\omega t$$

$$= I_m V_t \left(\frac{1}{\pi} - \frac{M}{4} \right) + I_m^2 R_{ak} \left(\frac{1}{4} - \frac{2M}{3\pi} \right) \quad (16)$$

For MOSFET devices, the main loss source for switching transitions is the capacitive turn-on loss resulting from the discharge of the junction capacitor Coss of MOSFETs [36], which is dependent on the switched dc bus voltage and switching frequency. Normally, this capacitive turn-on energy dissipation can be obtained from the device datasheet. Hence, the switching loss of active-stage MOSFETs can be simply expressed as

$$P_{SW_active_MOSFET} = f_{SW} E_{oss}(V_{ds}) \quad (18)$$

Another part of switching losses of active switches is induced by the diode reverse recovery of the zero-stage diodes. The switching energy induced in the

main switches during diode reverse recovery period can be approximated as

$$E_{d_rr} = V_{dc} I_L \left[\left(1 + \frac{I_{rr}}{2I_L} \right) t_a + \frac{I_{rr}}{4I_L} \right]$$

$$= V_{dc} I_L t_a + V_{dc} \frac{I_{rr}}{4} (2t_a + t_b) \quad (19)$$

where I_L is the switched load current, and the definitions of t_a , t_b , and I_{rr} are shown in Fig. 8. The switching loss of active-stage switches induced by the diode reverse recovery of the zero-stage devices can

be obtained by the integral of (19) in the whole grid cycle

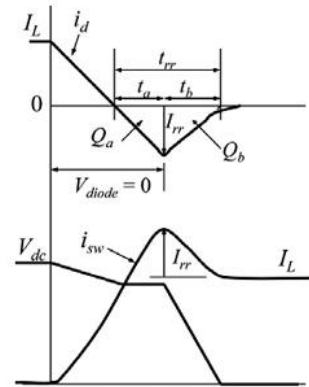


Fig. 8. Simplified waveforms showing switching losses induced in the main switches and diodes during diode reverse recovery.

$$P_{d_rr} = \frac{1}{2\pi} \int_0^\pi f_{SW} \left[V_{dc} I_m \sin(\omega t) t_a + V_{dc} \frac{I_{rr}}{4} (2t_a + t_b) \right] d\omega t$$

$$= \left(\frac{I_m t_a}{\pi} + \frac{I_{rr} (2t_a + t_b)}{8} \right) V_{dc} f_{SW} \quad (20)$$

TABLE II
TOTAL LOSSES OF POWER DEVICES AT
DIFFERENT CEC OUTPUT POWER
CONDITIONS AT 20 KHZ SWITCHING
FREQUENCY

Po (%)	H5 (W)	H6 (W)	DPB (W)	Proposed (W)
100%	76.99	68.65	53.56	53.56
75%	41.24	43.04	34.55	34.55
50%	30.67	23.89	20.12	20.12
30%	17.92	13.23	11.87	11.87
20%	12.79	9.45	8.85	8.85
10%	8.48	7.80	6.56	6.56

The third part of the switching losses is the switching loss induced in the diode during the diode reverse recovery interval, which can be approximated as

$$P_{d_sw} = f_{SW} (0.55 I_{rr}) (0.55 V_{dc}) t_b. \quad (21)$$

By substituting the parameters from the datasheets of IPW60R041C6 [33], IRGP4063D [34], and APT30DQ60B [35], the total losses calculated for CEC

efficiency evaluation for H5 [11], H6 [12], the dual-paralleled-buck (abbreviated as DPB) [13] transformerless PV inverters and the proposed inverter are listed in Table II. It can be seen that the total power semiconductor device losses for H5 is highest due to the IGBT's fixed voltage-drop. The power devices' losses of DPB and the proposed inverters are minimum and the proposed inverter can achieve the same high efficiency as the MOSFET DPB inverter in [13].

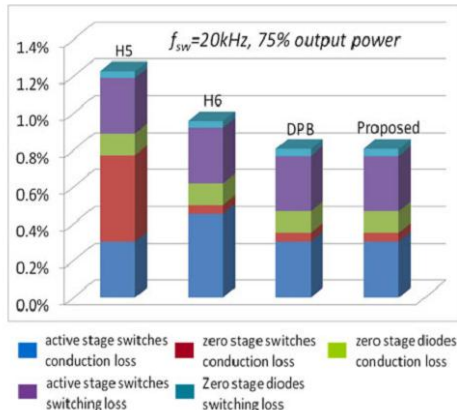


Fig. 9. Power semiconductor device losses distribution comparison for H5, H6, DPB, and proposed transformerless PV inverters with 75% of the rated output power.

The power semiconductor device losses distribution for H5, H6, DPB, and proposed inverters at 75% of the rated output power condition, which is the most dominant term in CEC efficiency evaluation, is also shown in Fig. 9. It can be seen from Fig. 9 that the switching losses for these four MOSFET inverters are almost the same. The conduction losses of H5 are highest because of the IGBT's fixed voltage drop. The conduction losses of the H6 inverter are higher than DPB and the proposed inverters because one more switch is in series in the current path during the active stages. The proposed transformer less inverter can achieve the same high efficiency as the DPB MOSFET inverter in [13]. However, the reliability of the proposed converter is greatly enhanced and the quality of output ac current is improved compared to the DPB MOSFET inverter in [13].

C. Loss Reduction With MOSFETs Replacing IGBTs as Power Switches for the Proposed Transformerless Inverter

In order to highlight the advantages of employing superjunction MOSFETs instead of IGBTs as the main switches to achieve ultra high efficiency, the loss reduction with MOSFETs replacing IGBTs as

power switches for the proposed transformerless inverter is evaluated in this section. The turn-on and turn-off switching losses for active-stage IGBTs can be calculated as (22) and (23), respectively.

$$P_{SW_on} = \frac{1}{2\sqrt{\pi}} f_{sw} \alpha_{on} I_m^{\beta_{on}} k_{g_on} \frac{V_{dc}}{V_{test}} \frac{r(\frac{\beta_{on}+1}{2})}{(\frac{\beta_{on}}{2}+1)} \quad (22)$$

$$P_{SW_off} = \frac{1}{2\sqrt{\pi}} f_{sw} \alpha_{off} I_m^{\beta_{off}} k_{g_off} \frac{V_{dc}}{V_{test}} \frac{r(\frac{\beta_{off}+1}{2})}{(\frac{\beta_{off}}{2}+1)} \quad (22)$$

where $\Gamma \beta_{off} + 12 / \Gamma \beta_{2off} + 1 = \sqrt{1\pi} 0\pi (\sin \omega t) \beta_{off} \omega t$; k_{g_on} is gate drive stiffness factor during turn-on; k_{g_off} is gate drive stiffness factor during turn-off; α_{on} and β_{on} are turn-on

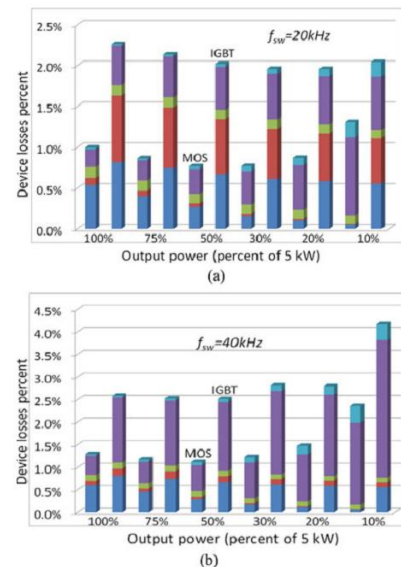


Fig 10 Power semiconductor device losses distribution comparison for the proposed inverter using MOSFETs and IGBTs at different output power: (a) 20 kHz switching frequency, and (b) 40 kHz switching frequency energy coefficients; α_{off} and β_{off} are turn-off energy coefficients; V_{dc} is the actual switched dc bus voltage; and V_{test} is test voltage for switching energy coefficients on the IGBT data sheets. α_{on} , β_{on} , α_{off} , and β_{off} can be obtained through MATLAB curve fitting based on the E_{on} and E_{off} of IGBT datasheet. The power semiconductor device losses distribution for the proposed inverter with MOSFETs and IGBTs at

different CEC output power with operating switching frequencies of 20 and 40 kHz are comparatively illustrated in Fig. 10(a) and (b), respectively. From Fig. 10(b), when IGBTs are employed as power devices, the total power semiconductor device losses of the proposed inverter are already more than 2.4% for all tested power ranges in CEC efficiency calculation at 40 kHz switching frequency. If other losses such as output inductor loss, gate drive loss, and control board loss are included, the losses of the whole inverter system will be above 3%. As a result, the efficiency of the whole inverter system is less than 97%, which is relatively low for a transformerless grid-connected PV inverter. On the other hand, for the MOSFET inverter operating at 40 kHz switching frequency, the total power semiconductor device losses are less than 1.2% with the output power higher than 30% of the rated power and no more than 2.4% even at 10% output power. If other losses are included, the CEC and EU efficiencies of the whole inverter can still achieve an efficiency over 98%, which is higher than most of the commercially available transformerless PV inverters. Hence, a higher switching frequency operation can be adopted for the proposed inverter with superjunction MOSFETs to reduce the output current ripple and the size of passive components, while the inverter still maintains a high-level system efficiency. The experimental waveforms of the grid current i_g , the inductor currents i_{Lo1} , and i_{Lo2} under the 240 Vrms grid voltage and half-load conditions are shown in Fig. 13. This figure shows that the proposed inverter presents high-power factor and low harmonic distortion. Fig. 14 shows the leakage current test waveforms, the CM leakage current is successfully limited with the peak value 59.5 mA and rms value 10.33 mA, which are well below the limitation requirements of the German standard VDE0126-1-1 [32]. Fig. 15 shows the measured efficiencies as a function of the output power for the proposed transformerless PV inverter at switching frequencies of 20 and 40 kHz. Note that the presented efficiency diagram covers the losses of the main power stage including power semiconductor device losses and output inductor losses, but it does not include the power consumption of control circuit and the associated driver circuit. The maximum experimental efficiency of the prototype circuit is 99.3% and 99.0% with 20 and 40 kHz switching frequency operations, respectively. As shown in (24), the CEC efficiency is calculated combining different weighted factors at different output power levels.

FUZZY LOGIC CONTROLLER

In FLC, basic control action is determined by a set of linguistic rules. These rules are determined by the system. Since the numerical variables are converted into linguistic variables, mathematical modeling of the system is not required in FC. The FLC comprises of three parts: fuzzification, inference engine and defuzzification. The FC is characterized as i. seven fuzzy sets for each input and output. ii. Triangular membership functions for simplicity. iii. Fuzzification using continuous universe of discourse. iv. Implication using Mamdani's, 'min' operator. v. Defuzzification using the height method.

Fuzzification: Membership function values are assigned to the linguistic variables, using seven fuzzy subsets: NB (Negative Big), NM (Negative Medium), NS (Negative Small), ZE (Zero), PS (Positive Small), PM (Positive Medium), and PB (Positive Big). The

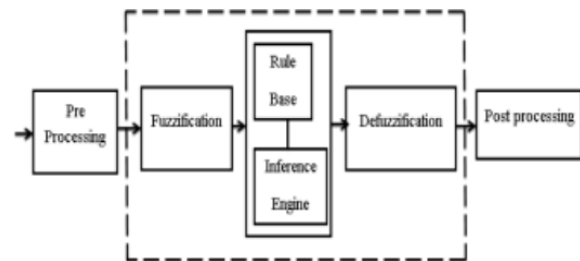


Fig.(a) Fuzzy logic controller

partition of fuzzy subsets and the shape of membership $CE(k)$ $E(k)$ function adapt the shape up to appropriate system. The value of input error and change in error are normalized by an input scaling factor.

Table I Fuzzy Rules

Change in error	Error						
	NB	NM	NS	Z	PS	PM	PB
NB	PB	PB	PB	PM	PM	PS	Z
NM	PB	PB	PM	PM	PS	Z	Z
NS	PB	PM	PS	PS	Z	NM	NB
Z	PB	PM	PS	Z	NS	NM	NB
PS	PM	PS	Z	NS	NM	NB	NB
PM	PS	Z	NS	NM	NM	NB	NB
PB	Z	NS	NM	NM	NB	NB	NB

In this system the input scaling factor has been designed such that input values are between -1 and +1. The triangular shape of the membership function of this arrangement presumes that for any particular $E(k)$ input there is only one dominant fuzzy subset. The input error for the FLC is given as

$$E(k) = \frac{P_{ph}(k) - P_{ph}(k-1)}{V_{ph}(k) - V_{ph}(k-1)} \quad (10)$$

$$CE(k) = E(k) - E(k-1) \quad (11)$$

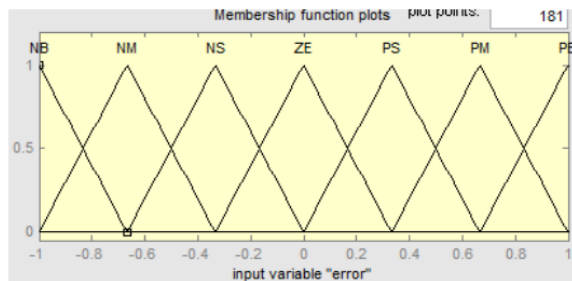


Fig.(b) Membership functions

Inference Method: Several composition methods such as Max-Min and Max-Dot have been proposed in the literature. In this paper Min method is used. The output membership function of each rule is given by the minimum operator and maximum operator. Table 1 shows rule base of the FLC.

Defuzzification: As a plant usually requires a non-fuzzy value of control, a defuzzification stage is needed. To compute the output of the FLC, „height“ method is used and the FLC output modifies the control output. Further, the output of FLC controls the switch in the inverter. In UPQC, the active power, reactive power, terminal voltage of the line and capacitor voltage are required to be maintained. In order to control these parameters, they are sensed and compared with the reference values. To achieve this, the membership functions of FC are: error, change in error and output

The set of FC rules are derived from

$$u = -[\alpha E + (1-\alpha)C]$$

Where α is self-adjustable factor which can regulate the whole operation. E is the error of the system, C is the change in error and u is the control variable. A large value of error E indicates that given system is not in the balanced state. If the system is unbalanced, the controller should enlarge its control variables to balance the system

as early as possible. On the other hand, small value of the error E indicates that the system is near to balanced state. Overshoot plays an important role in the system stability. Less overshoot is required for system stability and in restraining oscillations. During the process, it is assumed that neither the UPQC absorbs active power nor it supplies active power during normal conditions. So the active power flowing through the UPQC is assumed to be constant. The set of FC rules is made using Fig.(b) is given in Table 1.

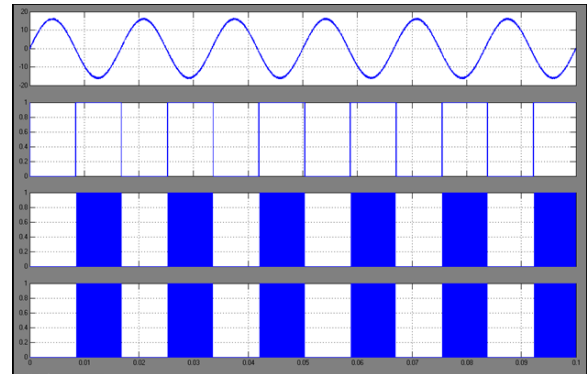


Fig. 11. Switch gating signals: in (a) grid cycle and (b) PWM cycle.

The calculated CEC efficiencies of the proposed transformer less inverter at 20 and 40 kHz switching frequencies are 99% and 98.8%, respectively. The CEC efficiency at 40 kHz switching frequency is about 0.2% lower than at 20 kHz switching frequency operation. However, 40 kHz operation can gain the benefits of reduced output current ripple and the reduced size of passive components.

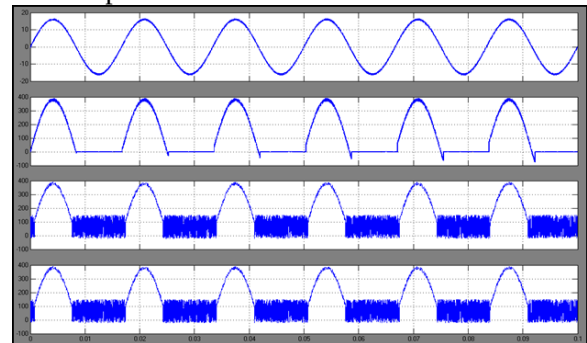


Fig. 12. Drain-source voltage waveforms of the switches S1, S3, and S5 : in (a) grid cycle and (b) in PWM cycle.

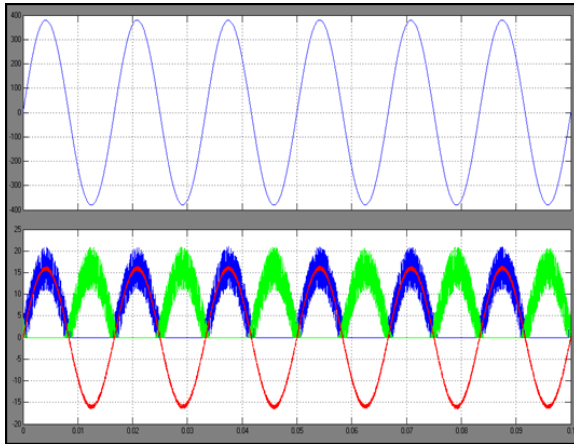


Fig. 13 Experimental waveforms of ground potential VEN, grid current, and current of inductor L_{o1} .

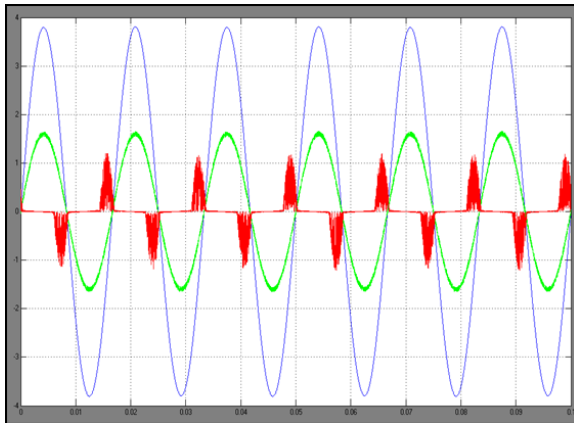


Fig 14 Leakage current test waveforms.

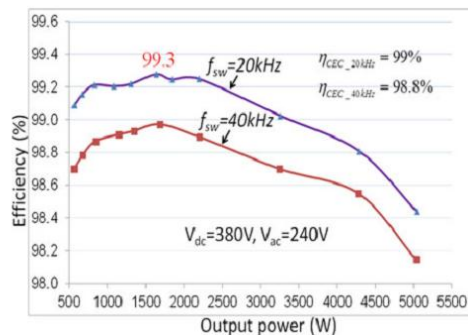


Fig. 15. Measured efficiency as a function of the output power with switching frequencies at 20 and 40 kHz.

CONCLUSION

A high reliability and efficiency inverter for transformer less PV grid-connected power generation systems is presented in this paper. The main characteristics of the proposed transformer less inverter are summarized as follows

1) Ultra high efficiency can be achieved over a wide output power range by reliably employing super junction

MOSFETs for all switches since their body diodes are never activated

2) No shoot-through issue leads to greatly enhanced reliability

3) low ac output current distortion is achieved because dead time is not needed at PWM switching commutation instants and grid-cycle zero-crossing instants

4) low-ground loop CM leakage current is present as a result of two additional unidirectional-current switches decoupling the PV array from the grid during the zero stages

5) Higher switching frequency operation is allowed to reduce the output current ripple and the size of passive components while the inverter still maintains high efficiency

6) The higher operating frequencies with high efficiency enables reduced cooling requirements and results in system cost savings by shrinking passive components.

The experimental results tested on a 5 kW hardware prototype verify the effectiveness of the proposed converter and show 99.0% CEC efficiency. With the super high efficiency, low leakage ground loop CM current, high quality of output current and greatly enhanced reliability, the proposed topology is very attractive for transformer less PV inverter applications.

REFERENCES

- [1] J. S. Lai, "Power conditioning circuit topologies," IEEE Ind. Electron. Mag., vol. 3, no. 2, pp. 24–34, Jun. 2009.
- [2] S. B. Kjaer, J. K. Pedersen, and F. Blaabjerg, "A review of single-phase grid-connected inverters for photovoltaic modules," IEEE Trans. Ind. Appl., vol. 41, no. 5, pp. 1292–1306, Sep./Oct. 2005.
- [3] M. Calais, J. Myrzik, T. Spooner, and V. G. Agelidis, "Inverters for single phase grid connected photovoltaic systems—An overview," in Proc. IEEE Annu. Power Electron. Spec. Conf., 2002, vol. 2, pp. 1995–2000.
- [4] Y. Xue, L. Chang, S. B. Kjaer, J. Bordonau, and T. Shimizu, "Topologies of single-phase inverter for small distributed power generators: An overview," IEEE Trans. Power Electron., vol. 19, no. 5, pp. 1305–1314, Sep. 2004.
- [5] Q. Li and P. Wolfs, "A review of the single phase photovoltaic module integrated converter topologies



with three different DC link configurations,” IEEE Trans. Ind. Electron., vol. 23, no. 23, pp. 1320–1333, Apr. 2008.

IEEE Trans. Power Electron., vol. 56, no. 4, pp. 1253–1260, Apr. 2011.

[6] J. M. A. Myrzik and M. Calais, “String and module integrated inverters for single-phase grid connected photovoltaic systems-A review,” in Proc. IEEE Bologna Power Tech Conf., Bologna, Italy, Jun. 2003, pp. 430–437.

[7] F. Schimpf and L. E. Norum, “Grid connected converters for photovoltaic, state of the art, ideas for improvement of transformerless inverters,” presented at the Nordic Workshop Power Ind. Electron., Espoo, Finland, Jun. 2008.

[8] R. Gonzalez, J. Lopez, P. Sanchis, and L. Marroyo, “Transformerless inverter for single-phase photovoltaic systems,” IEEE Trans. Power Electron., vol. 22, no. 2, pp. 693–697, Mar. 2007.

[9] H. Schmidt, C. Siedle, and J. Ketterer, “DC/AC converter to convert direct electric voltage into alternating voltage or into alternating current,” U.S. Patent 7046534 B2, May 2006.

[10] M. Victor, F. Greizer, S. Bremicker, and U. Hubler, “Method of converting a direct current voltage of a source of direct current voltage, more specifically of a photovoltaic source of direct current voltage, into an alternating current voltage,” U.S. Patent 7411802 B2, Aug. 2008.

[11] SMA Sunny Boy 8000TL-US datasheet. [Online]. Available: <http://www.sma-america-.com>

[12] W. Yu, J. S. Lai, H. Qian, and C. Hutchens, “High-efficiency MOSFET inverter with H6-type configuration for photovoltaic non-isolated AC-module applications,”