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Look-Ahead Clock Gating On Novel Auto-Gated Detff Flip-Flops

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Abstract:-

Gating of the clock signal in VLSI chips is nowadays a mainstream methodology for reducing switching power consumption. several techniques to reduce dynamic power of which clock gating is predominant. clock gating is employed at all levels: system architecture, block design, logic design and gates. three gating methods are known. the most popular is synthesis based on the logic of underlying system. It leaves the majority of clock pulses driving flip flops redundant. The data driven clock gating yields higher power savings but its design methodology is complex. Third method is auto gated flip flops , it is simple but yields small power savings. Our data-driven clock gating is integrated into an Electronic Design Automation (EDA) commercial backend design flow, achieving total power reduction of 15%–20% for various types of large-scale state-of-the-art industrial and academic designs in 40 and 65 manometer process technologies.

Keywords— Clock Gating; Clock Networks; Dynamic Power Reduction

I.INTRODUCTION

The increasing demand for low power mobile computing and consumer electronics products has refocused VLSI design in the last two decades on lowering power and increasing energy efficiency. Power reduction is treated at all design levels of VLSI chips, from architecture through block and logic levels, down to gate-level, circuit and physical implementation.One of the major dynamic power consumers is the system's clock signal, typically responsible for up to 50% of the total dynamic power consumption. major dynamic power consumers in computing and consumer electronics products is the system's clock signal, typically responsible for 30%–70% of the total dynamic power consumption . Several techniques to reduce the dynamic power are developed, of which clock gating is predominant. Ordinarily, when a logic unit is clocked, its underlying sequential elements receive the clock signal, regardless of whether or not they will toggle in the next cycle. With clock gating, the clock signals are ANDed with explicitly predefined enabling signals. Another grouping of FFs for clock switching power reduction, called multi bit FF (MBFF), has recently been proposed. MBFF attempts to physically merge FFs into a single cell such that the inverters driving the clock pulse into its master and slave latches are shared among all FFs in a group.

II. Various Clock Gating Techniques

2.1 AND CLOCK GATING:

In sequential circuit one two-input AND gate is inserted in logic for clock gating.one input to AND gate is clock while the second input is a signal used to control the output.clock gating technique for the counter by inserting one AND gate.when counter is negative edge triggered and

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enable changes from a clock cycle starting from the negative edge to the next negative edge.

2.2 NOR CLOCK GATING:

NOR gate is a suitable technique for clock gating where we need to be performed on positive edge of the global clock.for analyzing using NOR gate ,the counter will work when enable turn ON.when enable changes to "1" counter output is negative edge of the clock and small glitches will be occur.

2.3 SYNTHESIS BASED CLOCK GATING:

Synthesis-based clock gating is the most widely used method by EDA tools. The utilization of the clock pulses, measured by data-to-clock toggling ratio, left after the employment of synthesis- based gating may still be very low. In this method, the average data-to-clock toggling ratio, obtained by extensive power simulations of 61 blocks comprising 200 k FFs, taken from a 32 nm high-end 64-bit microprocessor. Those are mostly control blocks of the data-path, register-file and memory management units of the processor. The technology parameters used throughout the papers are of 22 nm low-leakage process technology. Their clock enabling signals were derived by a mix of logic synthesis and manual definitions. The clock capacitive load is 70% of their total load. The blocks are increasingly ordered by their data-to-clock activity ratio. It is clearly shown that the data toggles in a very low rate compared to the gated clocks.

2.4 DATA DRIVEN CLOCK GATING:

Clock enabling signals are very well understood at the system level and thus can effectively be defined and capture the periods where functional blocks and modules do not need to be clocked. Those are later being automatically synthesized into clock enabling signals at the gate level. In many cases, clock enabling signals are manually added for every FF as a part of a design methodology. Still, when modules at a high and gate level are clocked, the state transitions of their underlying FFs depend on the data being processed. It is important to note that the entire dynamic power consumed by a system stems from the periods where modules' clock signals are enabled. A FF finds out that its clock can be disabled in the next cycle byXORing its output with the present data input that will appear at its output in the next cycle. The outputs of k XOR gates are ORed to generate a joint gating signal for k FFs, which is then latched to avoid glitches. The combination of a latch with AND gate is commonly used by commercial tools and is called integrated clock gate.

2.5 ADAPTIVE CLOCK GATING:

In this method, a FF can find out that its clock can be disabled in the next cycle. A XOR gate compares the FF's current outputwith the present data input thatwill appear at the output in the next cycle. The XOR's output indicates whether a clock signal will be required in the next cycle. The clock driver is then replaced by a 2-way AND gate called clock gater. We will use the symbol in to represent FFs that incorporate generation. In practice the XOR is connected to the output of FF's internal master rather than D, as it is guaranteed to be stable when the FF's slave is transparent. Controlling the clock in each FF by a dedicated gater was studied. An implementation for a linear feedback shift register (LFSR) has been presented, where a 10% net power reduction was reported. Additional power reduction can be achieved by lowering the number of clock gaters. We could drive several FFs with a common gater if we knew that they are toggling simultaneously most of the time, thus achieving almost the same power reduction, but with fewer gaters. The grouping may place up to several

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dozens of FFs in a single group, and is usually done by synthesizers during the physical design phase. Such tools are focusing on skew, power, and area minimization, and are not aware of the toggling correlations of the underlying FFs.

III. PROPOSED WORK

Look-ahead clock gating has been shown to be very useful in reducing the clock switching power. The computation of the Clock enabling signals one cycle ahead of time avoids the tight timing constraints existing in other gating methods. A closed form model characterizing the power saving was presented and used in the implementation of the gating logic. The gating logic can be further optimized by matching target FFs for joint gating which may significantly reduce the hardware overheads.While this technique discussed the case of merging two target FFs for joint gating, clustering target FFs in larger groups may yield higher power savings.

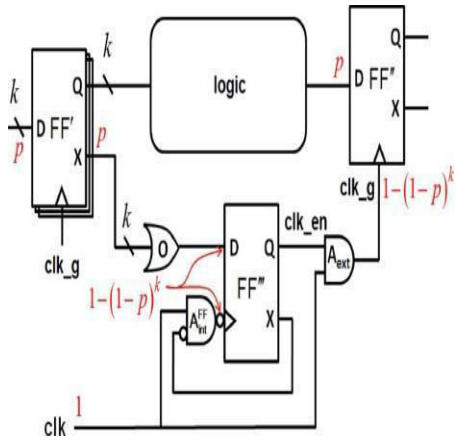

Fig: Look ahead clock gating

IV. CONCLUSION

In a power-managed system, the state of operation of various components is dynamically adapted to the required performance level, in an effort to minimize the power wasted by idle or underutilized components. For most system components, state transitions have nonnegligible power and performance costs. Thus, the problem of designing power management policies that minimize power under performance constraints is a challenging one.

We surveyed several classes of power-managed systems and power management policies. Furthermore, we analyzed the tradeoffs involved in designing and implementing power-managed systems. Several practical examples of power-managed systems were analyzed anddiscussed in detail.Look-ahead clock gating has been shown to be very useful in reducing the clock switching power. The computation of the clock enabling signals one cycle ahead of time avoids the tight timing constraints existing in other gating methods. A closed form model characterizing the power saving was presented and used in the implementation of the gating logic. The gating logic can be further optimized by matching target FFs for joint gating which may signifcantly reduce the hardware overheads. While this paper discussed the case of merging two target FFs for joint gating, clustering target FFs in larger groups may yield higher power savings. This is a matter of a further research.

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