International Journal of Research (IJR)
e-ISSN: 2348-6848, p- ISSN: 2348-795X Volume 3, Issue 01, January 2016
Available at http://internationaljournalofresearch.org

Implementation of Neural network based Control Scheme for Capacitor Voltage balancing of a Diode clamped inverter

A.Bhavana [1] & K.Kranthi Pratap Singh [2]
[1]M.Tech Scholar,Dept. of EEE, ASR College of Engineering and Technology, JNTUK, A.P
[2]Assistant Professor, Dept. of EEE, ASR College of Engineering and Technology, JNTUK, A.P

Abstract: — *This paper suggests an energetic front-end answer for you to stability this dc-link capacitor voltage of the five-level diode clamped inverter. Capacitor voltage handling is completed with a three-level raise converter connected to each intrinsic capacitors of a five level diode clamped inverter and additional handling circuits on the different two surface capacitors. An intelligent load control is employed to monitor the load and to regulate the output to the load such that converter is protected. The proposed configuration is tested by means of simulation for several heap electric power element problems at a large modulation index. The actual outcome proves the actual reliability of the offered settings to be able to harmony the actual dc-link capacitor voltage in the preferred degree. The control techniques are modeled and simulated in MATLAB using Simulink and Sim Power System set tool boxes.*
Keywords: DC-Link Capacitor Voltage Balancing; Diode Clamped; Multilevel Inverter; Three-Level Boost Converter (TLBC)

I. INTRODUCTION

Several very popular voltage-source multilevel inverters can be broken down straight into three different types according to their own topology: simple level clamped, flying capacitor, as well as cascade H-bridge [1]–[3].Scientific tests on three-, four-, five- as well as sixlevel diode-clamped inverters pertaining to such utilize similar to static VAR compensators, high voltage grid interconnections, as well as varied speed motor devices are already deemed [4]–[6]. It's extended been recently regarded in which, with the diode-clamped inverter with an increase of compared to three amounts, the passive frontend capacitor voltage managing procedure is possible if your modulation directory is fixed in order to with regards to 60% associated with it is utmost importance pertaining to loads with a standard 0. 8 strength issue. If your modulation directory will be improved over this kind of importance, the guts capacitors steadily release, last but not least, this inverter end result converges at three amounts [11]. To help overcome this kind of limitation, the multilevel inverter can be supplied by means of isolated dc solutions like external circuit because this productive front-end remedy associated with dc-link capacitor managing [10], using managing circuit by means of shifting cost in one capacitor to a new capacitor in order to stability level [11], [12] or this modification on the pulse width modulation (PWM) switching pattern.

Numerous creators of these studies suggested PWM tips for capacitor voltage managing in order to avoid more charge when you use lively front-end or managing routine. This technique can be found to get limit in the number regarding function while using the changing from the electrical power factor along with modulation list.. Once any PWM tactic is utilized with regard to dc-link capacitor voltage managing, resolving troubles for instance complete harmonic distortion, common-mode voltage cancellation, along with leakage latest removal while using the same tactic is not possible. It is brought up in the benefits regarding that capacitor voltage managing along with common mode Voltage cancellation is not reached together in a multilevel inverter.

International Journal of Research (IJR)
e-ISSN: 2348-6848, p- ISSN: 2348-795X Volume 3, Issue 01, January 2016
Available at http://internationaljournalofresearch.org

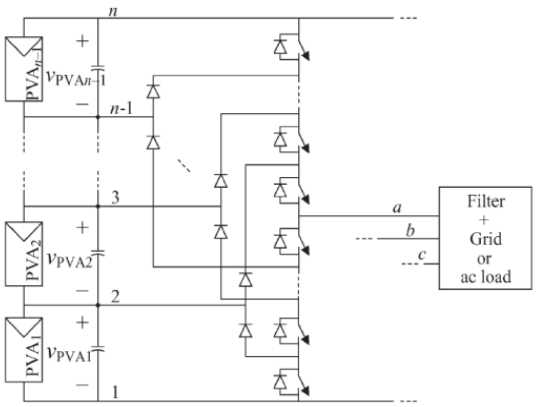


Fig. 1. Connection of n − 1 series-connected PVAs to the grid (or ac load) through an n-level three-phase diode clamped inverter.

In photovoltaic (PV) power systems, a conventional two level inverter is supplied by the series connection of PV arrays (PVAs). Partial shading, dust, and disparity in panel aging (yellowing) cause differences in the V−I characteristic of the PV string. The differences result to the rise of several local maximum power points in the string P−V curve that leads to the reduction of the power generated from its potential maximum [8]. It is more practical to install PV with fewer series connections and more on parallel connection. Some authors proposed a substitution of the conventional two level inverter by a multilevel inverter. The series of independently controlled PVAs placed parallel to every dc link capacitor is shown in Fig. 1. By using this configuration, the n-level inverter will need n−1 sets of PVAs. In this paper, a three-level boost converter (TLBC) is used to supply a five-level diode-clamped inverter as shown in Fig. 2.

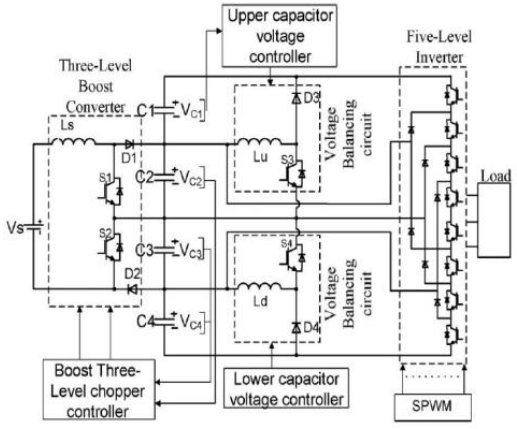


Fig2. Proposed three-level (TL) boost chopper and balancer circuit for C1 and C4

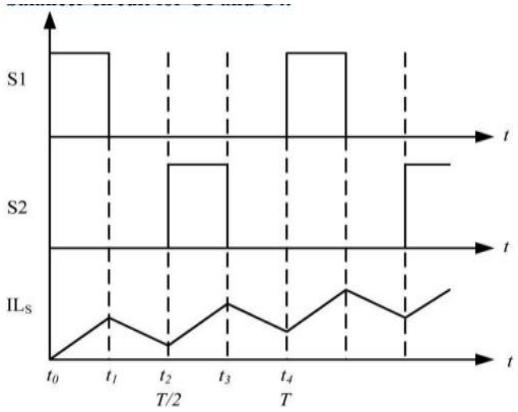


Fig.3. Switching signal and inductance current waves of boost TL chopper

In power alteration process, a good start chopper is normally applied because straight forward topology as well as manage technique. TLBC provides strengths within excessive power software for example diminished transitioning deficits as well as diminished slow restoration deficits of your diode [13]. Using diminished inductor current ripple within TLBC, a smaller dimensions inductor may be used within TLBC compared to the conventional boost converter. DC-link capacitor voltage controlling is conducted by using a mix of lively front-end along with controlling circuits. TLBC is utilized for you to sense of balance the two internal capacitors; C1 along with C2, along with one more controlling world is utilized for you to sense of balance the particular external capacitors, C1 along with C4, by means of shifting the particular charge in the internal capacitors on the external capacitors. Just about all management capabilities pertaining to TLBC, controlling circuits, and also the five-level inverter tend to be implemented thoroughly within software having a Tx Devices TMS320F28335 digital camera indication controller (DSC).

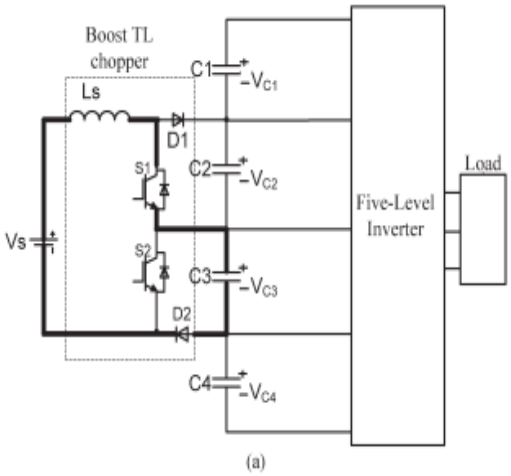
II. PROPOSED TOPOLOGY –INNER CAPACITOR BALANCING WITH TLBC

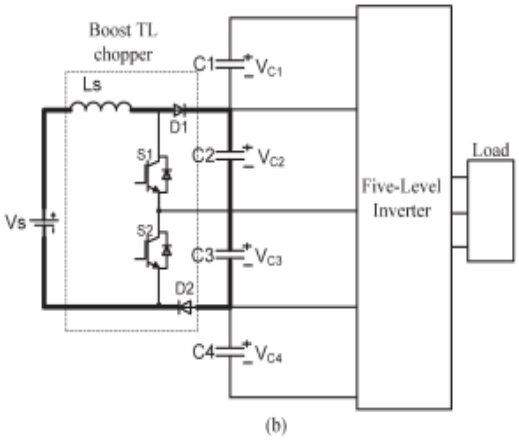
A. Basic diagram of the proposed system

The actual enterprise diagram involving TLBC can be found with Fig. 2. The actual buttons S1 along with S2 usually are turned don and doff also consider to. Fig. 3. displays your moving over indication waveforms and inductor current iLs intended for duty quotients (D < 0. 5). Via t0 to t1, S1 is usually with, and S2 is usually down; furthermore, your inductance current runs inside the signal marked having solid solid collections with

International Journal of Research (IJR)
e-ISSN: 2348-6848, p- ISSN: 2348-795X Volume 3, Issue 01, January 2016
Available at http://internationaljournalofresearch.org

Fig. 4(a). The force is usually stored inside the inductance, capacitor C3 is usually incurred, and VC3 little by little soars. Via t1 to t2 and t3 to t4, S1 and S2 are generally down, and current circulation is usually marked with Fig. 4(b). The force stored inside the inductance is usually transferred to C2 and C3. Via t2 to t3, S1 is usually down, and S2 is usually with. The inductance current flows in the circuit marked in Fig. 4(c). The energy is stored in inductance, capacitor C2 is charged, and VC2 gradually rises.





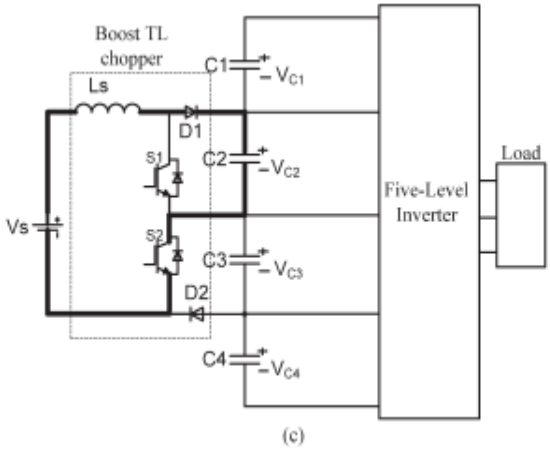


Fig. 4. Inner capacitor balancing using boost TL chopper.

Capacitors C2 and also C3 may be charged differently to the wanted voltage level by means of preventing the duty ratios D. Escalating some time length of time from t0 to t1 raises the actual voltage in capacitor C3, and also improving some time length of time from t2 to t3 raises the actual voltage in capacitor C2. TLBC may be run in several various algorithms [26]. In this kind of cardstock, only one formula the location where the period moving over involving S1 and that involving S2 tend not to overlapped one another can be used.

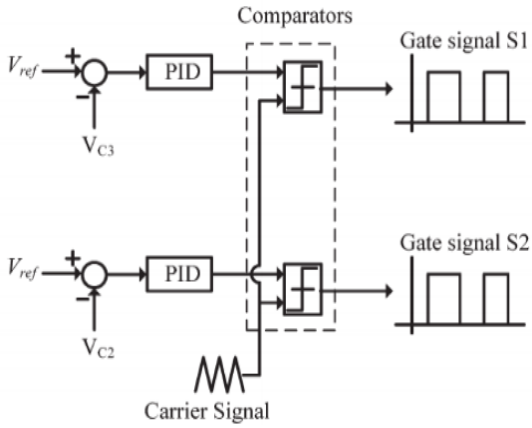


Fig. 5. Control diagram of the boost TL chopper.

The boost feature of the TLBC can be written as

$$V_o = V_{C2} + V_{C2} = \frac{2V_s}{(2-D)} \qquad (1)$$

where D is the duty ratio of this algorithm (2t1/T). D is varied from 0 to 1.

International Journal of Research (IJR)
e-ISSN: 2348-6848, p- ISSN: 2348-795X Volume 3, Issue 01, January 2016
Available at http://internationaljournalofresearch.org

The current ripple for the conventional boost inverter can be written as

$$\Delta I = V_s D T_{sw} / L_s \qquad (2)$$

where Tsw is the switching frequency of the conventional boost converter

The current ripple for TLBC operation is

$$\Delta I = \frac{V_o(1 - V_s/V_o)(2V_s/V_o - 1)}{2L_s f_{sw}} \qquad (3)$$

where fsw is the switching frequency of the conventional boost converter

Through (2) along with (3), this demonstrates the existing ripple of TLBC can be half the ripple that is generated by the typical enhance converter. It suggests that a good inductor of scaled-down dimension can be employed from the TLBC. To guarantee the equivalent voltage involving capacitors C2 and C3, some sort of voltage handling controller with regard to TLBC, revealed with Fig. 5, is needed. The duty rate from the enhance buttons S1 and S2 will be handled by simply using a proportional-integral-derivative (PID) controller exactly where Vref may be the desired dc voltage on C2 and C3.

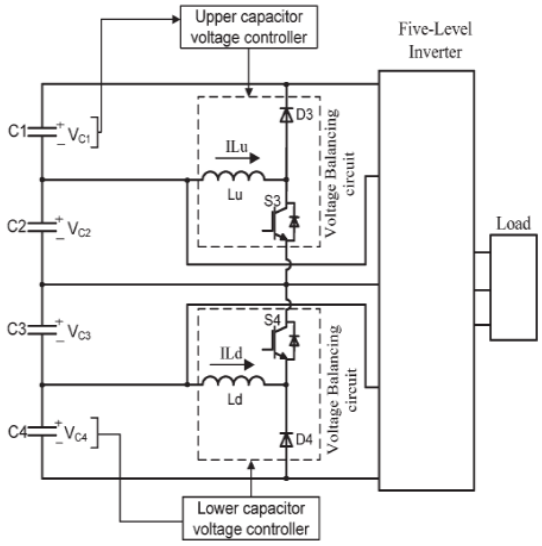


Fig.6. Outer capacitor balancing circuit

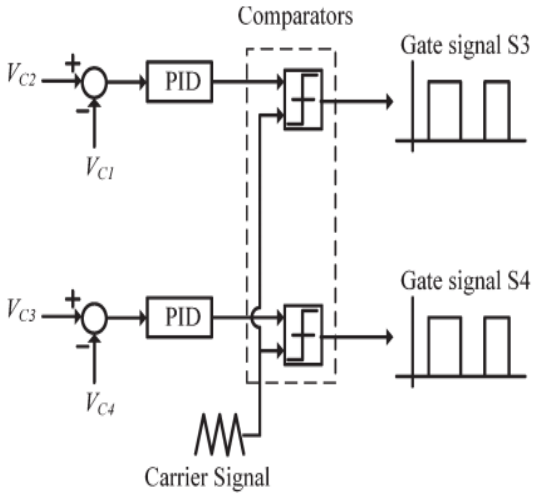


Fig.7. Balancing circuit control diagram.

This PID controller with regard to voltage regulations was designed to have a very proportional achieve (Kp) involving 20, an integral achieve (Ki) involving 0. 003, as well as a kind achieve (Kd) involving 10. Normally, simply by using a passive approach [11], [12], your dc origin is attached in between outside capacitors C1 as well as C4 while proven in Fig. 2, that is four times your specific capacitor voltage level. Much more line strings associated with PV sections have to be utilized to offer larger voltage that is improper in PV installation. This suggested configuration calls for reduced voltage level while proven in Fig. 4, where the outside capacitors aren't provided directly coming from your TLBC. This method is far more practical due to the fact just one pair of PVAs along with fewer series-connected PV sections is employed. Here in this paper , PID controller is replaced by Neural Network based controller for more accuracy and the corresponding results proves the proposed system is an effective one .

International Journal of Research (IJR)
e-ISSN: 2348-6848, p- ISSN: 2348-795X Volume 3, Issue 01, January 2016
Available at http://internationaljournalofresearch.org

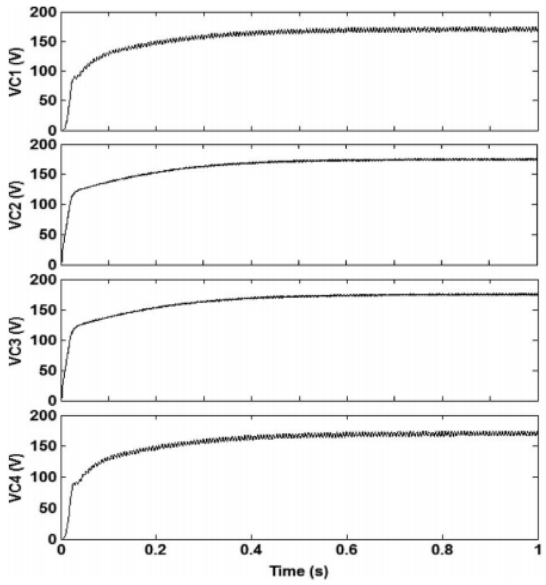


Fig. 8. DC-link capacitor voltage balancing using PID controller

B. Outer Capacitor Balancing Strategy :

Outside capacitors C1 and also C4 are usually manipulated with the handling world revealed within Fig. 6. The particular voltage on C1, Vc1, can be incurred on the voltage stage adequate to Vc2, along with the voltage on C4, Vc4, can be incurred on the voltage stage adequate to
Vc3 simply by changing the work relation involving S3 and also S4, respectively. Fig.7 exhibits this PID controllers helpful to harmony top of the capacitor C1 and also reduce capacitor C4. The particular controller is made with the price Kp = 10, Ki = 0. 001, and also Kd = 10.
Increasing the work relation involving S3 and also S4 will slow up the getting moment involving VC1 and also VC4, respectively. Nonetheless, when the job relation can be too big, the center capacitors C2 and also C3 will over discharge and also slow up the voltage on these capacitors. To solve this issue, this controller within Fig. 7 should operate with a reduced fee than the TLBC controller revealed within Fig. 5. Fig. 8 exhibits this simulation
consequence effectiveness involving both this PID controllers handling all four dc-link capacitors. During steady state, top of the inductor and also reduce inductor currents circulation continuously (ILu(t) > 0 and also ILd(t) > 0). As a result, the time essential in the inductor voltage around a single phase should be absolutely nothing.

$$V_{C2}t_{3on} + V_{C1}t_{3off} = 0. \qquad (4)$$

When VC2 as well as VC1 tend to be equal throughout degree, the actual steady-state obligation cycle associated with change S3 is going to be 0.5. The work cycle
pertaining to change S4 will in addition possibly be 0. 5 if VC3 is corresponding to VC4.

III. MATLAB BASED SIMULATION & RESULTS

The proposed configuration has been simulated using MATLAB/Simulink for the BLTC connected to a five-level diode-clamped inverter. The switching frequency of the BLTC was 5 kHz. To examine the balancing of dc-link capacitor voltage, a five-level diode-clamped inverter with a high modulation index of 1.0 is connected to variations of the load power factor.

To verify the feasibility of the proposed system a simulink model is developed. Fig.9 shows the sub system in the simulink model.

All the mathematical calculated simulatution parameters are given by table.1

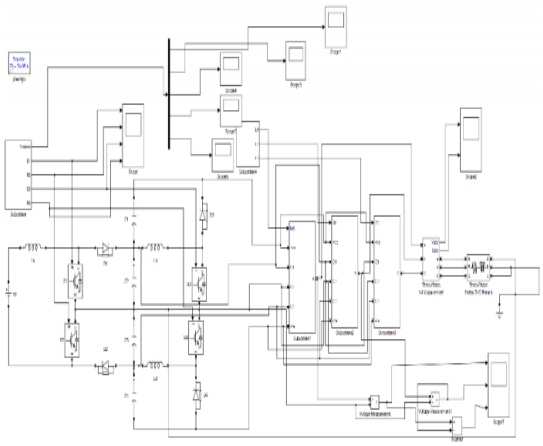
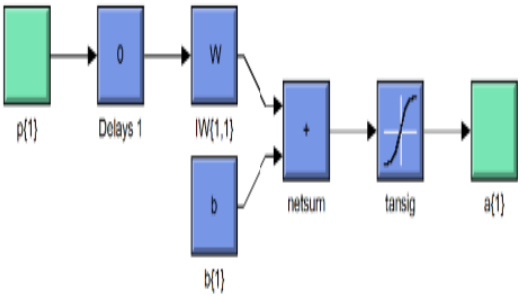


Fig.9.MATLAB based simulation diagram of proposed system with masked diagrams



International Journal of Research (IJR)
e-ISSN: 2348-6848, p- ISSN: 2348-795X Volume 3, Issue 01, January 2016
Available at http://internationaljournalofresearch.org

Fig.10.MATLAB based simulation diagram of proposed system with masked layer-1

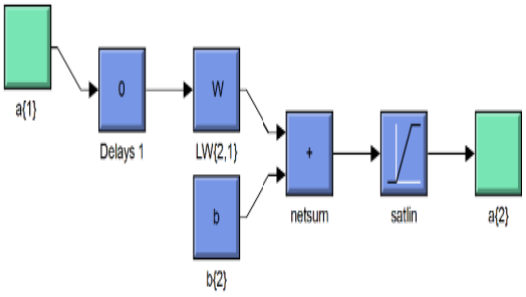
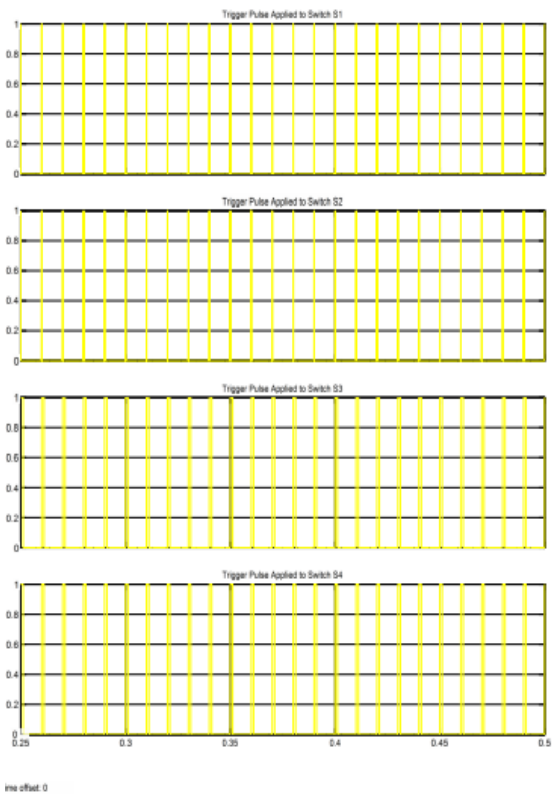


Fig.11.MATLAB based simulation diagram of proposed system with masked layer-2

Fig.12.MATLAB based simulation diagram of proposed system – (a) Load voltage (b) Load current

Fig.13.MATLAB based simulation diagram of proposed system – (a) Poles voltage-A (b) Poles voltage-B (c) Line-LineVoltag



International Journal of Research (IJR)
e-ISSN: 2348-6848, p- ISSN: 2348-795X Volume 3, Issue 01, January 2016
Available at http://internationaljournalofresearch.org

Fig.14.MATLAB based simulation diagram of gate pulses for proposed system

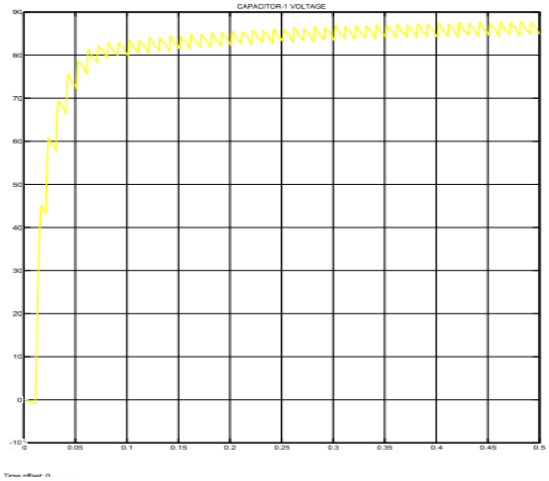


Fig.15.MATLAB based simulation diagram capacitor-1 voltage

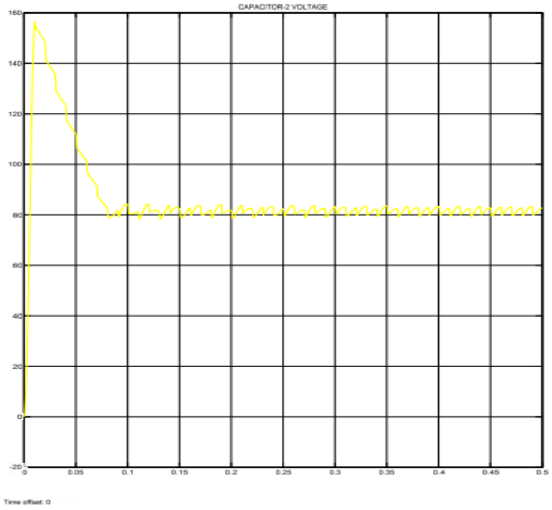


Fig.16.MATLAB based simulation diagram capacitor-2 voltage

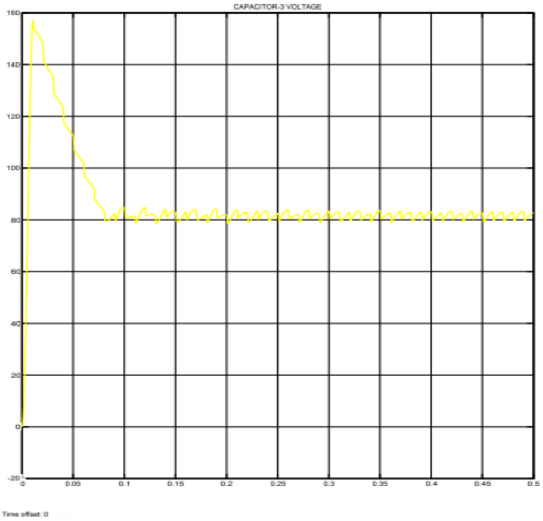


Fig.17.MATLAB based simulation diagram capacitor-3 voltage

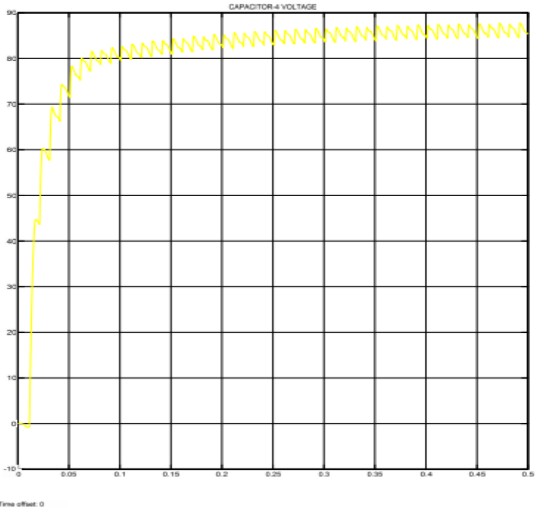


Fig.18.MATLAB based simulation diagram capacitor-4 voltage

APPENDIX TABLE.I.SIMULATION SPECIFICATIONS

Parameter	*Rating*
Input dc voltage	90-136 Vdc
Output dc voltage	110 V
Maximum output power	1.1 kW
Switching frequency	5 kHz
output voltage frequency	50Hz
R Load	150Ω
L Load	2.87 mH
Modulation Index	1.0

CONCLUSION

This paper has proposed a new configuration to balance the dc-link capacitor voltages of the five-level diode-clamped inverter with Neural Network based controller. Connecting a TLBC at the input of the inverter regulates the two inner dc-link capacitors' voltage at the desired level with the changing of the converter dc source and, at the same time, provides voltage balancing. Balancing circuits are added to balance the voltage of the two outer capacitors.

Overall, the investigations show that the proposed converter operates well in various load power factor

conditions. This configuration is suitable for the grid-connected PV system due to the unidirectional power transfer. In addition, only one set of PVAs is needed instead of four sets of independently controlled PVAs required to supply the inverter in the conventional system.

REFERENCES

[1] R. Stala, "A natural dc-link voltage balancing of diode-clamped inverters in parallel systems," *IEEE Trans. Ind. Electron.*, vol. 60, no. 11, pp. 5008– 5018, Nov. 2013.

[2] M. Khazraei, H. Sepahvand, K. A. Corzine, and M. Ferdowsi, "Active capacitor voltage balancing in single-phase flying-capacitor multilevel power converters," *IEEE Trans. Ind. Electron.*, vol. 59, no. 2, pp. 769– 778, Feb. 2012.

[3] S. A. Khajehoddin, A. Bakhshai, and P. K. Jain, "A simple voltage balancing scheme for m-level diode-clamped multilevel converters based on a generalized current flow model," *IEEE Trans. Power Electron.*, vol. 23, no. 5, pp. 2248–2259, Sep. 2008.

[4] M. M. Renge and H. M. Suryawanshi, "Threedimensional space-vector modulation to reduce commonmode voltage for multilevel inverter," IEEE Trans. Ind. Electron., vol. 57, no. 7, pp. 2324–2331, Jul. 2010.

[5] K. Hasegawa and H. Akagi, "Low-modulation-index operation of a fivelevel diode-clamped PWM inverter with a dc-voltage-balancing circuit for a motor drive," IEEE Trans. Power Electron., vol. 27, no. 8, pp. 3495– 3504, Aug. 2012.

[6] K. Hasegawa and H. Akagi, "A new dc-voltage balancing circuit including a single coupled inductor for a five-level diode-clamped PWM inverter," IEEE Trans. Ind. Appl., vol. 47, no. 2, pp. 841–852, Mar./Apr. 2011.

[7] H. A. Hotait, A. M. Massoud, S. J. Finney, and B.W.Williams, "Capacitor voltage balancing using redundant states of space vector modulation for five-level diode clamped inverters," IET Power Electron., vol. 3, no. 2, pp. 292–313, Mar. 2010.

[8] M. Jang and V. G. Agelidis, "A minimum power-processing-stage fuelcell energy system based on a boost-inverter with a bidirectional backup battery storage," *IEEE Trans. Power Electron.*, vol. 26, no. 5, pp. 1568–1577, May 2011.

[9] K. Beer and B. Piepenbreier, "Properties and advantages of the quasi-Zsource inverter for DC–AC conversion for electric vehicle applications," *Proc. Electr. Power Train Emobility*, pp. 1–6, 2010.

[10] A. Florescu, O. Stocklosa, M. Teodorescu, C. Radoi, D. A. Stoichescu, and S. Rosu, "The advantages, limitations and disadvantages of Z-source inverter," in *Proc. 2010 Int. Semicond. Conf. (CAS)*, Oct. 2010, vol. 2, pp. 483, 486.

[11] B. S. Prasad, S. Jain, and V. Agarwal, "Universal single-stage gridconnected inverter," *IEEE Trans. Energy. Convers.*,, vol. 23, no. 1, pp. 128– 137, Mar. 2008.

[12] T.F. Wu, Y.S. Lai, J.C. Hung and Y.M. Chen, ―Boost Converter with Coupled Inductors and Buck–Boost Type of Active Clamp‖ *IEEE Trans Ind. Electron.*,vol. 55, no. 1, Jan. 2008.

[13] B. Axelrod, Y. Berkovich and A.Ioinovici, ―Switched Capacitor/Switched-Inductor Structures for Getting Transformerless Hybrid DC–DC PWM Converters‖, *IEEE Trans Circuits And Systems—I: Regular Papers*, Vol. 55, no. 2, Mar 2008.

[14] D. Sabin and A. Sundaram, "Quality enhances reliability," *IEEE Spectrum*, vol. 33, no. 2, Feb. 1996, pp. 34-41.

[15] R.J. Wai, C.Y. Lin, C.Y. Lin, R.Y. Duan and Y.R. Chang, ―HighEfficiency Power Conversion System for Kilowatt-Level StandAlone Generation Unit with Low Input Voltage‖, *IEEE Trans Ind.Electron.*, vol. 55, no. 10, Oct 2008.

[16] G.S. Yang, T.J. Liang and J.F. Chen, ―Transformerless DC–DC Converters With High Step-Up Voltage‖, *IEEE Trans Ind.Electron.*, vol. 56, no. 8, Aug 2009.

[17] J.M. Burkhart, R. Korsunsky, and D.J. Perreault, ―Design Methodology For A Very High Frequency Resonant Boost Converter‖, *IEEE Trans. Power Electron.*, vol. 28, no. 4, Apr 2013.

[18] F.S. Garcia, J.A. Pomilio and G. Spiazzi, ―Modeling and Control Design of the Interleaved Double Dual Boost Converter‖, *IEEETrans Ind. Electron.*,vol. 60, no. 8, Aug 2013.

[19] F.H. Dupont, C. Rech, R. Gules and J. R. Pinheiro, ―Reduced Order Model and Control Approach for the Boost Converter With a Voltage Multiplier Cell‖, *IEEETrans Power Electron.,vol.* 28, no. 7, July 2013.

[20] R. J. Wai and R. Y. Duan, ―High step-up converter with coupledinductor,‖ *IEEE Trans.Power Electron.*, vol. 20, no. 5, pp. 1025–1035, Sep. 2005.

[21] R. J. Wai, L. W. Liu and R. Y. Duan, ―High efficiency voltage clamped dc–dc converter with reduced reverse-recovery current and switch voltage stress,‖ *IEEE Trans. Ind. Electron..*, vol. 53, no. 1, pp. 272–280,Feb. 2005.

[22] J. W. Baek, M. H. Ryoo, T. J. Kim, D. W. Yoo and J. S. Kim, ―High boost converter using voltage multiplier,‖ in *Proc. IEEEIECON*, 2005, pp. 567–572.

[23] S.K. Changchien, T.J Liang, J.F. Chen and L.S. Yang, ―Novel High Step-Up DC–DC Converter for Fuel Cell Energy Conversion System‖, *IEEE Trans Ind. Electron.*, vol. 57, no. 6, June 2010.

[24] Y. Zhao, Y. Deng and Xiangning, ―Interleaved Converter with Voltage Multiplier Cell for High Step-Up and High Efficiency Conversion‖, *IEEE Trans. Power Electron.*, vol. 25, no. 9, Sep 2010.