

# Cascade Multilevel Inverter Based on H-Bridge Unit for Production of 56-Levels

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**Abstract:**— *Multilevel inverters have received more attentions their considerable advantages such as high power quality, lower harmonic components, better electro- magnetic consistence, lower dv/dt and lower switching losses. Lot of research was going on multi level inverter topologies and many researchers are proposed so many multi level inverter topologies. Most of the research conducted on these topologies emphasizes on voltage stress reduction, usage of optimized number of switches for production of more number of levels at the output terminals. In this project a single phase multi level configuration based on H-Bridge units for production of 56 levels in the output terminals is proposed for analysis. Mathematical modeling and simulation studies using Sim power systems Block set of MATLAB are proposed. Switching scheme for the proposed converter circuit is designed with the help of sinusoidal pulse width modulation scheme. Total Harmonic distortion in the output voltage is evaluated using FFT tool of MATLAB SIMULINK.*

**Keywords:** Hybrid cascaded multilevel inverter; Total harmonic Distortion; Sinusoidal Pulse width modulation; H-Bridge Units; Switching control;

## INTRODUCTION

The application of (FACTS) controllers, such flexible ac transmission systems as static compensator (STATCOM) and static synchronous series compensator (SSSC), is increasing in power systems. This is due to their ability to stabilize the transmission systems and to improve power quality (PQ) in distribution systems. STATCOM is popularly accepted as a reliable reactive power controller replacing conventional var compensators, such as the thyristor-switched capacitor (TSC) and thyristor-controlled reactor

(TCR). This device provides reactive power compensation, active power oscillation damping, flicker attenuation, voltage regulation, etc...

Generally, in high-power applications, var compensation is achieved using multilevel inverters [2]. These inverters consist of a large number of dc sources which are usually realized by capacitors. Hence, the converters draw a small amount of active power to maintain dc voltage of capacitors and to compensate the losses in the converter. However, due to mismatch in conduction and switching losses of the switching devices, the capacitors voltages are unbalanced. Balancing these voltages is a major research challenge in multilevel inverters. Various control schemes using different topologies are reported in [3]–[7]. Among the three conventional multilevel inverter topologies cascade H-bridge is the most popular for static var compensation[5],[6]. However, the aforementioned topology requires a large number of dc capacitors. The control of individual dc-link voltage of the capacitors is difficult.

Each bidirectional power switch includes two IGBTs, two power diodes, and one driver circuit if the common emitter configuration is used. Therefore, in these topologies, the installation space and total cost of the inverter increase. As a result, several asymmetric cascaded multilevel inverters have been presented in which the unidirectional switches from the voltage point of view and the bidirectional switches from the current point of view are used in them. Each unidirectional switch consists of an IGBT with an anti parallel diode. Two of these topologies have

been presented in [20]. Two other algorithms for the H-bridge cascaded multilevel inverter have been also presented in [9] and [10]. Because of the asymmetric topology and used unidirectional switches, it seems that the lower number of power electronic devices is the main advantage of these inverters. However, the main disadvantage of the asymmetric topologies is the lost of modularity, which means the use of a high variety of semiconductor devices and dc voltage sources.

In this paper, a new single-phase cascaded multilevel inverter with series connection of the novel H-bridge basic units is proposed. Moreover, nine different algorithms to determine the magnitude of dc voltage sources are proposed to generate all output voltage levels. These algorithms are compared to each other from the number of required IGBTs, dc voltage sources, and different voltage amplitudes of the used source points of view. These investigations are done to determine the best proposed algorithm. Then, the proposed topology with its best proposed algorithm is compared to the conventional topologies. These comparisons consist of the amount of the blocked voltage by switches and the number of used power electronic devices. Finally, in order to reconfirm the correct performance of the proposed cascaded multilevel inverter and its algorithms in generating all voltage levels, the experimental results of a single-phase 56-level inverter based on the proposed topology are used.

### I. PROPOSED TOPOLOGY AND IT'S OPERATION

The topology of the novel H-bridge basic unit is shown in Fig. 1. This unit consists of six unidirectional power switches from the voltage point of view ( $SL,1$ ,  $SL,2$ ,  $SR,1$ ,  $SR,2$ ,  $Sa$ , and  $Sb$ ) and two insulated dc voltage sources ( $VL,1$  and  $VR,1$ ), which is called the developed H-bridge unit [22]. The main disadvantage of the

proposed basic unit over the H-bridge is its higher number of required dc voltage sources and power switches; however, this basic unit is able to generate seven different levels at the output, whereas three output levels are only generated in the H-bridge. In addition, in each switching pattern, one power switches from each leg ( $SL,1$  or  $SL,2$ ), ( $SR,1$  or  $SR,2$ ), and  $Sa$  or  $Sb$  are turned on simultaneously.

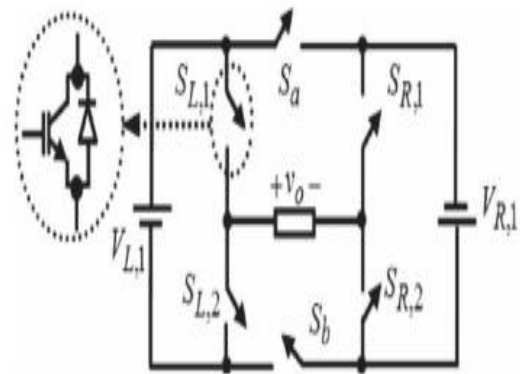


Fig. 1. Basic unit based on developed H-bridge.

If the magnitudes of the dc voltage sources are equally considered, the proposed inverter can generate five levels at the output. Therefore, in order to generate more numbers of output levels at the output, the magnitude of dc voltage sources have to be selected differently. Therefore, the magnitude of the dc voltage sources is considered as follows:

$$V_{R,1} = V_{dc} \quad (1)$$

$$V_{L,1} = 2V_{dc} \quad (2)$$

A new cascaded multilevel inverter can be made by series connection of  $n$  number of the H-bridge basic units. This inverter is shown in Fig. 2. According to Fig. 2, the output voltage of the proposed cascaded multilevel inverter is equal to adding the output levels of different units and is given by

$$v_o(t) = v_{o,1}(t) + v_{o,2}(t) + \dots + v_{o,n}(t). \quad (3)$$

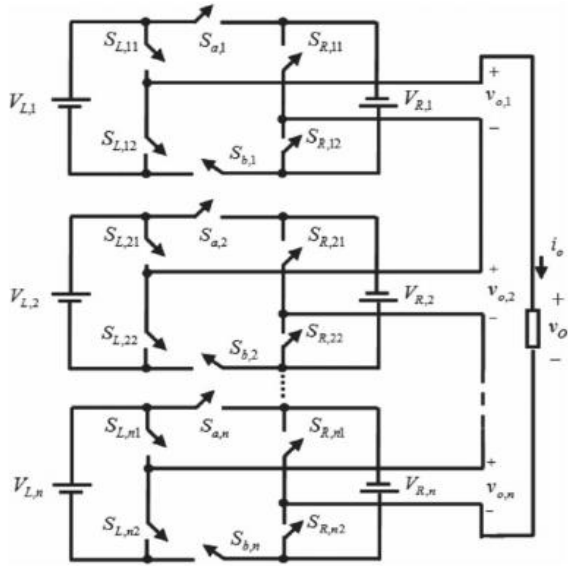


Fig.2. Proposed cascaded multilevel inverter.

In the proposed cascaded multilevel inverter for 56 levels, the number of switches ( $N_{switch}$ ), IGBTs ( $N_{IGBT}$ ), driver circuits ( $N_{driver}$ ), and dc voltage sources ( $N_{source}$ ) are calculated as follows:

$$N_{switch} = N_{IGBT} = N_{driver} = 6n \quad (4)$$

$$N_{source} = 2n. \quad (5)$$

The other main parameter in calculating the total cost of the inverter is the maximum amount of the blocked voltage by switches. If the values of the blocked voltage by switches are reduced, the total cost of the inverter decreases [9]. Therefore, in order to calculate this index, it is necessary to consider the amount of the blocked voltage by each of the switches. According to Fig. 2, the values of the blocked voltage by switches  $SR,1$  and  $SR,2$  are equal to

$$V_{SR,1} = V_{SR,2} = V_{R,1}. \quad (6)$$

In (6),  $V_{SR,1}$  and  $V_{SR,2}$  indicate the values of the blocked voltage by switches  $SR,1$  and  $SR,2$ , respectively. The value of the blocked voltage by switches  $SL,1$  and  $SL,2$  is equal to

$$V_{SL,1} = V_{SL,2} = V_{L,1}. \quad (7)$$

In (7),  $V_{SL,1}$  and  $V_{SL,2}$  indicate the values of the blocked voltage by switches  $SL,1$  and  $SL,2$ , respectively. Moreover, the values of the blocked voltage by switches  $Sa$  and  $Sb$  are equal to

$$V_{Sa} = V_{Sb} = V_{R,1} + V_{L,1} \quad (8)$$

where  $V_{Sa}$  and  $V_{Sb}$  indicate the values of the blocked voltage by switches  $Sa$  and  $Sb$ , respectively.

Therefore, the maximum amount of the blocked voltage by all of the used switches in the first unit, i.e.,  $V_{block,1}$ , is equal to

$$V_{block,1} = 4(V_{R,1} + V_{L,1}). \quad (9)$$

Similarly, the maximum value of the blocked voltage by the switches in other units is calculated, and thus, the maximum amount of the blocked voltage in the proposed cascaded multilevel inverter, i.e.,  $V_{block}$ , is equal to

$$\begin{aligned} V_{block} &= V_{block,1} + V_{block,2} + \dots + V_{block,n} \\ &= 4(V_{R,1} + V_{L,1} + V_{R,2} + V_{L,2} + \dots + V_{R,n} + V_{L,n}). \end{aligned} \quad (10)$$

In [14], the H-bridge cascaded multilevel inverter with two different algorithms has been presented. This topology and its algorithms are considered by  $R1$  and  $R2$  in this investigation. Moreover, two other algorithms for this inverter have been presented in [9] and [10]. These algorithms are indicated by  $R3$  and  $R4$ , respectively. The other presented symmetric cascaded multilevel inverters in [15] and [16] are indicated by  $R7$  and  $R10$ , respectively. Other asymmetric topology has been also presented in [20]. In this investigation, this topology is shown by  $R8$ . It is important to note that the unidirectional power switches from the voltage point of view are used in all of the aforementioned topologies. Moreover, several asymmetric cascaded multilevel inverters with bidirectional switches have been presented in [17]–[19] and [21]. These topologies are shown by  $R5$ – $R6$ ,  $R11$ , and  $R8$ , respectively.

Fig. 3. compares the number of the IGBTs in the proposed topology and the conventional cascaded multilevel inverters. As it is obvious from Fig. 3, the number of IGBTs in the proposed cascaded multilevel inverter is less than other topologies. As mentioned before, in the proposed topology, the number of switches, power diodes, and driver circuits is the same as the number of IGBTs. This comparison shows that the number of used power switches in the proposed topology is not only lower than the topologies with bidirectional switches but also less than the topologies with unidirectional ones. As a result, the proposed topology has a better feature in this point of view.

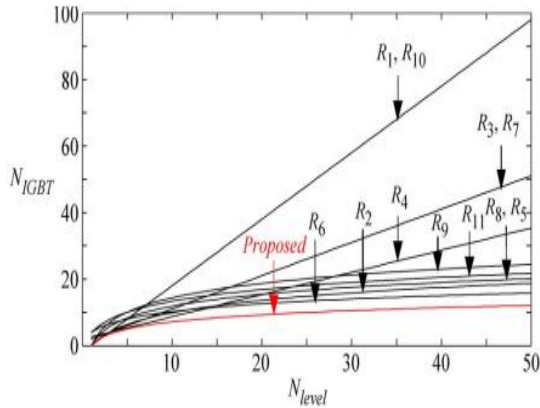


Fig.3. Variation of  $N_{IGBT}$  versus  $N_{level}$

Fig. 4. shows the comparison of the number of required dc voltage sources. As Fig. 4. indicates, the number of required dc voltage sources in the proposed inverter is lower than the other aforementioned topologies instead of the topologies that are indicated by R9.

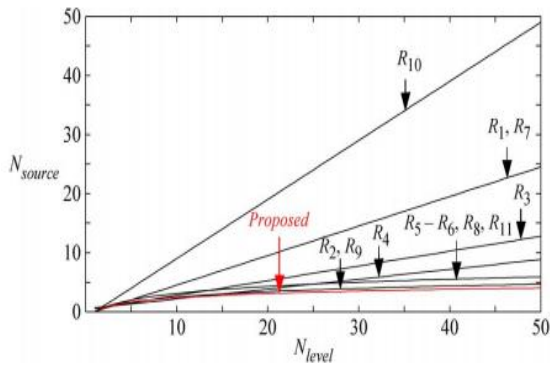


Fig.4. Variation of  $N_{source}$  versus  $N_{level}$ .

Fig. 5. compares the number of different voltage amplitudes of the used sources in the proposed inverter and the conventional cascaded multilevel inverters. In this comparison, the first proposed algorithm is considered. This selection is based on the obtained result from Fig. 5. It is obvious from Fig. 5. that the proposed cascaded multilevel inverter has a lower number of different voltage amplitudes of the used sources. However, this index in the proposed inverter is the same as the topologies that are shown by R1, R7, and R10. It is also important to note that the number of different voltage amplitudes of the used sources is one of the most important features in determining the cost of an inverter. By reducing this amount, the total cost of the inverter decreases. Therefore, this feature is one of the most important advantages of the proposed topology.

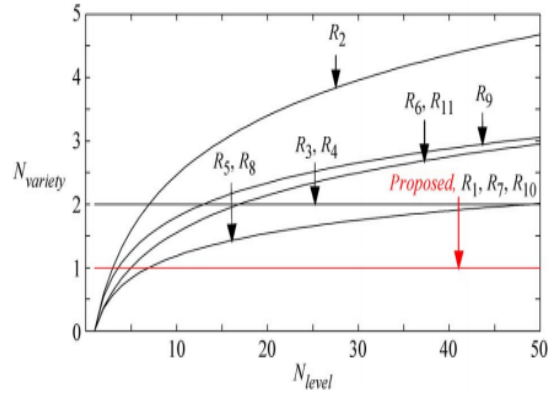


Fig. 5. Variation of  $N_{variety}$  versus  $N_{level}$ .

Fig. 6. compares the magnitude of the blocked voltage by the switches in the proposed inverter and the conventional cascaded multilevel inverters. Fig. 6. shows that the proposed topology consists of the lowest amount of the blocked voltage by switches. This feature in the proposed topology is the same as the topologies that are shown by R1 R4 and R10. This feature is known as one of the main important indexes in selecting the kinds of power switches and determines the total cost of the inverter. Therefore, if the value of the blocked voltage is reduced, the used switches have lower rating, and thus, the total cost of the inverter decreases. It is point out that all values are considered in per unit.

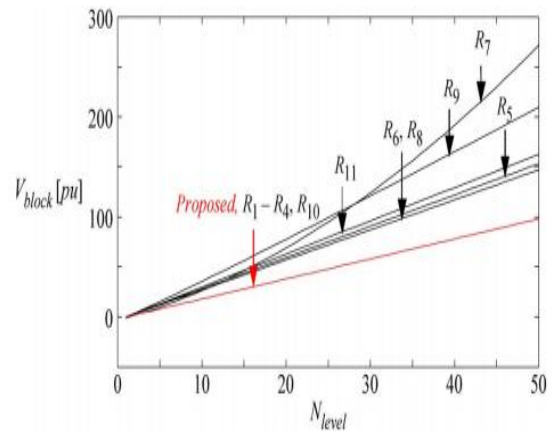


Fig. 6. Variation of  $V_{block}$  versus  $N_{level}$ .

It is clear that the proposed cascaded multilevel inverter requires a minimum number of IGBTs, power diodes, driver circuits, and dc voltage sources. In addition, in this inverter, the different voltage amplitudes of the used sources and the amount of the blocked voltage by switches are also less than the most of the conventional cascaded multilevel inverters that have been presented in the literatures, except the H-bridge cascaded multilevel inverter. These features lead to reduction of the installation space and total cost of the



inverter, whereas the number of output voltage levels is increased. As a result, this inverter could be a suitable topology to replace the conventional cascaded inverters in many of applications such as drive and control of electrical machines, connection of renewable sources, flexible alternating current transmission system devices, etc. Although the proposed inverter needs several insulated dc voltage sources, it is important to note that many of the conventional cascaded multilevel inverters, such as the presented topologies in [14], [16], and [20], require a higher number of insulated dc voltage sources. In other words, in the proposed cascaded multilevel inverter, the minimum number of insulated dc voltage sources is used.

## II. MATLAB BASED SIMULATION & IT'S RESULTS

Fig.7. shows the MATLAB based simulation diagram of proposed system.

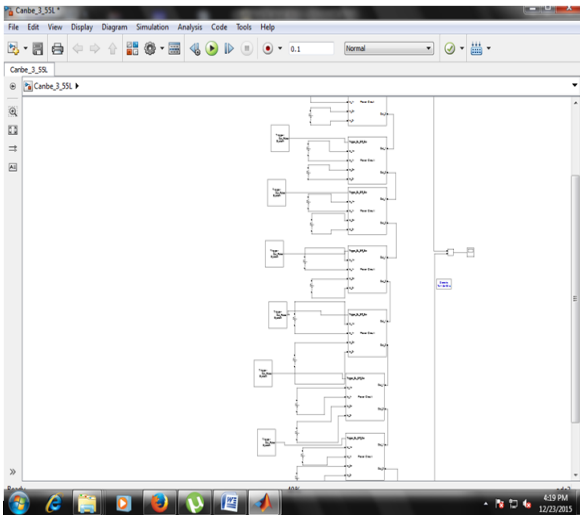


Fig.7. MATLAB based simulation diagram of proposed system

Fig.8. shows the MATLAB based simulation waveform diagram of proposed system with 56 levels

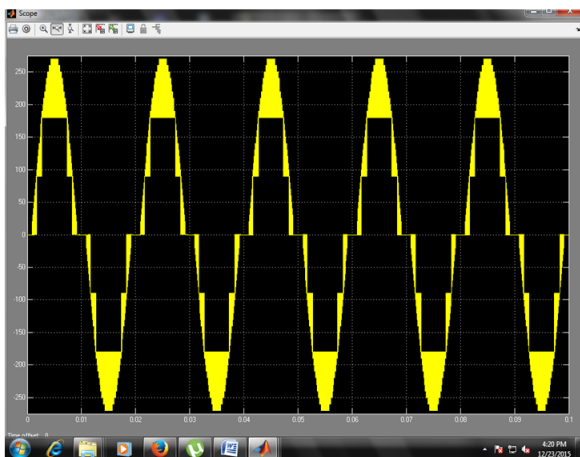


Fig.8. MATLAB based simulation waveform diagram of proposed system with 56 levels

Table.1 shows the simulation parameters for the proposed system

TABLE .I.SIMULATION SPECIFICATIONS

<i>Parameter</i>	<i>Rating</i>
R-C Filters	$R = 100 \Omega, L = 55 \text{ mH}$
R-L Filters	$R = 100 \Omega$ and $L = 55 \text{ mH}$
Stepped levels	56
Source frequency	60 Hz
Maximum output voltage	240 V

## III. CONCLUSION & FUTURE SCOPE

Mathematical model of the proposed hybrid cascaded multilevel inverter based on H-bridge unit for production of 56 levels is derived. The proposed model is simulated with the help of MATLAB SIMULNK software. It has been observed that the model require less number of switching devices for production of 56 levels in the output when compared with their counter parts like Cascaded H-Bridge inverters, Neutral point clamped inverters and flying capacitor inverters. As the proposed inverter configuration uses less number of switching devices the switching losses are minimized. It has been observed that the inverter configuration proposed gives reduced the total harmonic distortion. More levels are available at the output terminals for a given value of output voltage, voltage sources having low magnitude can be used at the input terminals.

The proposed topology is controlled with Sinusoidal Pulse Width modulation, Implementation of Closed loop control would not be a difficult task. The proposed configuration require more number of sources at the input terminals, interfacing with a Photo Voltaic Cell arrays would be very easy. More number of levels are available at the output terminals of the inverter, this inverter can be used in FACTS devices as a voltage regulator and reactive power compensator .

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